N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		20 Terminal Ceramic LCC	Die
60V	3Ω	VN2106NF	VN2106ND
100V	3Ω	VN2110NF	VN2110ND

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

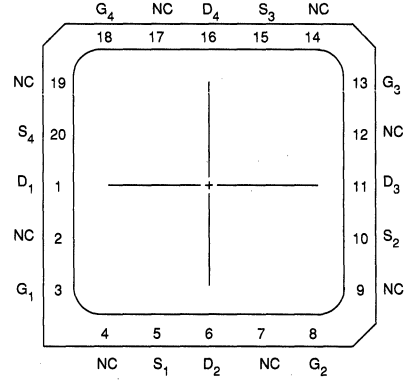
- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view

20-pin Ceramic LCC

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation* @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}
20 Terminal LCC	0.46A**	2.0A	1.25W	170	100	0.46A**	2.0A

† I_D (continuous) is limited by max rated T_j.

* Total for package.

** Single die.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN2110	100			V	I_D = 1mA, V_{GS} = 0
		VN2106	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	I_D = 1mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage			0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				1		V_{GS} = 0, V_{DS} = Max Rating
					100	µA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	V_{GS} = 5V, V_{DS} = 25V
			1.0	2.50			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4.50	5	Ω	V_{GS} = 5V, I_D = 250mA
				2	3		V_{GS} = 10V, I_D = 1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.70	1.0	%/°C	I_D = 1A, V_{GS} = 10V
G_{FS}	Forward Transconductance		300	400		m℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance				50	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance				25		
C_{RSS}	Reverse Transfer Capacitance				5		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 1.0A R_S = R_L = 50Ω
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	I_{SD} = 2.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			400		ns	I_{SD} = 1.0A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit