VN4012 SERIES

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

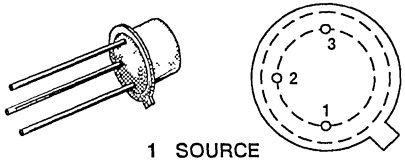
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN4012L	400	12	0.16	TO-92
VN4012B	400	12	0.42	TO-205AF
VN3515L	350	15	0.15	TO-92

Performance Curves: **VNDV40** (See Section 7)

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-205AF BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN4012L	VN4012B[2]	VN3515L	UNITS
Drain-Source Voltage		V_{DS}	400	400	350	V
Gate-Source Voltage		V_{GS}	±30	±20	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.16	0.42	0.15	A
	T_A = 100°C		0.10	0.27	0.09	
Pulsed Drain Current[1]		I_{DM}	0.65	1.3	0.60	
Power Dissipation	T_A = 25°C	P_D	0.80	5	0.80	W
	T_A = 100°C		0.32	2	0.32	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN4012L	VN4012B	VN3515L	UNITS
Junction-to-Ambient	R_{thJA}	156	125	156	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case for all temperature tests

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				VN4012		VN3515		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	420	400		350		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.6	1.8	0.6	1.8	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10		±10	nA
		T_J = 125°C	±5					
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V	0.002		1		1	µA
		T_J = 125°C	0.8		100		100	
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	300	150		150		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 100 mA	9					Ω
		V_{GS} = 4.5 V, I_D = 100 mA	9.5		12		15	
		T_J = 125°C	17		30		35	
Forward Transconductance[3]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA	350	125		125		mS
Common Source Output Conductance[3]	g_{OS}		17					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	80		90		90	pF
Output Capacitance	C_{oss}		10		20		20	
Reverse Transfer Capacitance	C_{rss}		2		5		5	
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 250 Ω, I_D = 0.1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3.5		20		20	ns
	t_r		2		20		20	
Turn-Off Time	$t_{d(OFF)}$		25		65		65	
	t_f		15		65		65	

NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for VN4012B.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.