INTERSIL

VN40AF, VN67AF, VN89AF
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- Simple DC biasing
- Extended safe operating area
- Inherently temperature stable
- Reliable, low cost plastic package

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers
- DC motor controllers

2

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- VN40AF 40V
- VN67AF 60V
- VN89AF 80V

Drain-gate Voltage
- VN40AF 40V
- VN67AF 60V
- VN89AF 80V

Continuous Drain Current (see note 1) 1.7A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... −0.3V
Thermal Resistance, Junction to Case ..... 10.4°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 12W

Linear Derating Factor ..... 96mW/°C
Operating Junction
- Temperature Range ..... −40 to +150°C

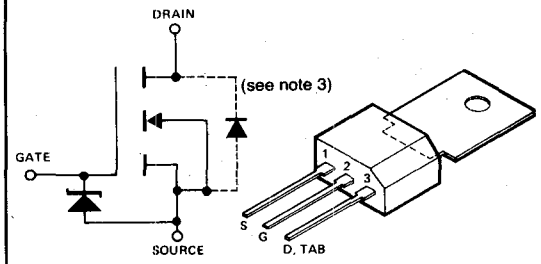
Storage Temperature Range ..... −40 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

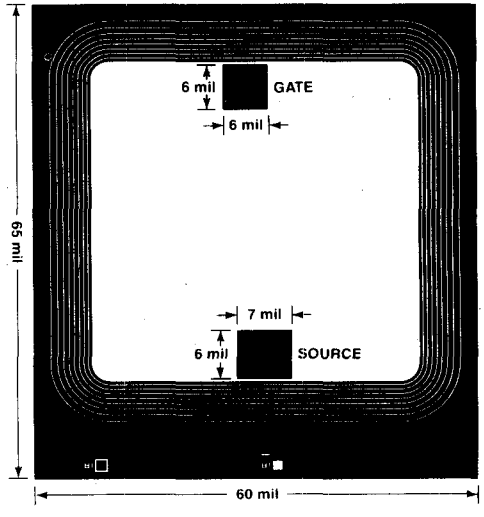
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-202)



Body internally connected to source.
Drain common to tab.

CHIP TOPOGRAPHY



VN40AF, VN67AF, VN89AF

INTERSIL

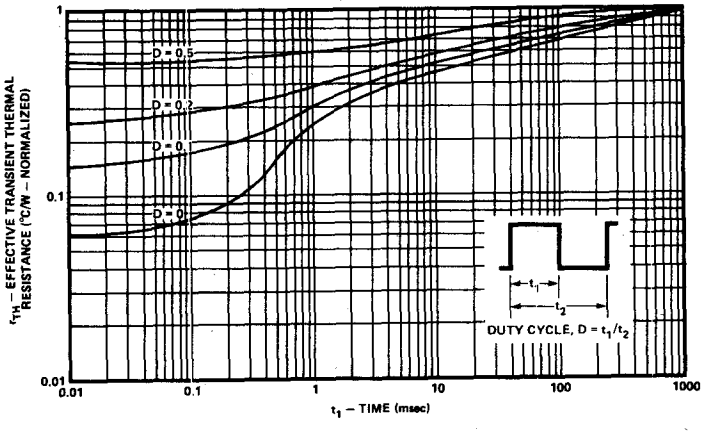
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		VN40AF			VN67AF			VN89AF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 10μA	
2				40			60			80				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate-Threshold Voltage	0.6	1.2		0.8	1.2		0.8	1.2			V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10V, V_{DS} = 0	
5						100			100			100		V_{GS} = 10V, V_{DS} = 0, T_A = 125°C (Note 2)	
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, V_{GS} = 0	
7						100			100			100		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.3			0.4		V	V_{GS} = 5V, I_D = 0.1A	(Note 1)
11					1.0	2.0		1.0	1.7		1.4	1.9		V_{GS} = 5V, I_D = 0.3A	
12					1.0			1.0			1.3			V_{GS} = 10V, I_D = 0.5A	
13					2.2	5.0		2.2	3.5		2.2	4.5		V_{GS} = 10V, I_D = 1.0A	
14	DYNAMIC	g_m	Forward Transconductance		250			250			250		mU	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	
15		C_{iss}	Input Capacitance			50			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz	(Note 2)
16		C_{rss}	Reverse Transfer Capacitance			10			10			10			
17		C_{oss}	Common-Source Output Capacitance			50			50			50			
18		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5		2	5	ns		
19		t_r	Rise Time		2	5		2	5		2	5			
20		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5		2	5			
21		t_f	Fall Time		2	5		2	5		2	5			

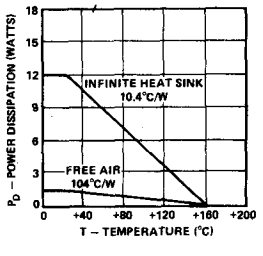
Note 1. Pulse test — 80μs pulse, 1% duty cycle.
Note 2. Sample test.

2

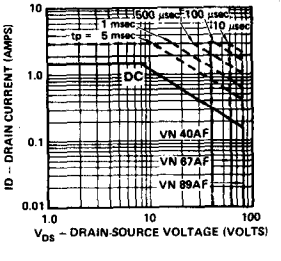
THERMAL RESPONSE



POWER DISSIPATION vs CASE TEMPERATURE



DC SAFE OPERATING REGION T_C = 25°C



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE