

VN40AF, VN67AF, VN89AF

n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- Simple DC biasing
- Extended safe operating area
- Inherently temperature stable
- Reliable, low cost plastic package

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-source Voltage

VN40AF	40V
VN67AF	60V
VN89AF	80V

Drain-gate Voltage

VN40AF	40V
VN67AF	60V
VN89AF	80V

Continuous Drain Current (see note 1) 1.7A

Peak Drain Current (see note 2) 3.0A

Continuous Forward Gate Current 2.0mA

Peak-gate Forward Current 100mA

Peak-gate Reverse Current 100mA

Gate-source Forward (Zener) Voltage +15V

Gate-source Reverse (Zener) Voltage -0.3V

Thermal Resistance, Junction to Case 10.4°C/W

Continuous Device Dissipation at (or below)

25°C Case Temperature 12W

Linear Derating Factor $96\text{mW}/^\circ\text{C}$

Operating Junction

Temperature Range -40 to $+150^\circ\text{C}$

Storage Temperature Range -40 to $+150^\circ\text{C}$

Lead Temperature

(1/16 in. from case for 10 sec) $+300^\circ\text{C}$

Note 1. $T_C = 25^\circ\text{C}$; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width $80\mu\text{sec}$, duty cycle 1.0%.

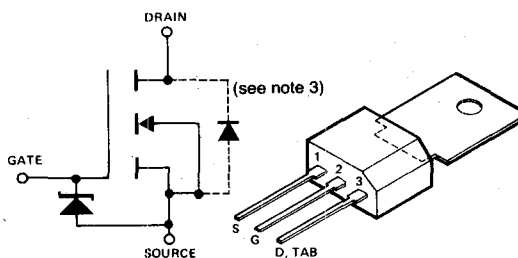
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers
- DC motor controllers

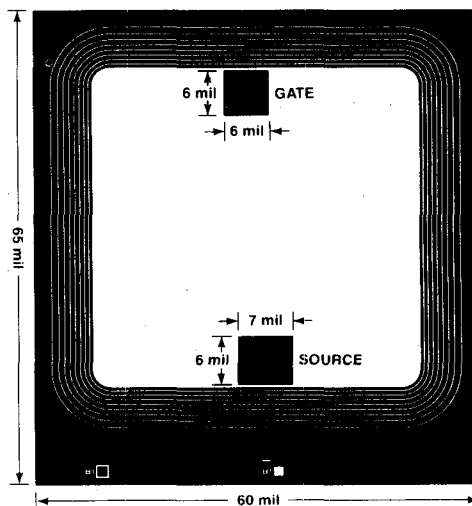
2

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-202)



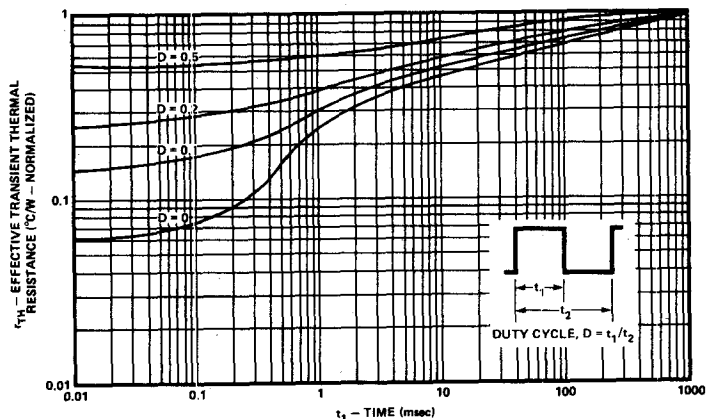
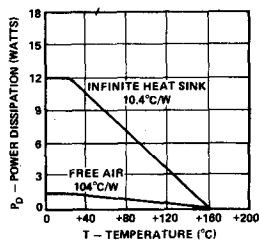
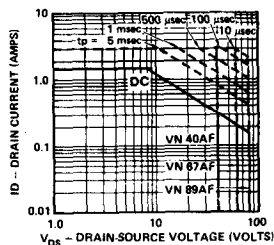
Body internally connected to source.
Drain common to tab.

CHIP TOPOGRAPHY



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	CHARACTERISTIC	VN40AF			VN67AF			VN89AF			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	BV _{DSS} Drain-Source Breakdown	40			60			80			V	V _{GS} = 0, I _D = 10μA
2		40			60			80				V _{GS} = 0, I _D = 2.5mA
3	V _{GS(th)} Gate-Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2			V _{DS} = V _{GS} , I _D = 1mA
4	I _{GSS} Gate-Body Leakage		0.01	10		0.01	10		0.01	10		V _{GS} = 10V, V _{DS} = 0
5	Zero Gate Voltage Drain Current			100			100			100	μA	V _{GS} = 10V, V _{DS} = 0, T _A = 125°C (Note 2)
6				10			10			10		V _{DS} = Max. Rating, V _{GS} = 0
7				100			100			100		V _{DS} = 0.8 Max. Rating, V _{GS} = 0, T _A = 125°C (Note 2)
8	I _{DSS} Drain Current			100			100			100	nA	V _{DS} = 25V, V _{GS} = 0
9	I _{D(on)} ON-State Drain Current	1.0	2		1.0	2		1.0	2		A	V _{DS} = 25V, V _{GS} = 10V
10	V _{DS(on)} Drain-Source Saturation Voltage		0.3			0.3			0.4			V _{GS} = 5V, I _D = 0.1A
11			1.0	2.0		1.0	1.7		1.4	1.9		V _{GS} = 5V, I _D = 0.3A
12			1.0			1.0			1.3			V _{GS} = 10V, I _D = 0.5A
13			2.2	5.0		2.2	3.5		2.2	4.5		V _{GS} = 10V, I _D = 1.0A
14	g _m Forward Transconductance		250			250			250		mT	V _{DS} = 24V, I _D = 0.5A, f = 1KHz
15	C _{iss} Input Capacitance			50			50			50	pF	V _{GS} = 0, V _{DS} = 25V, f = 1.0 MHz
16	C _{rss} Reverse Transfer Capacitance			10			10			10		
17	C _{oss} Common-Source Output Capacitance			50			50			50		
18	t _{d(on)} Turn-ON Delay Time		2	5		2	5		2	5		
19	t _r Rise Time		2	5		2	5		2	5		(Note 2)
20	t _{d(off)} Turn-OFF Delay Time		2	5		2	5		2	5		
21	t _f Fall Time		2	5		2	5		2	5		

Note 1. Pulse test — 80μs pulse, 1% duty cycle.**Note 2.** Sample test.**THERMAL RESPONSE****POWER DISSIPATION vs CASE TEMPERATURE****DC SAFE OPERATING REGION
T_C = 25°C****BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE**