



VN750-E / VN750S-E VN750PT-E / VN750B5-E

HIGH SIDE DRIVER

Table 1. General Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN750-E VN750B5-E VN750S-E VN750PT	60 m Ω	6 A	36 V

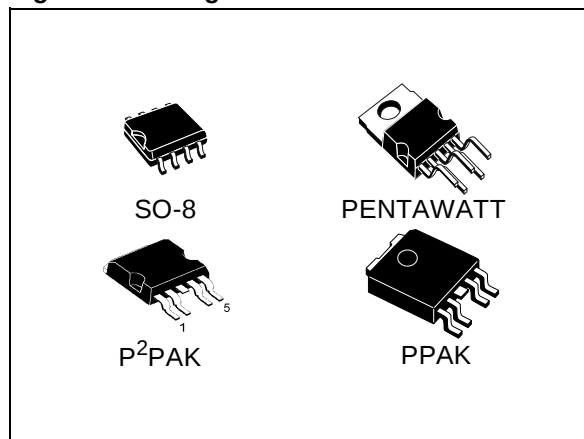
- CMOS COMPATIBLE INPUT
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

The VN750-E, VN750S-E, VN750PT-E, VN750B5-E are a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Figure 1. Package



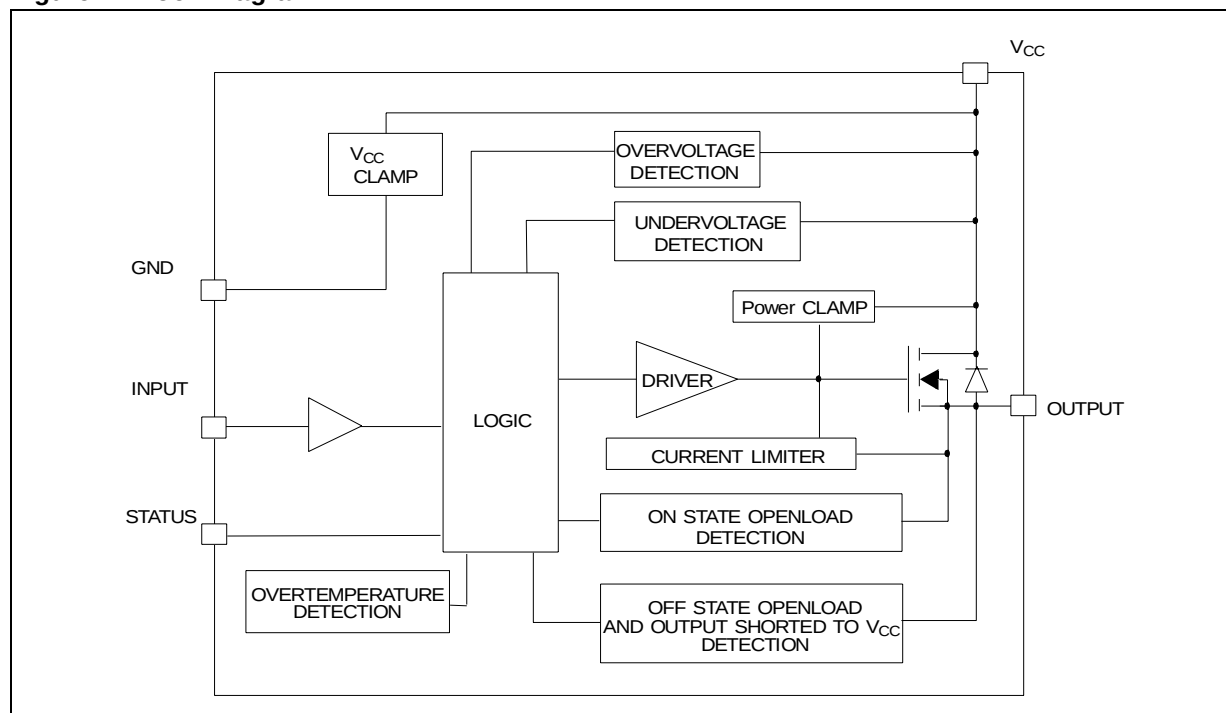
Active current limitation combined with thermal shutdown and automatic restart protect the device against overload.

The device detects open load condition both is on and off state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PENTAWATT	VN750-E	-
SO-8	VN750S-E	VN750STR-E
P ² PAK	VN750B5-E	VN750B5TR-E
PPAK	VN750PT-E	VN750PTTR-E

Note: (*) See application schematic at page 9.

VN750-E / VN750S-E / VN750PT-E / VN750B5-E**Figure 2. Block Diagram****Table 3. Absolute Maximum Ratings**

Symbol	Parameter	Value				Unit
		SO-8	PENTAWATT	P ² PAK	PPAK	
V _{CC}	DC Supply Voltage		41			V
- V _{CC}	Reverse DC Supply Voltage		- 0.3			V
- I _{gnd}	DC Reverse Ground Pin Current		- 200			mA
I _{OUT}	DC Output Current		Internally Limited			A
- I _{OUT}	Reverse DC Output Current		- 6			A
I _{IN}	DC Input Current		+/- 10			mA
I _{STAT}	DC Status Current		+/- 10			mA
V _{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)					
	- INPUT		4000			V
	- STATUS		4000			V
	- OUTPUT		5000			V
	- V _{CC}		5000			V
E _{MAX}	Maximum Switching Energy (L=1.8mH; R _L =0Ω; V _{bat} =13.5V; T _{jstart} =150°C; I _L =9A)	100				mJ
E _{MAX}	Maximum Switching Energy (L=2.46mH; R _L =0Ω; V _{bat} =13.5V; T _{jstart} =150°C; I _L =9A)			138	138	mJ
P _{tot}	Power Dissipation T _C =25°C	4.2	60	60	60	W
T _j	Junction Operating Temperature		Internally Limited			°C
T _C	Case Operating Temperature		- 40 to 150			°C
T _{stg}	Storage Temperature		- 55 to 150			°C

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Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins

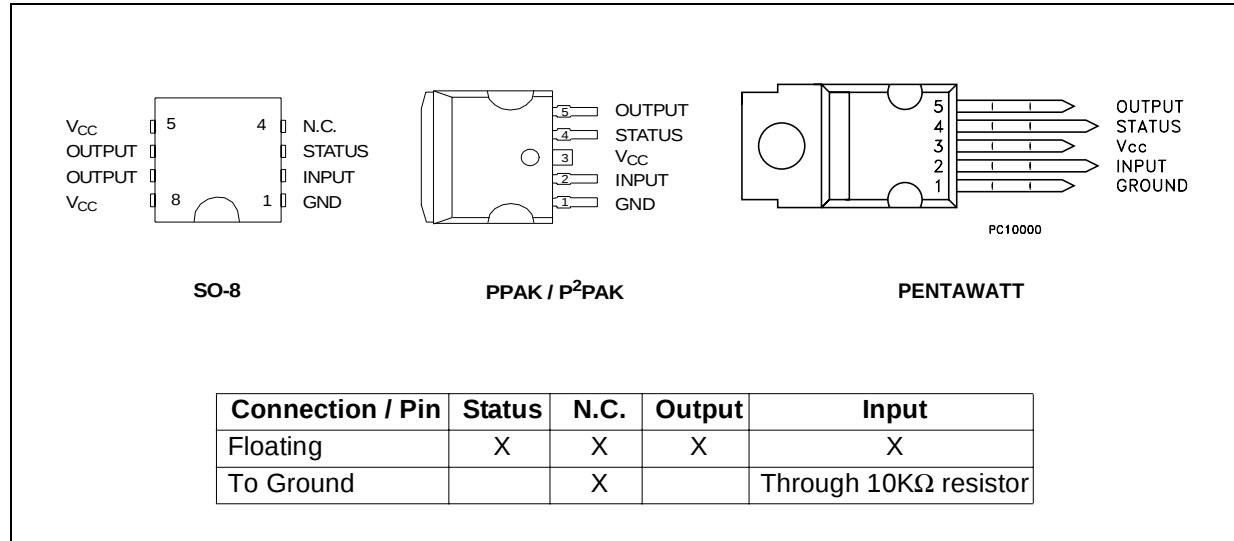


Figure 4. Current and Voltage Conventions

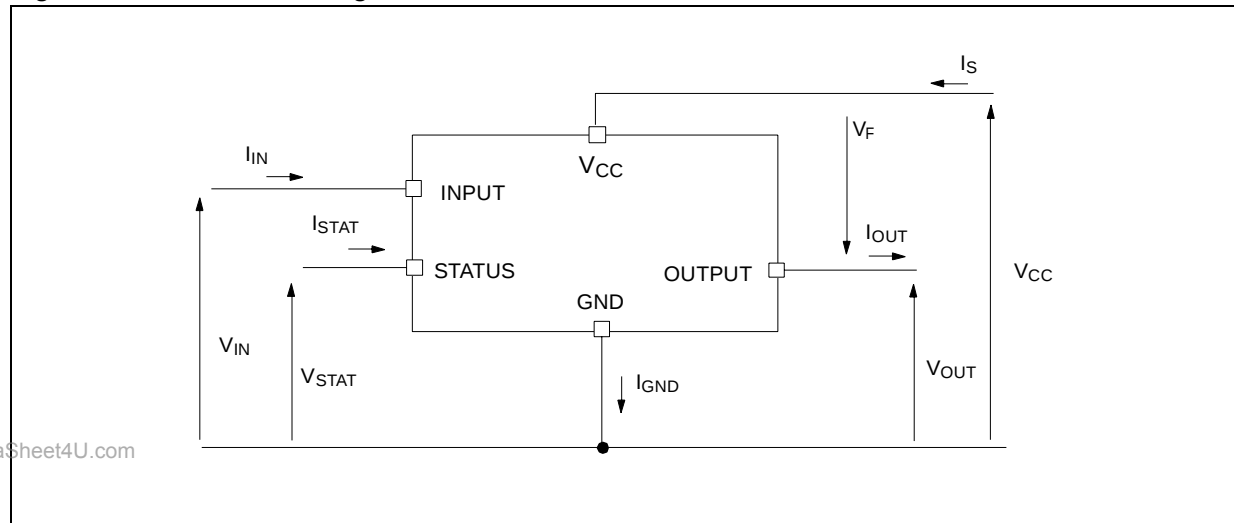


Table 4. Thermal Data

Symbol	Parameter		Value				Unit
			SO-8	PENTAWATT	P²PAK	PPAK	
R _{thj-case}	Thermal Resistance Junction-case	Max	-	2.1	2.1	2.1	°C/W
R _{thj-lead}	Thermal Resistance Junction-lead	Max	30	-	-	-	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	93 ⁽¹⁾	62.1	52.1 ⁽³⁾	77.1 ⁽³⁾	°C/W
			82 ⁽²⁾	62.1	37 ⁽⁴⁾	44 ⁽⁴⁾	°C/W

⁽¹⁾ When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

⁽²⁾ When mounted on a standard single-sided FR-4 board with 2cm² of Cu (at least 35μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

⁽³⁾ When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick). Horizontal mounting and no artificial air flow.

⁽⁴⁾ When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35μm thick). Horizontal mounting and no artificial air flow.

VN750-E / VN750S-E / VN750PT-E / VN750B5-E**ELECTRICAL CHARACTERISTICS** (8V<V_{CC}<36V; -40°C<T_j<150°C unless otherwise specified)**Table 5. Power**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating Supply Voltage		5.5	13	36	V
V _{USD}	Undervoltage Shut-down		3	4	5.5	V
V _{USDhyst}	Undervoltage Shut-down Hysteresis			0.5		V
V _{OV}	Overvoltage Shut-down		36			V
R _{ON}	On State Resistance	I _{OUT} =2A; T _j =25°C; V _{CC} >8V I _{OUT} =2A; V _{CC} >8V		(#)	60 120	mΩ mΩ
I _S	Supply Current	Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C On State; V _{CC} =13V; V _{IN} =5V; I _{OUT} =0A		10 10 2	25 20 3.5	μA μA mA
I _{L(off1)}	Off State Output Current	V _{IN} =V _{OUT} =0V	0	(#)	50	μA
I _{L(off2)}	Off State Output Current	V _{IN} =0V; V _{OUT} =3.5V	-75		0	μA
I _{L(off3)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =125°C			5	μA
I _{L(off4)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =25°C			3	μA

Table 6. Switching (V_{CC} =13V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on Delay Time	R _L =6.5Ω from V _{IN} rising edge to V _{OUT} =1.3V		40		μs
t _{d(off)}	Turn-off Delay Time	R _L =6.5Ω from V _{IN} falling edge to V _{OUT} =11.7V		30		μs
dV _{OUT} /dt _(on)	Turn-on Voltage Slope	R _L =6.5Ω from V _{OUT} =1.3V to V _{OUT} =10.4V		(#)		V/μs
dV _{OUT} /dt _(off)	Turn-off Voltage Slope	R _L =6.5Ω from V _{OUT} =11.7V to V _{OUT} =1.3V		(#)		V/μs

Table 7. Input Pin

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{IL}	Input Low Level			(#)	1.25	V
I _{IL}	Low Level Input Current	V _{IN} =1.25V	1	(#)		μA
V _{IH}	Input High Level		3.25	(#)		V
I _{IH}	High Level Input Current	V _{IN} =3.25V		(#)	10	μA
V _{hyst}	Input Hysteresis Voltage		0.5	(#)		V
V _{ICL}	Input Clamp Voltage	I _{IN} =1mA I _{IN} =-1mA	6	6.8 -0.7	8	V V

Note: (#) See relative diagram

VN750-E / VN750S-E / VN750PT-E / VN750B5-E**ELECTRICAL CHARACTERISTICS** (continued)**Table 8. V_{CC} - Output Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _F	Forward on Voltage	-I _{OUT} =1.3A; T _J =150°C			0.6	V

Table 9. Status Pin

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{STAT}	Status Low Output Voltage	I _{STAT} =1.6mA		(#)	0.5	V
I _{LSTAT}	Status Leakage Current	Normal Operation; V _{STAT} =5V		(#)	10	μA
C _{STAT}	Status Pin Input Capacitance	Normal Operation; V _{STAT} =5V			100	pF
V _{SCL}	Status Clamp Voltage	I _{STAT} =1mA I _{STAT} =-1mA	6	6.8 -0.7	8	V V

Table 10. Protections (see note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T _{TSD}	Shut-down Temperature		150	175	200	°C
T _R	Reset Temperature		135			°C
T _{hyst}	Thermal Hysteresis		7	15		°C
t _{SDL}	Status delay in overload condition	T _J >T _{Jsh}			20	μs
I _{lim}	Current limitation	9V<V _{CC} <36V 5V<V _{CC} <36V	6	9	15 15	A A
V _{demag}	Turn-off Output Clamp Voltage	I _{OUT} =2A; V _{IN} =0V; L=6mH	V _{CC} -41	V _{CC} -48	V _{CC} -55	V

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 11. Openload Detection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _{OL}	Openload ON State Detection Threshold	V _{IN} =5V	50	(#)	200	mA
t _{DOL(on)}	Openload ON State Detection Delay	I _{OUT} =0A			200	μs
V _{OL}	Openload OFF State Voltage Detection Threshold	V _{IN} =0V	1.5	(#)	3.5	V
t _{DOL(off)}	Openload Detection Delay at Turn Off				1000	μs

Note: (#) See relative diagram

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Figure 5.

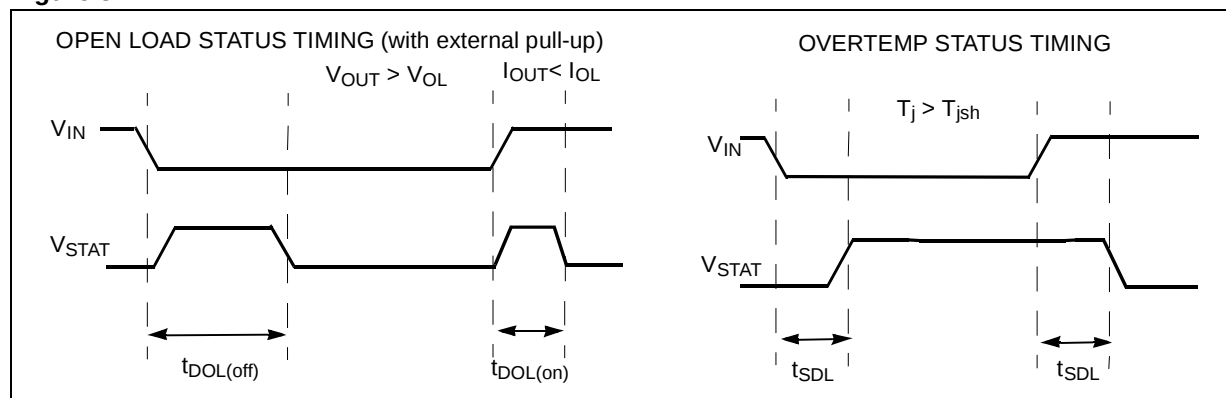
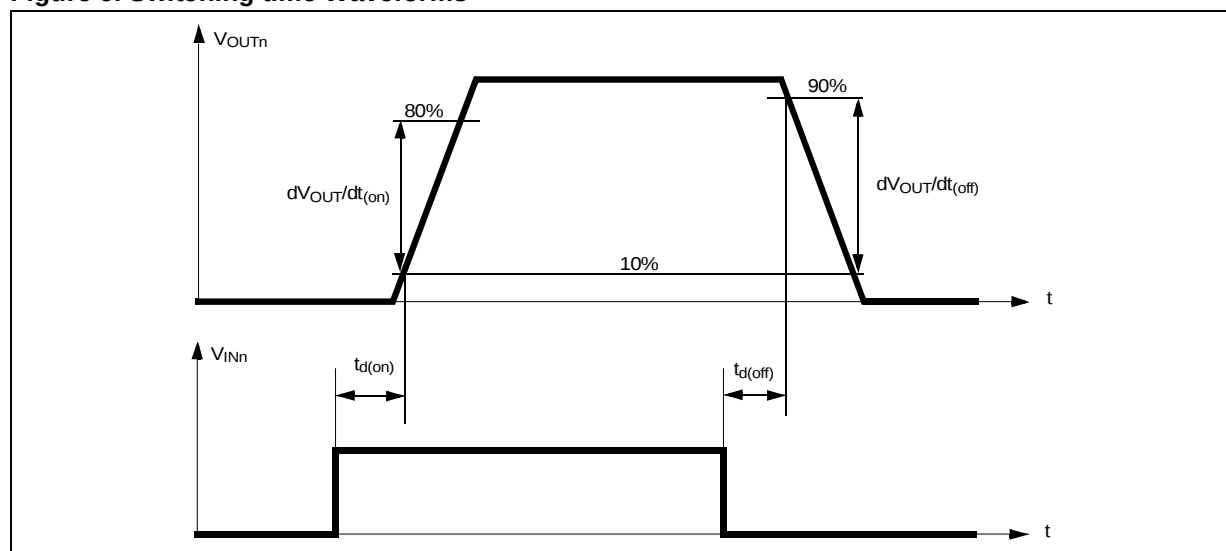


Table 12. Truth Table

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > V_{OL}	L H	H H	L H
Output Current < I_{OL}	L H	L H	H L

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Figure 6. Switching time Waveforms



VN750-E / VN750S-E / VN750PT-E / VN750B5-E**Table 13. Electrical Transient Requirements On V_{CC} Pin**

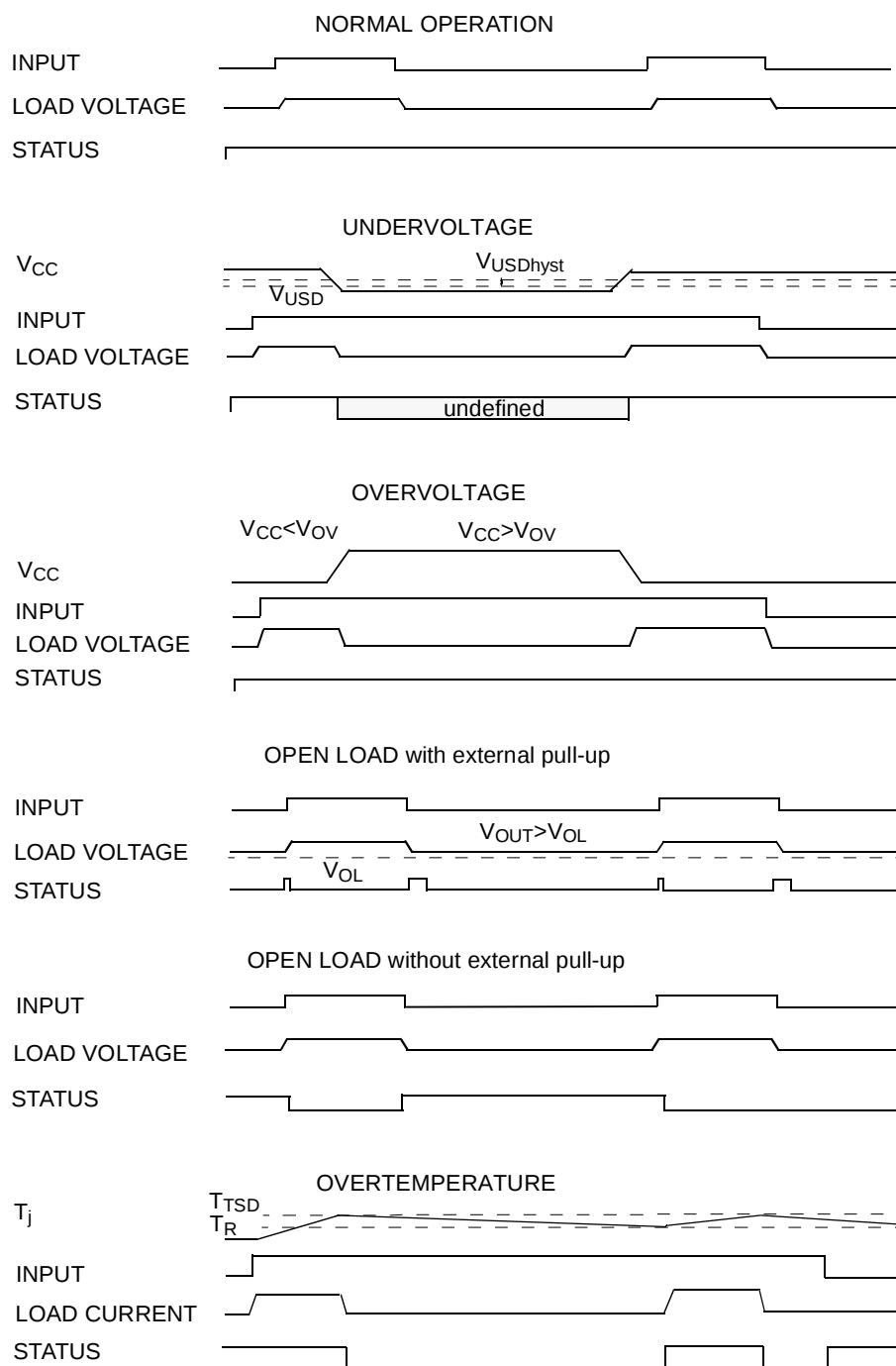
ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

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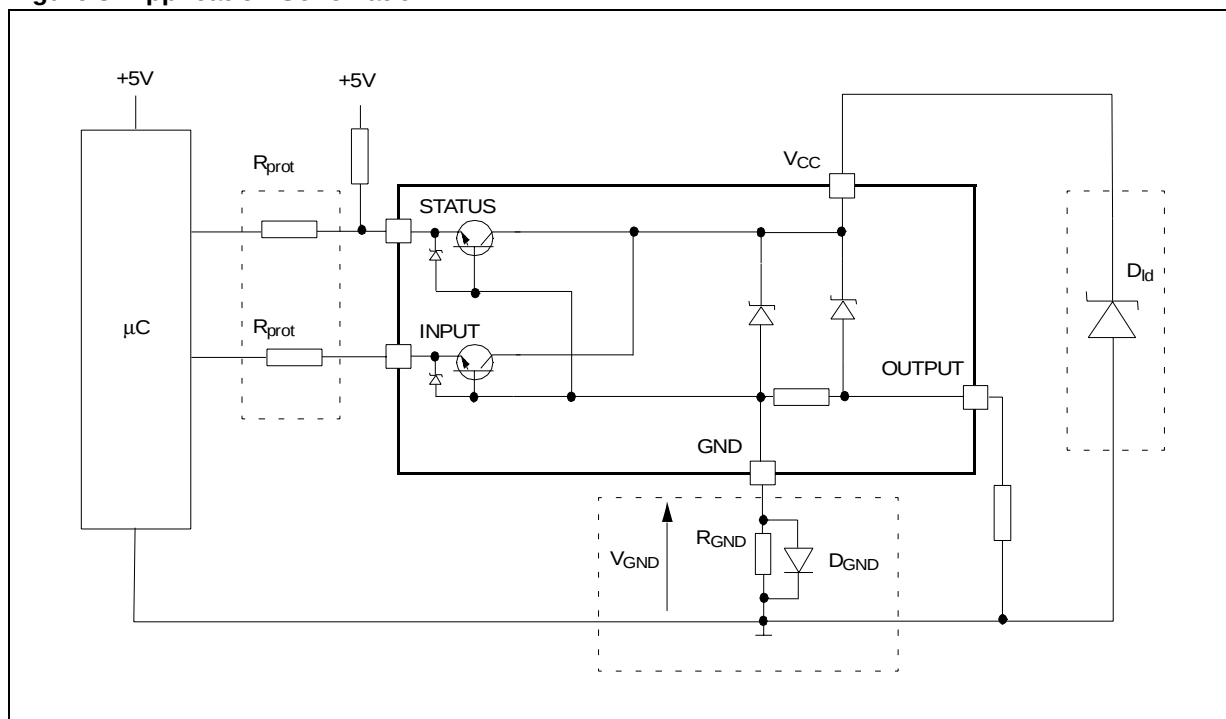
Figure 7. Waveforms



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VN750-E / VN750S-E / VN750PT-E / VN750B5-E

Figure 8. Application Schematic

**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND}=1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of

the ground network will produce a shift ($\approx 600\text{mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$
 $5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$.

Recommended R_{prot} value is $10\text{k}\Omega$.

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OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

- 1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition

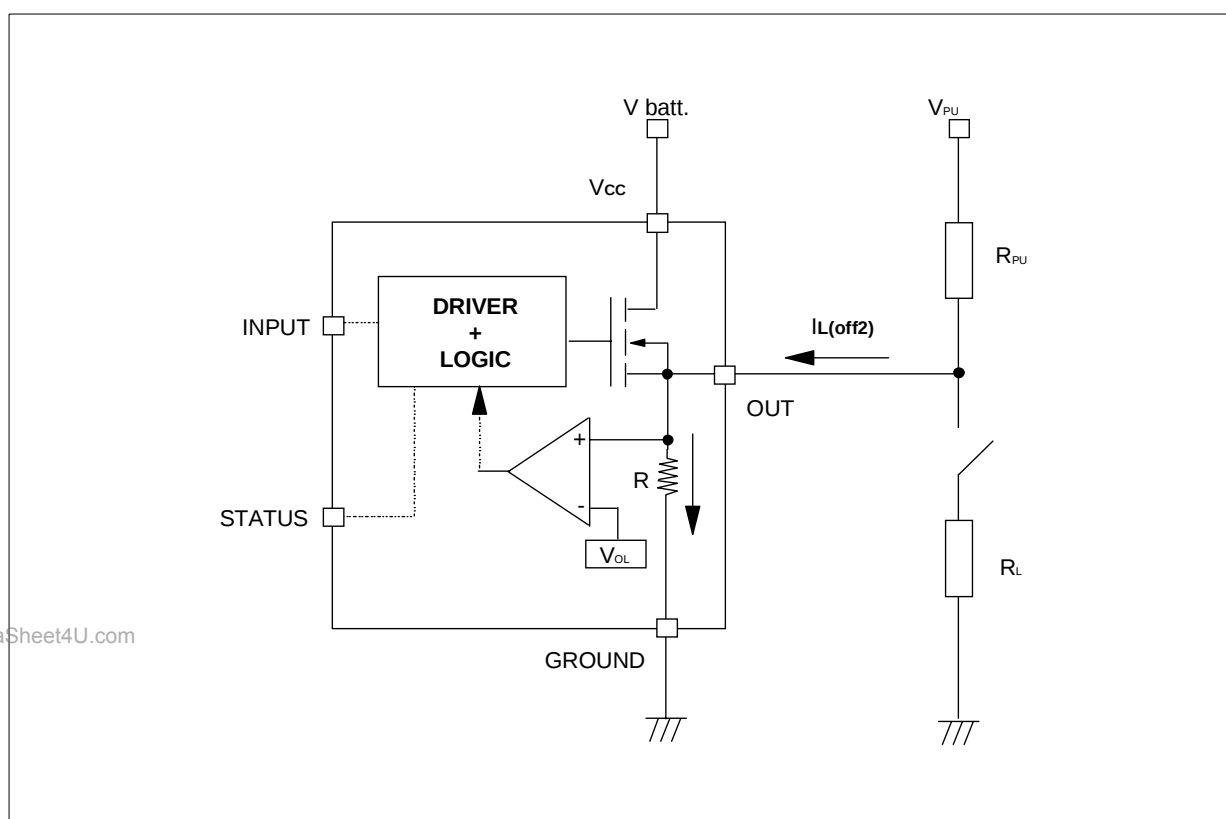
$$V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}.$$

- 2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{S(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

The values of V_{OLmin} , V_{OLmax} and $I_{L(off2)}$ are available in the Electrical Characteristics section.

Figure 9. Open Load detection in off state



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Figure 10. Off State Output Current

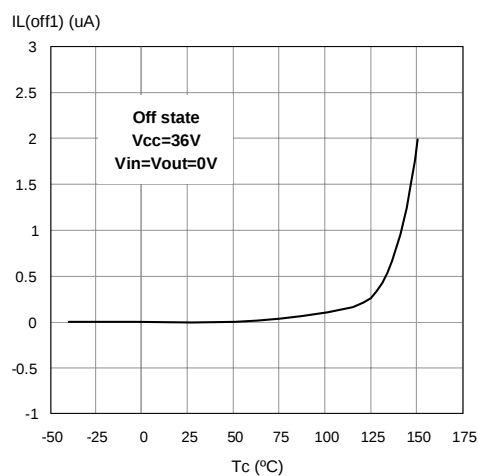


Figure 11. High Level Input Current

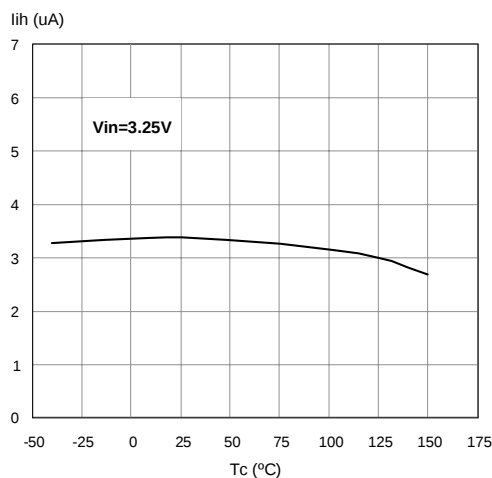


Figure 12. Input Clamp Voltage

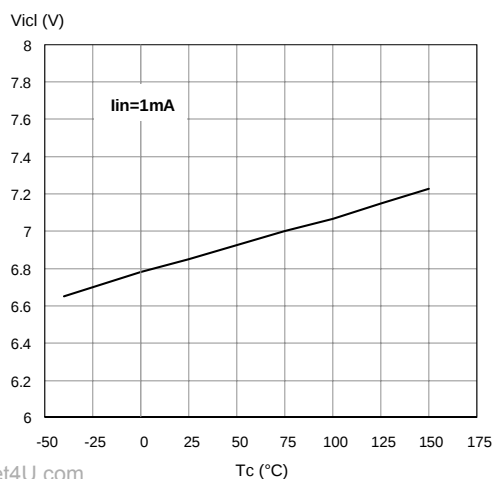


Figure 14. Status Leakage Current

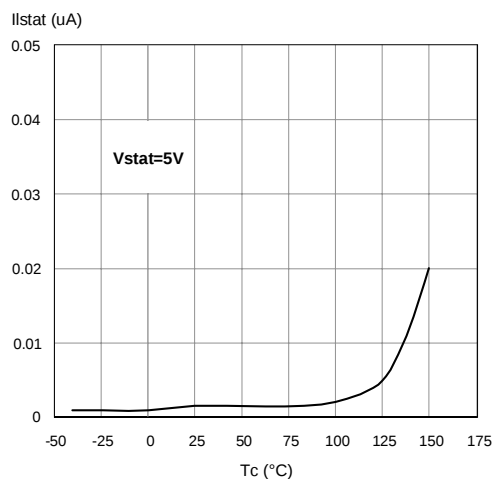


Figure 13. Status Low Output Voltage

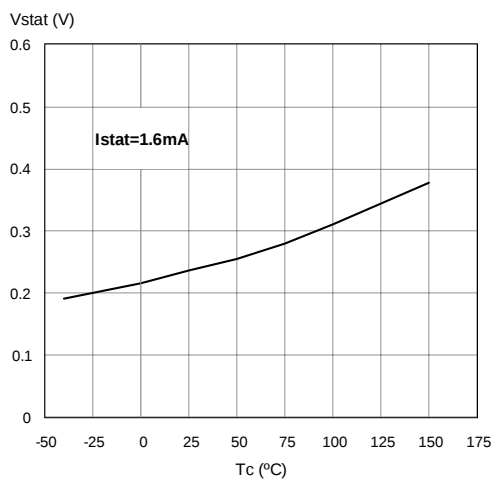
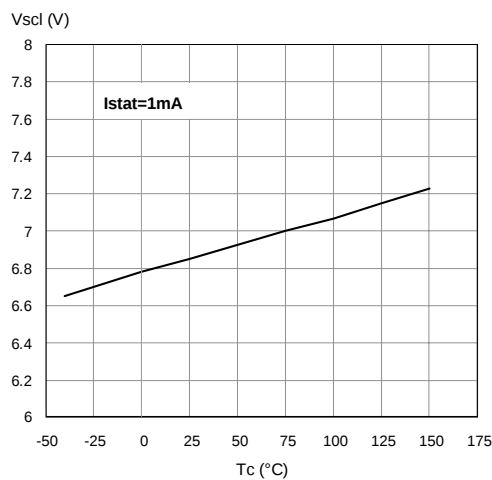
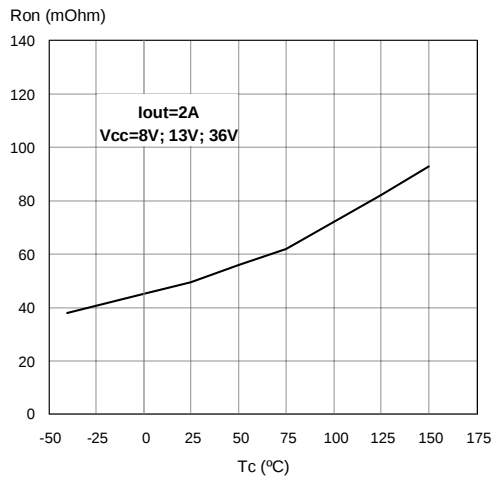
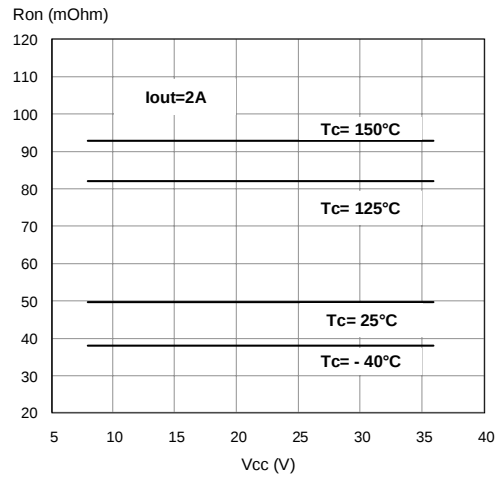
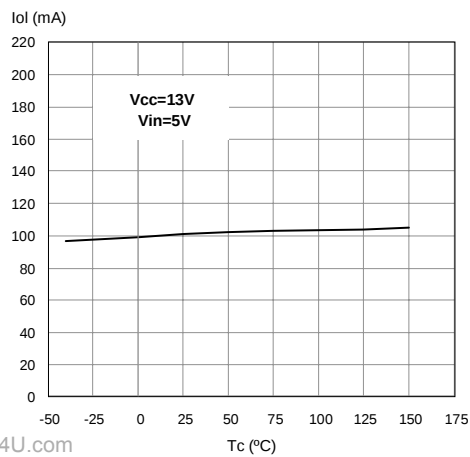
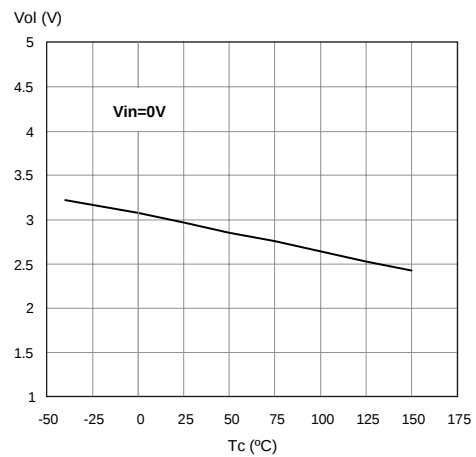
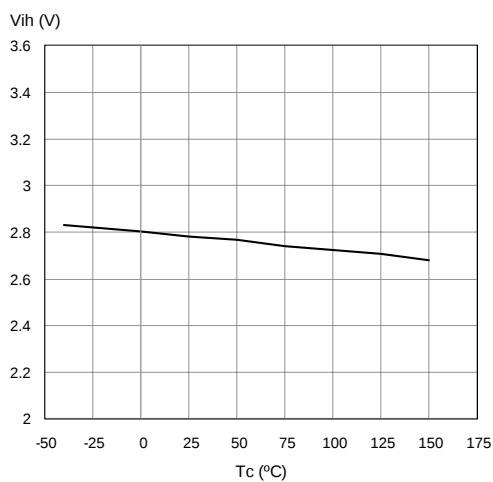
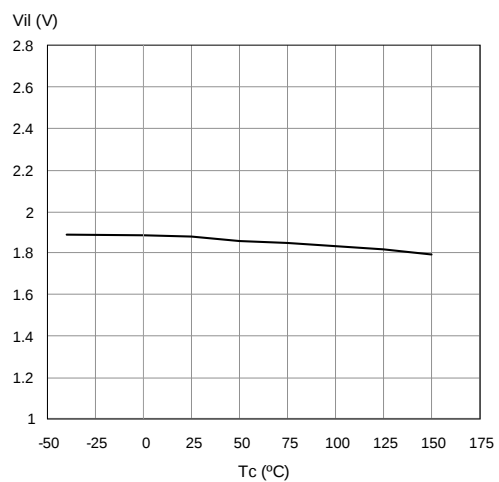


Figure 15. Status Clamp Voltage



VN750-E / VN750S-E / VN750PT-E / VN750B5-E**Figure 16. On State Resistance Vs T_{case}** **Figure 17. On State Resistance Vs V_{CC}** **Figure 18. Openload On State Detection Threshold****Figure 20. Openload Off State Voltage Detection Threshold****Figure 19. Input High Level****Figure 21. Input Low Level**

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Figure 22. Turn-on Voltage Slope

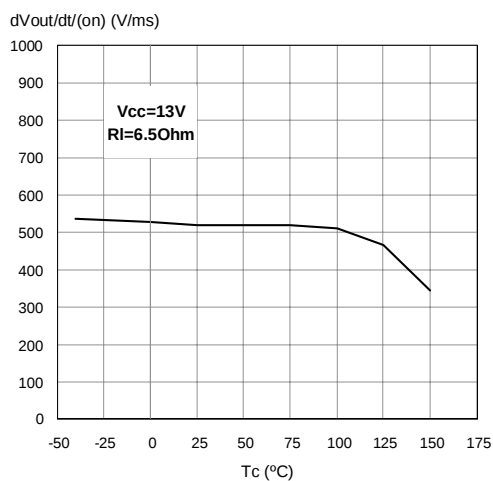


Figure 25. Turn-off Voltage Slope

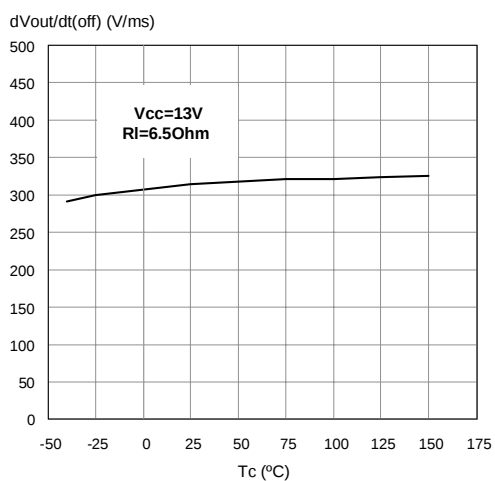
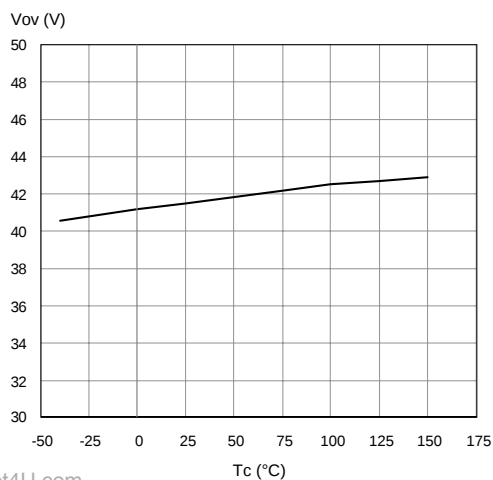
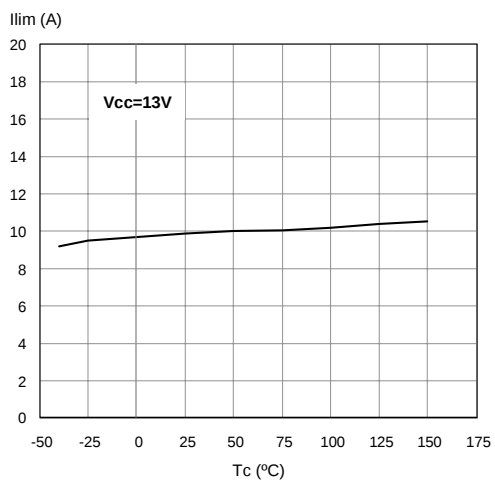
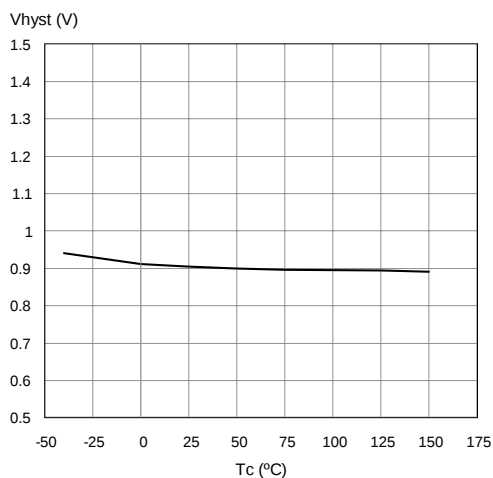


Figure 23. Overvoltage Shutdown

Figure 26. I_{LIM} Vs T_{case}

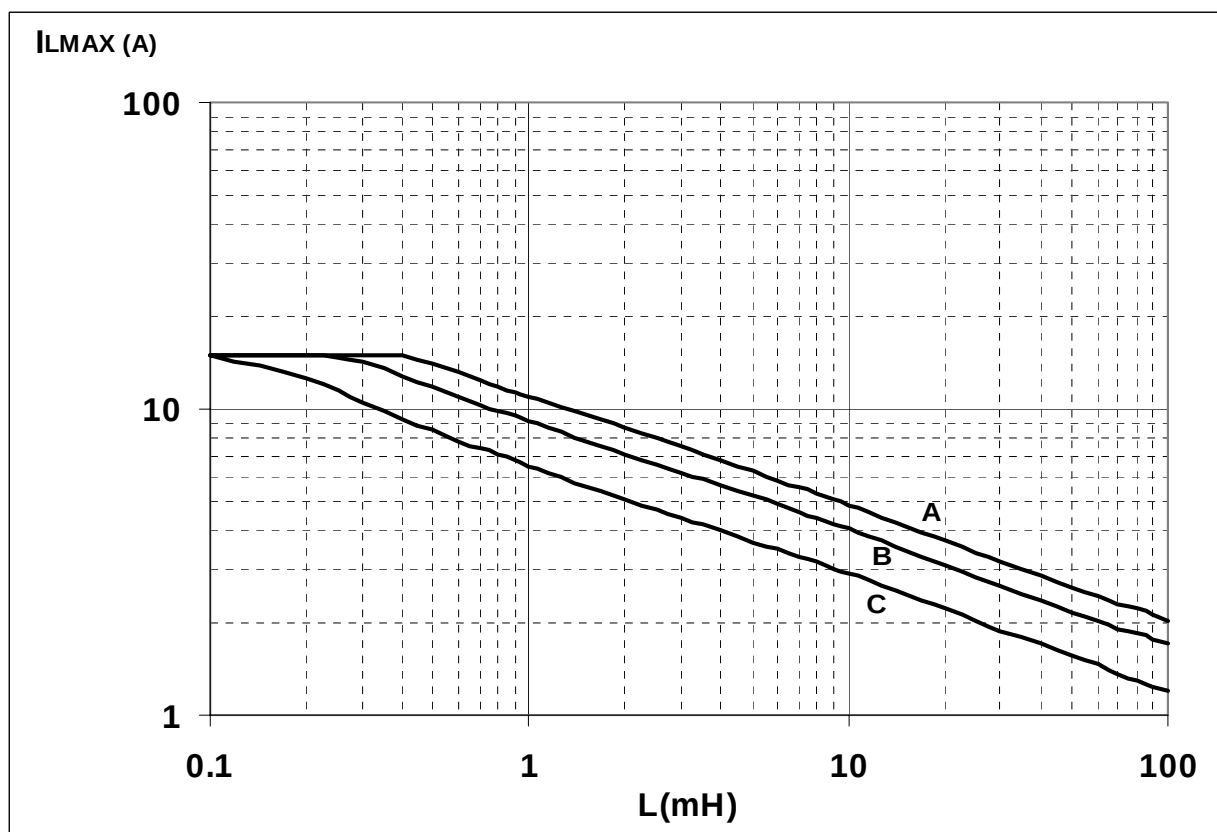
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Figure 24. Input Hysteresis Voltage

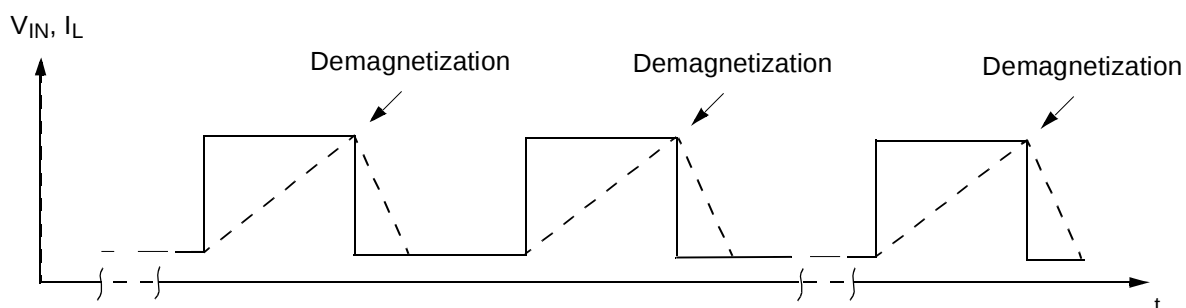


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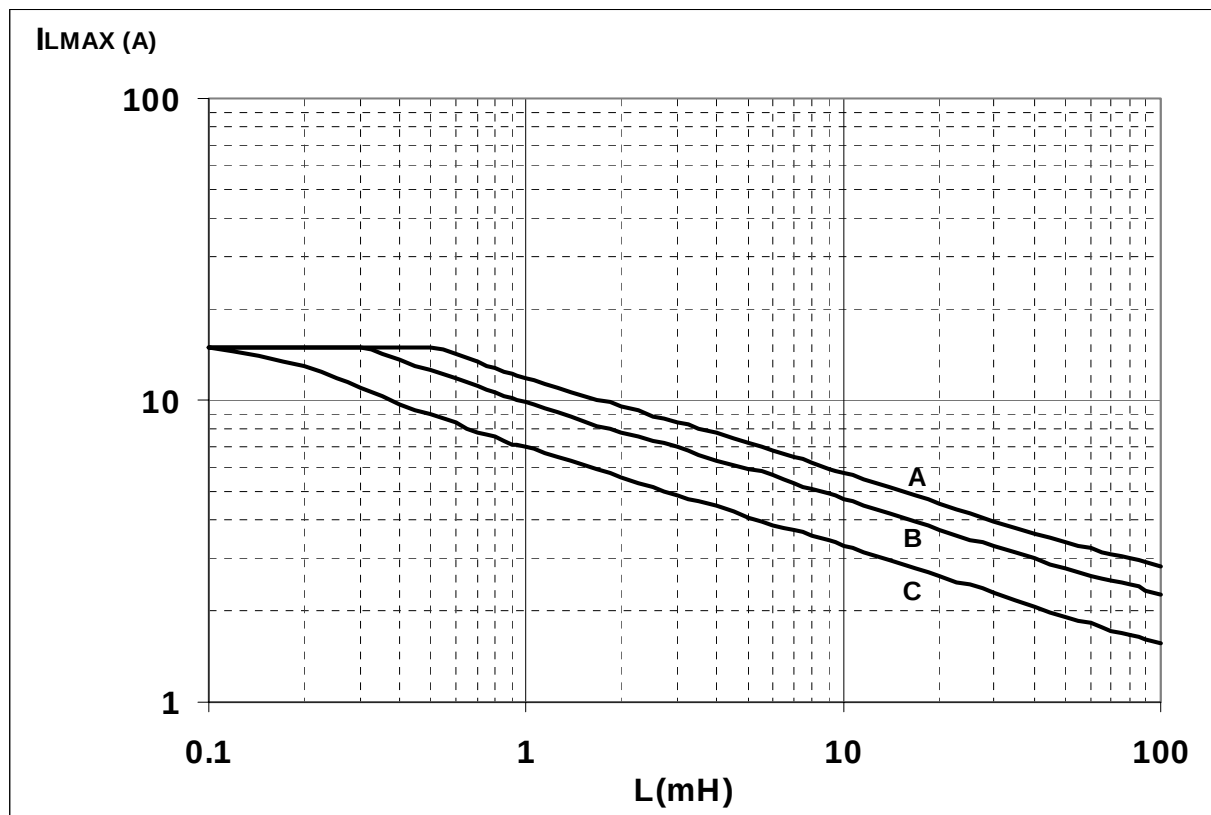
Figure 27. SO-8 Maximum turn off current versus load inductance

A = Single Pulse at $T_{Jstart}=150^{\circ}C$ B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$ C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$ Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions: $V_{CC}=13.5V$ 

VN750-E / VN750S-E / VN750PT-E / VN750B5-E

Figure 28. PPAK, P²PAK Maximum turn off current versus load inductance

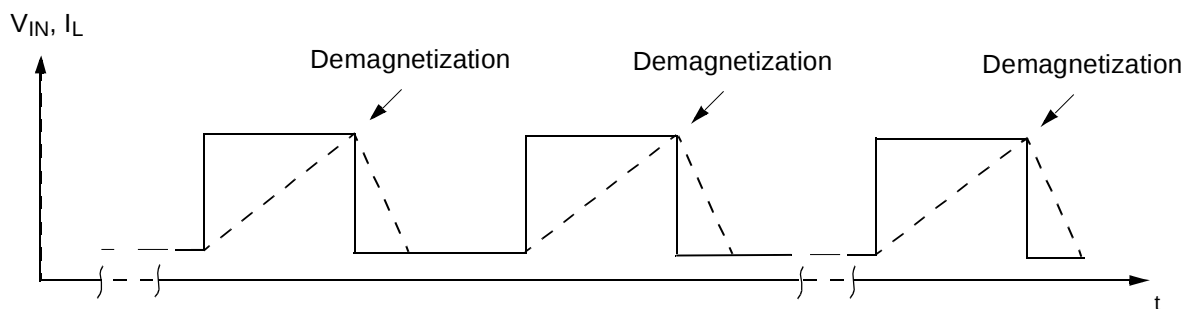
A = Single Pulse at $T_{Jstart}=150^{\circ}\text{C}$
 B= Repetitive pulse at $T_{Jstart}=100^{\circ}\text{C}$
 C= Repetitive Pulse at $T_{Jstart}=125^{\circ}\text{C}$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

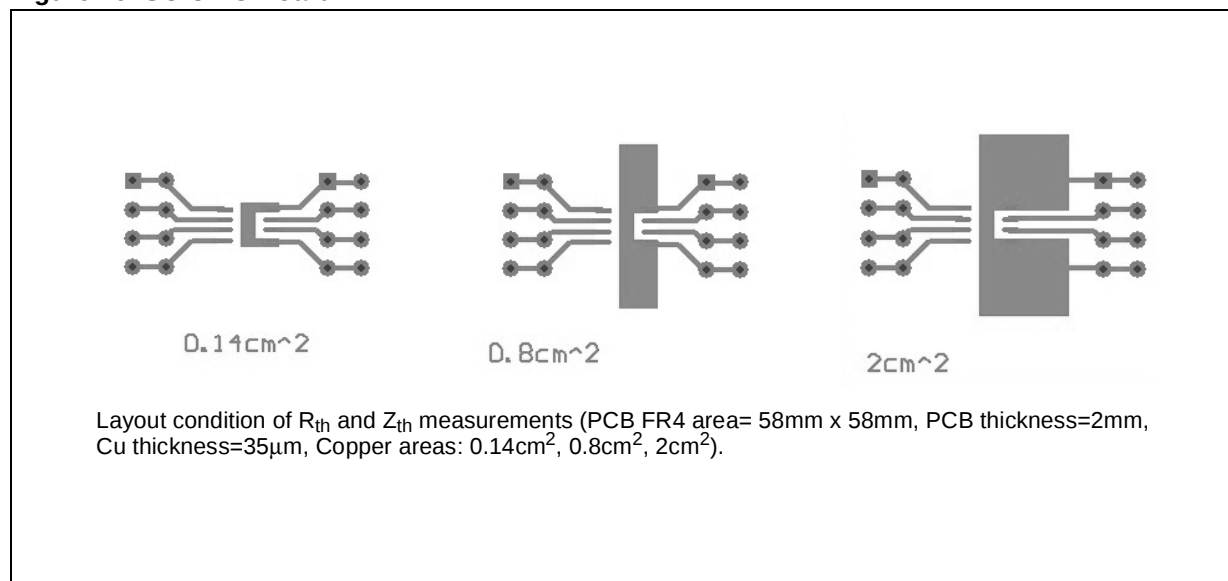
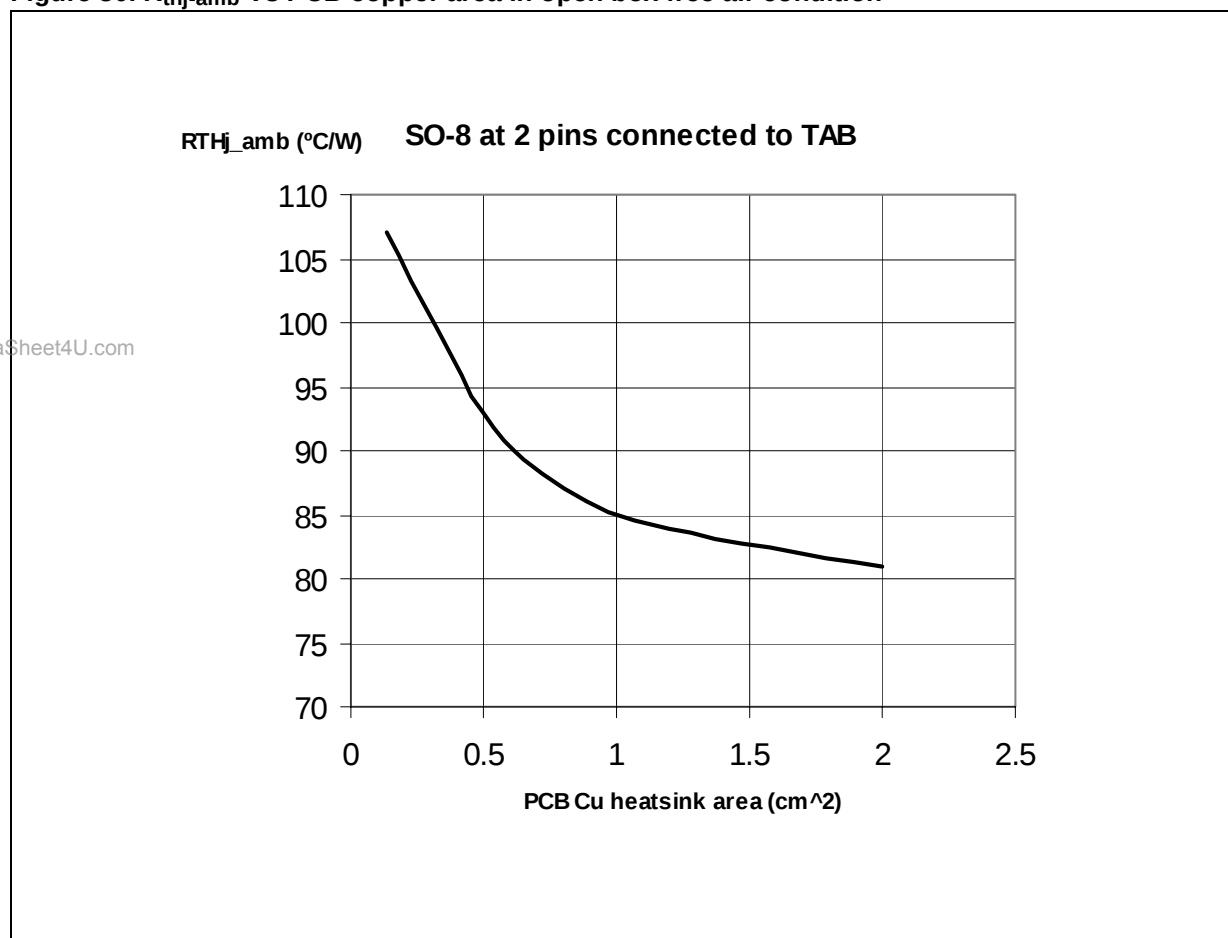
$V_{CC}=13.5\text{V}$



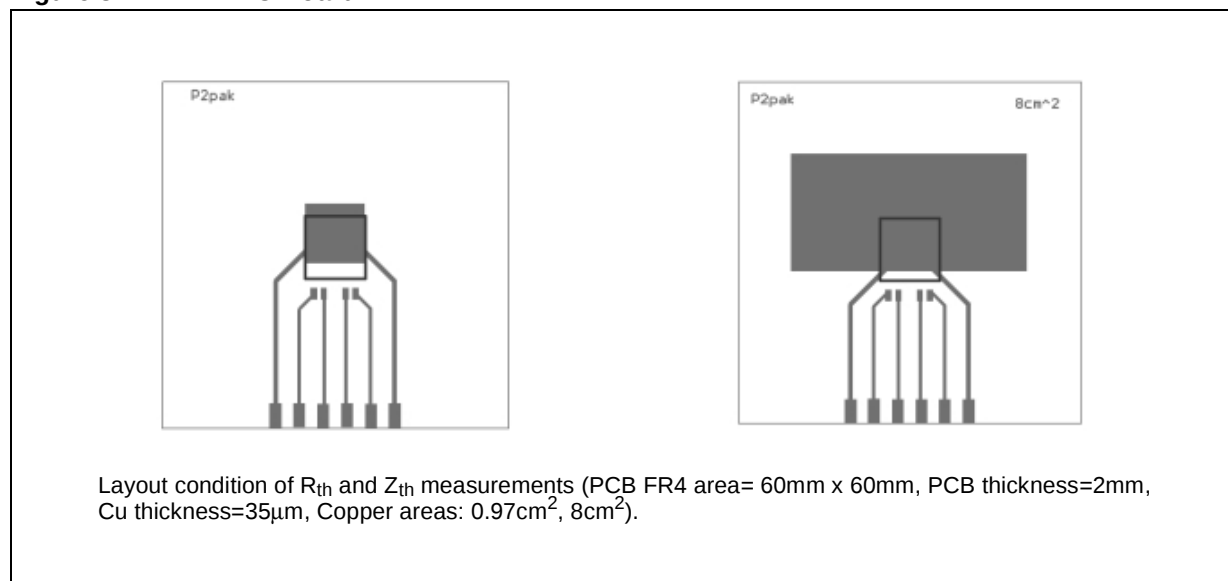
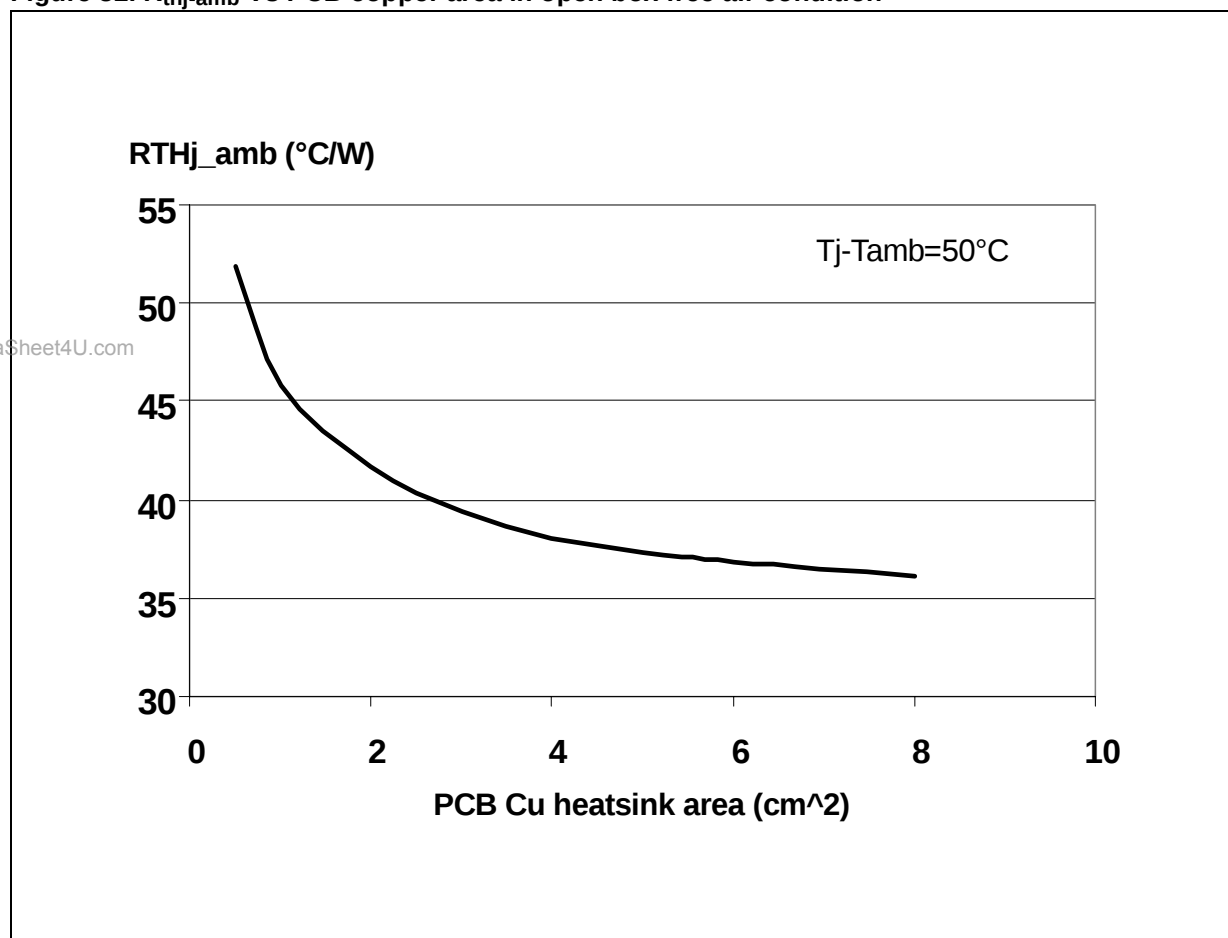
VN750-E / VN750S-E / VN750PT-E / VN750B5-E

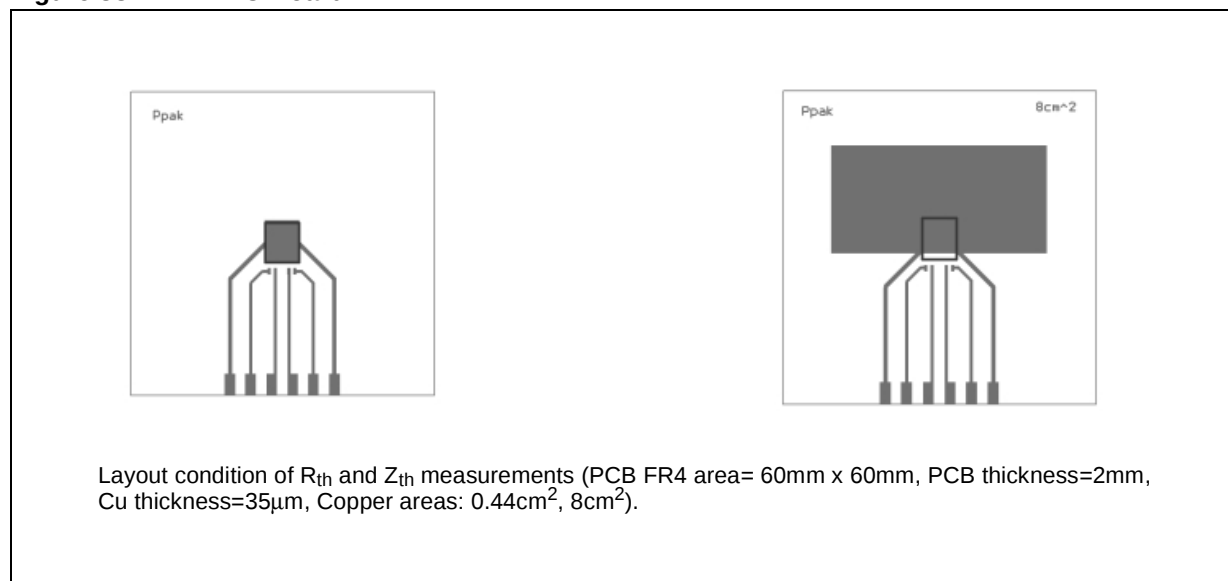
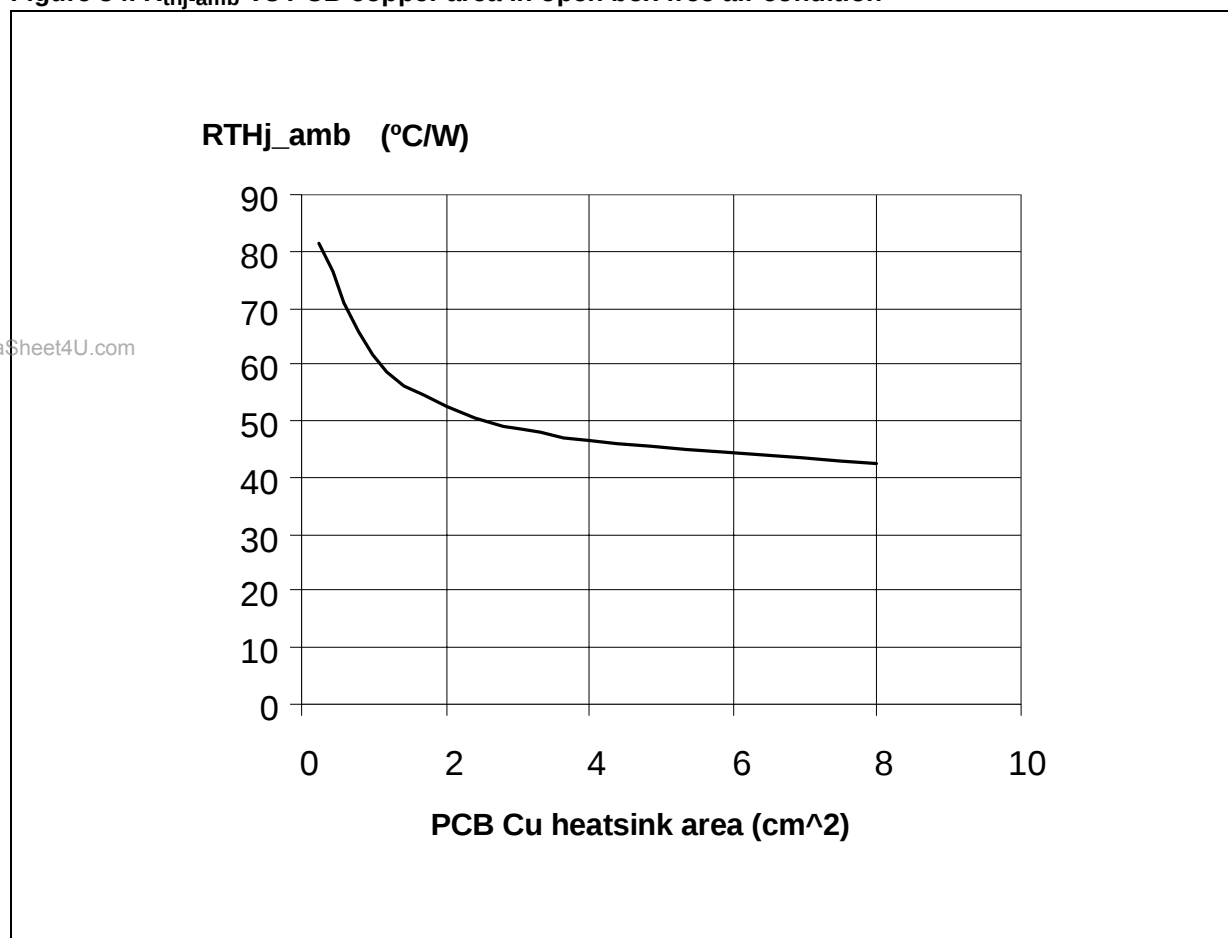
SO-8 Thermal Data

Figure 29. SO-8 PC Board

Figure 30. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

VN750-E / VN750S-E / VN750PT-E / VN750B5-E

P²PAK Thermal DataFigure 31. P²PAK PC BoardFigure 32. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

VN750-E / VN750S-E / VN750PT-E / VN750B5-E**PPAK Thermal Data****Figure 33. PPAK PC Board****Figure 34. $R_{thj-amb}$ Vs PCB copper area in open box free air condition**

VN750-E / VN750S-E / VN750PT-E / VN750B5-E

Figure 35. SO-8 Thermal Impedance Junction Ambient Single Pulse

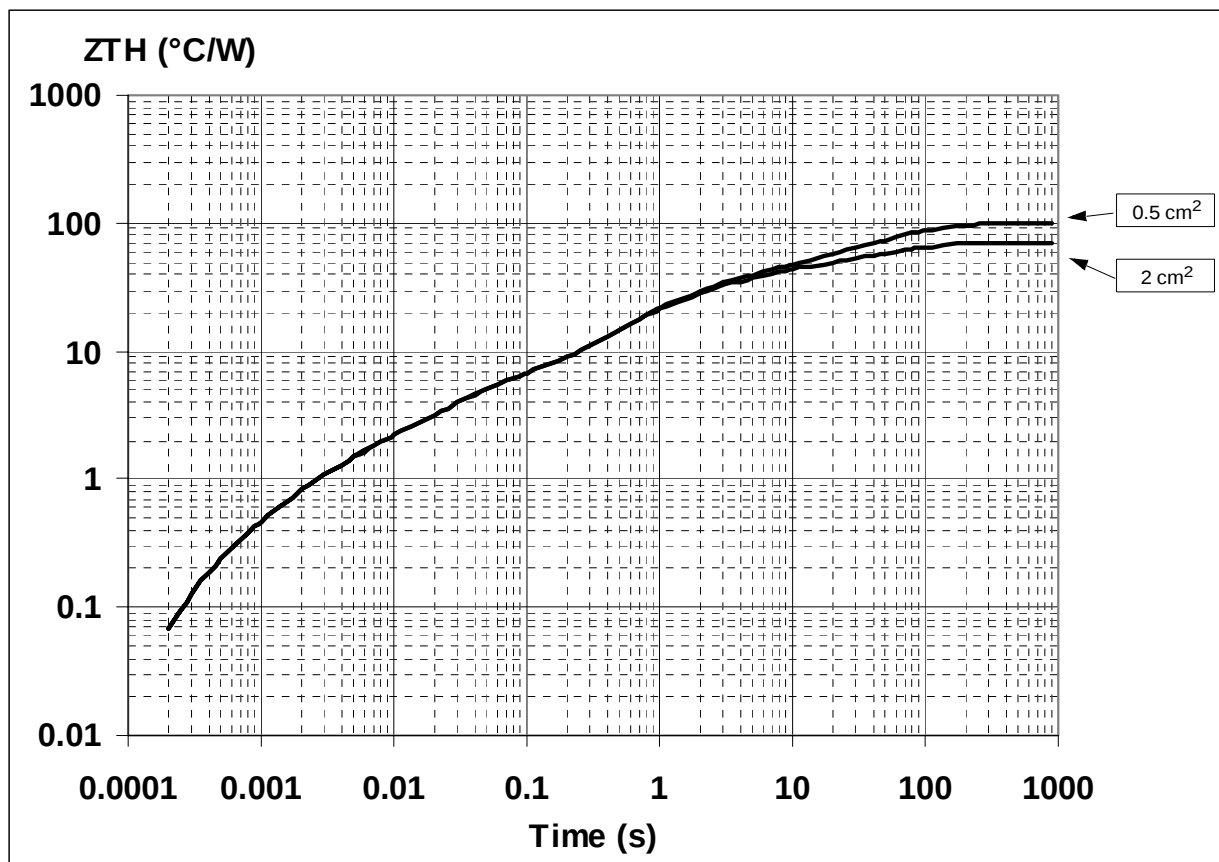
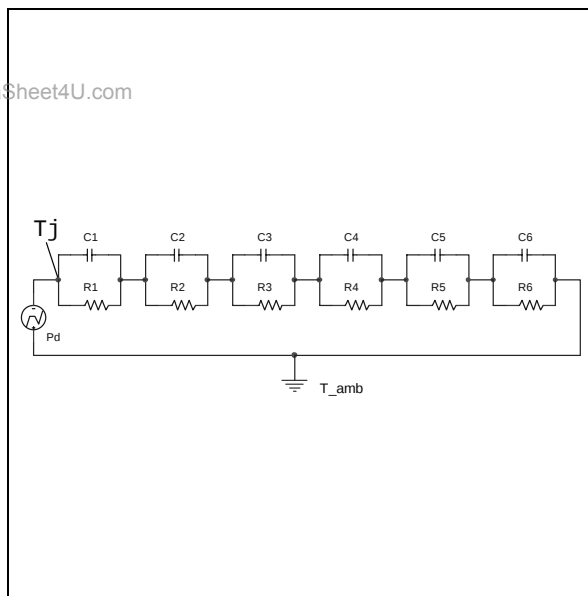


Figure 36. Thermal fitting model of a single channel HSD in SO-8



Pulse calculation formula

$$T_{H\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Table 14. Thermal Parameter

Area/island (cm ²)	0.5	2
R1 (°C/W)	0.05	
R2 (°C/W)	0.8	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.006	
C2 (W.s/°C)	2.60E-03	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

VN750-E / VN750S-E / VN750PT-E / VN750B5-E

Figure 37. PPAK Thermal Impedance Junction Ambient Single Pulse

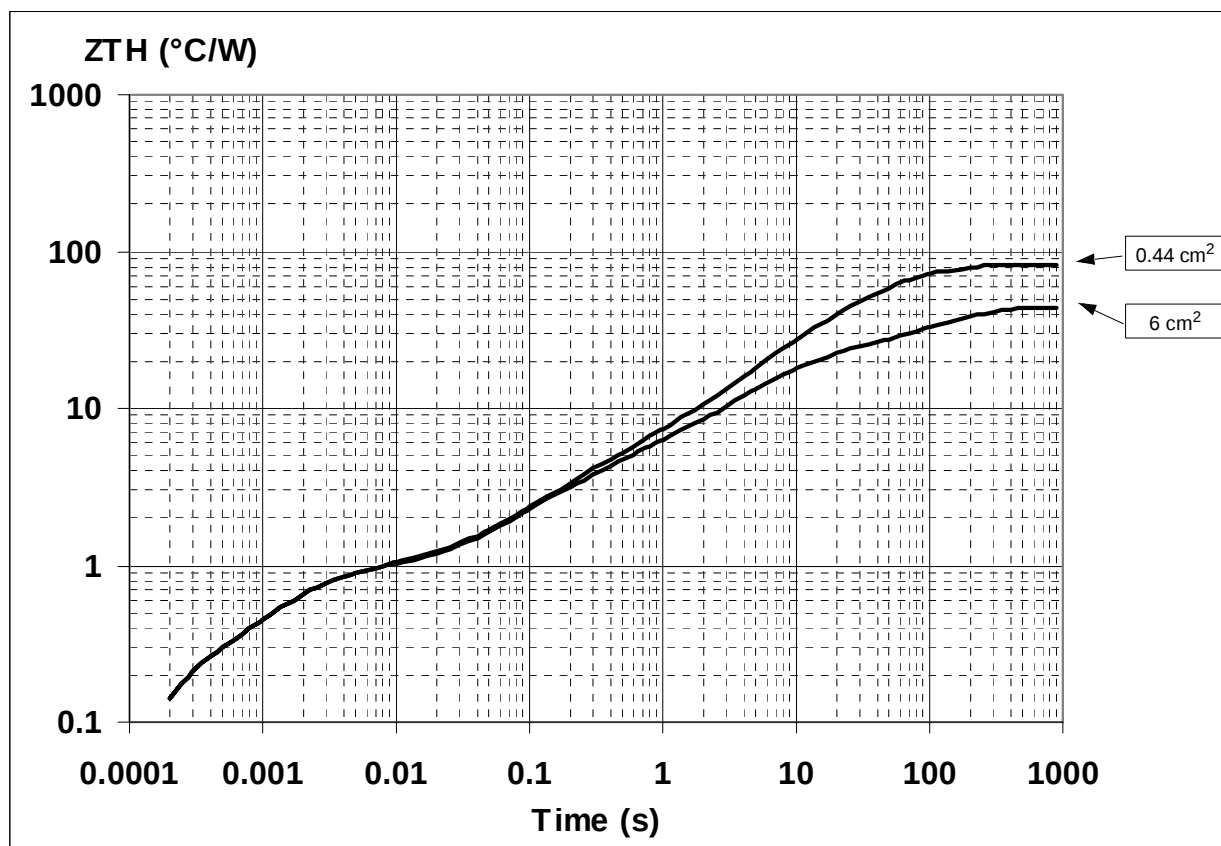
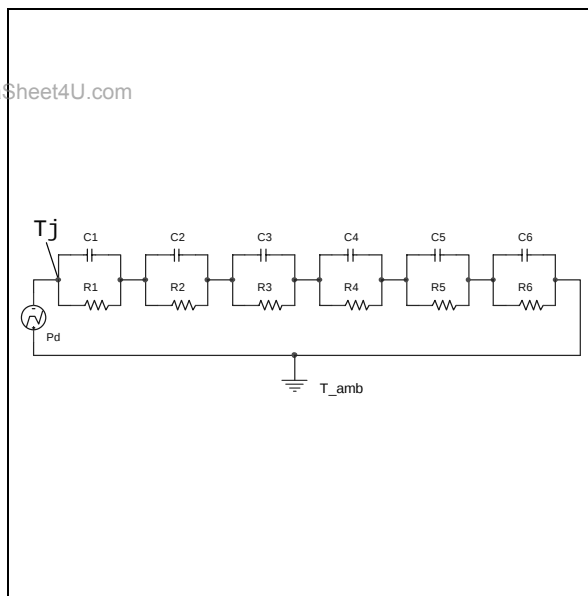


Figure 38. Thermal fitting model of a single channel HSD in PPAK



Pulse calculation formula

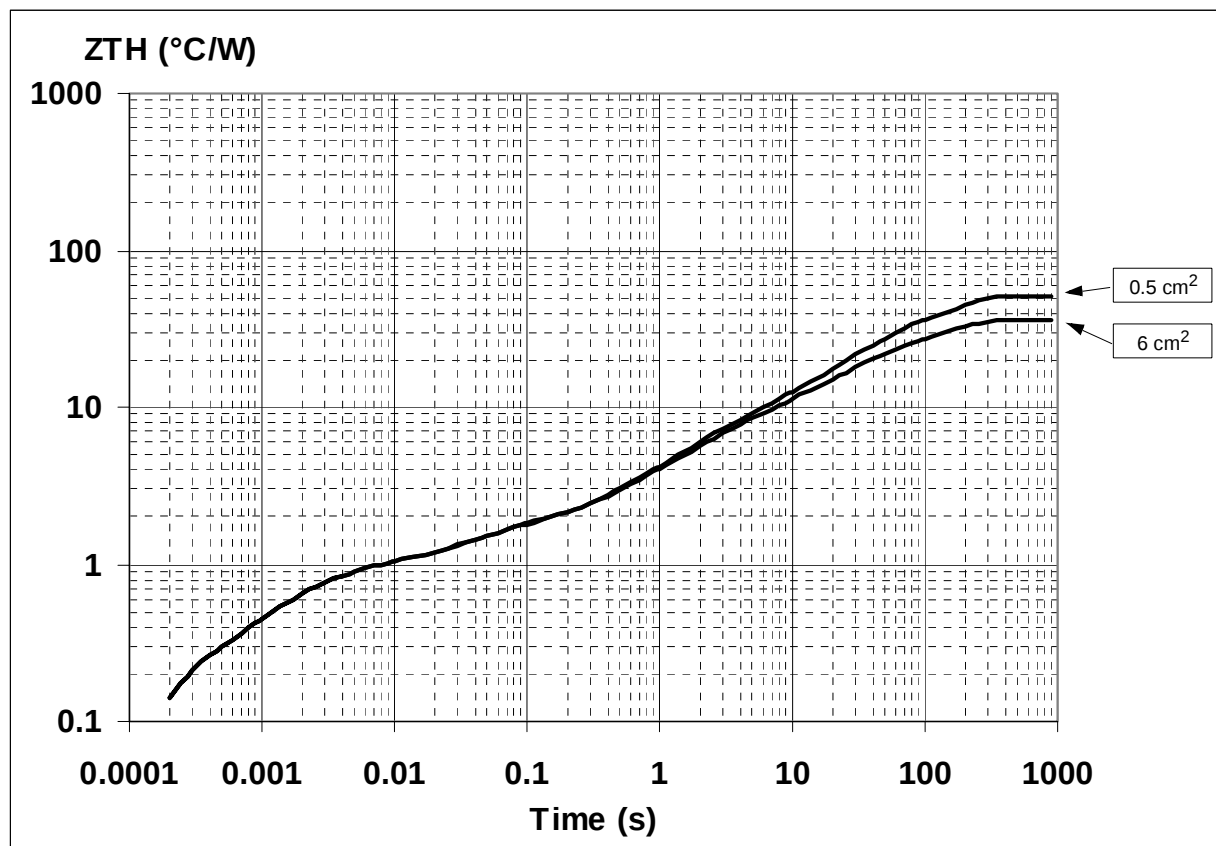
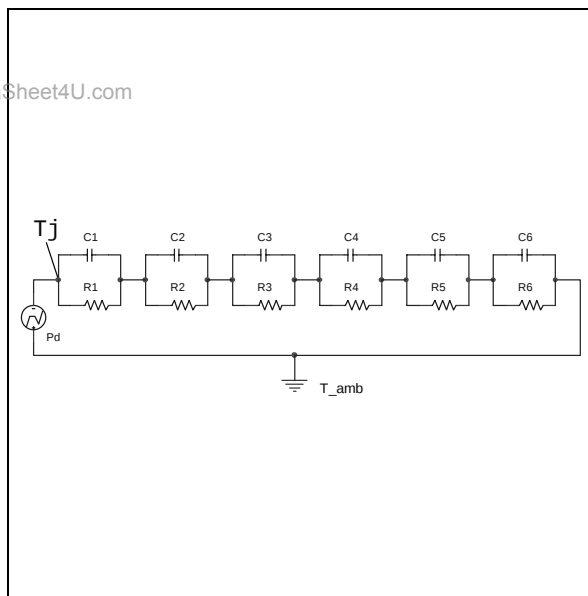
$$T_{H\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Table 15. Thermal Parameter

Area/island (cm ²)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	1.6	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.08	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

VN750-E / VN750S-E / VN750PT-E / VN750B5-E

Figure 39. P²PAK Thermal Impedance Junction Ambient Single PulseFigure 40. Thermal fitting model of a single channel HSD in P²PAK

Pulse calculation formula

$$T_{H\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

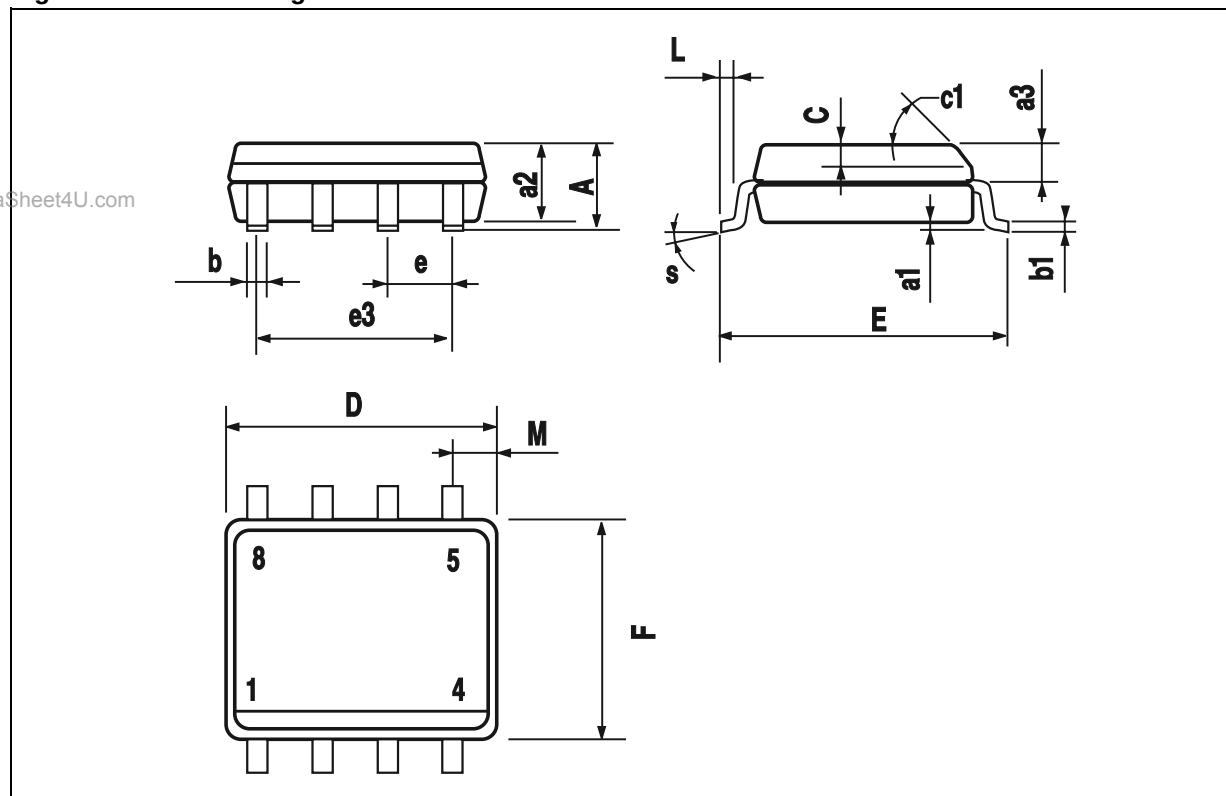
$$\text{where } \delta = t_p / T$$

Table 16. Thermal Parameter

Area/island (cm ²)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	0.7	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.055	
C4 (W.s/°C)	0.4	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

VN750-E / VN750S-E / VN750PT-E / VN750B5-E**PACKAGE MECHANICAL****Table 17. SO-8 Mechanical Data**

Symbol	millimeters		
	Min	Typ	Max
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

Figure 41. SO-8 Package Dimensions

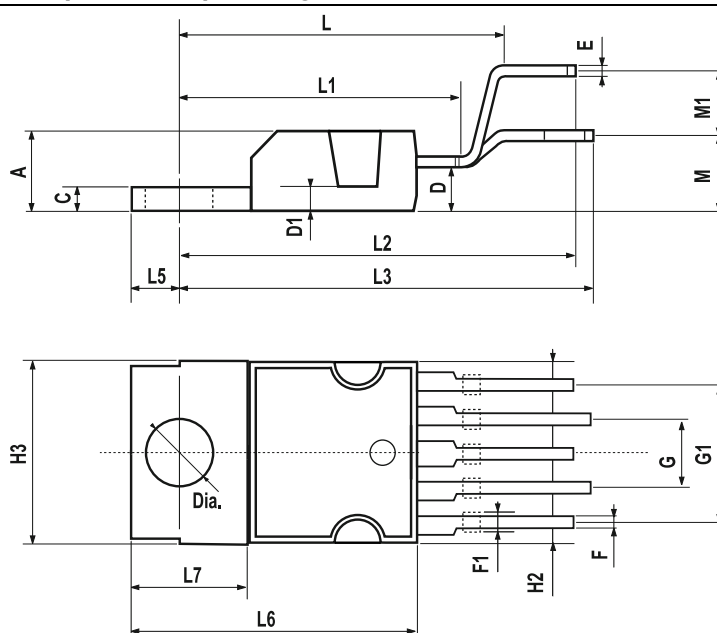
VN750-E / VN750S-E / VN750PT-E / VN750B5-E

PACKAGE MECHANICAL

Table 18. PENTAWATT (VERTICAL) Mechanical Data

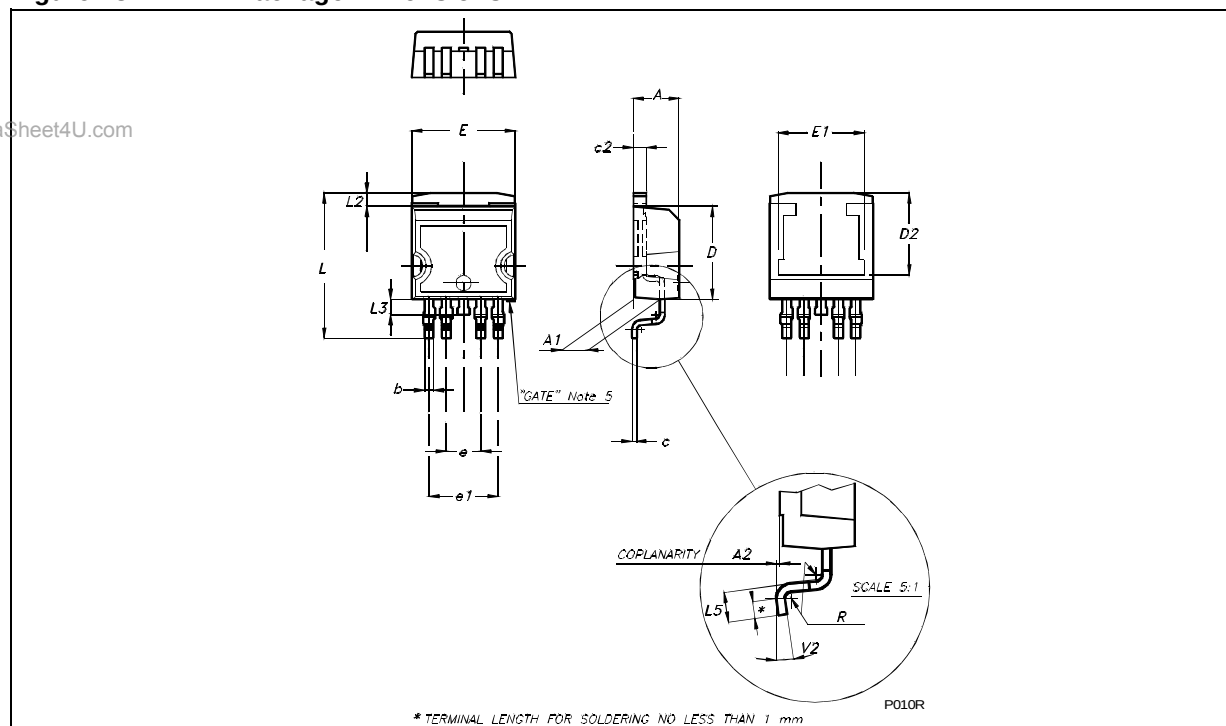
Symbol	millimeters		
	Min	Typ	Max
A			4.8
C			1.37
D	2.4		2.8
D1	1.2		1.35
E	0.35		0.55
F	0.8		1.05
F1	1		1.4
G	3.2	3.4	3.6
G1	6.6	6.8	7
H2			10.4
H3	10.05		10.4
L		17.85	
L1		15.75	
L2		21.4	
L3		22.5	
L5	2.6		3
L6	15.1		15.8
L7	6		6.6
M		4.5	
M1		4	
Diam.	3.65		3.85

Figure 42. PENTAWATT (VERTICAL) Package Dimensions



VN750-E / VN750S-E / VN750PT-E / VN750B5-E**PACKAGE MECHANICAL****Table 19. P²PAK Mechanical Data**

Symbol	millimeters		
	Min	Typ	Max
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0°		8°
Package Weight	1.40 Gr (typ)		

Figure 43. P²PAK Package Dimensions

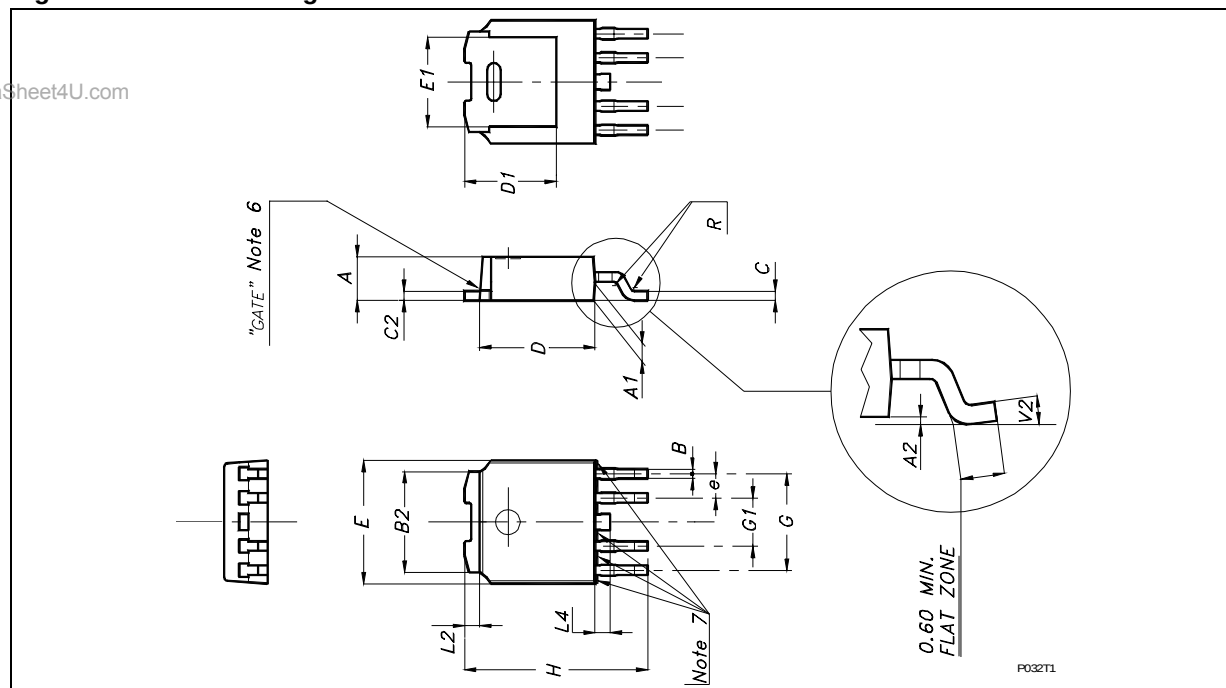
VN750-E / VN750S-E / VN750PT-E / VN750B5-E

PACKAGE MECHANICAL

Table 20. PPAK Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0°		8°
Package Weight	Gr. 0.3		

Figure 44. PPAK Package Dimensions



VN750-E / VN750S-E / VN750PT-E / VN750B5-E

Figure 45. SO-8 TUBE SHIPMENT (no suffix)

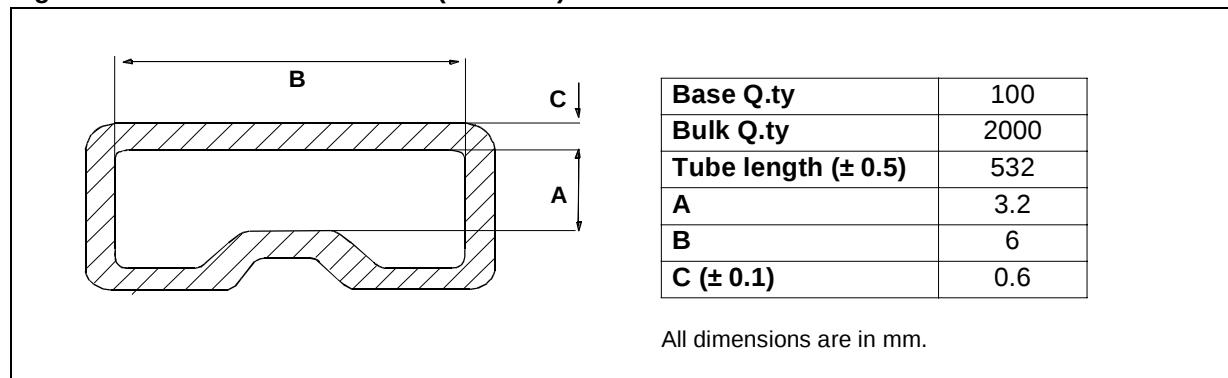
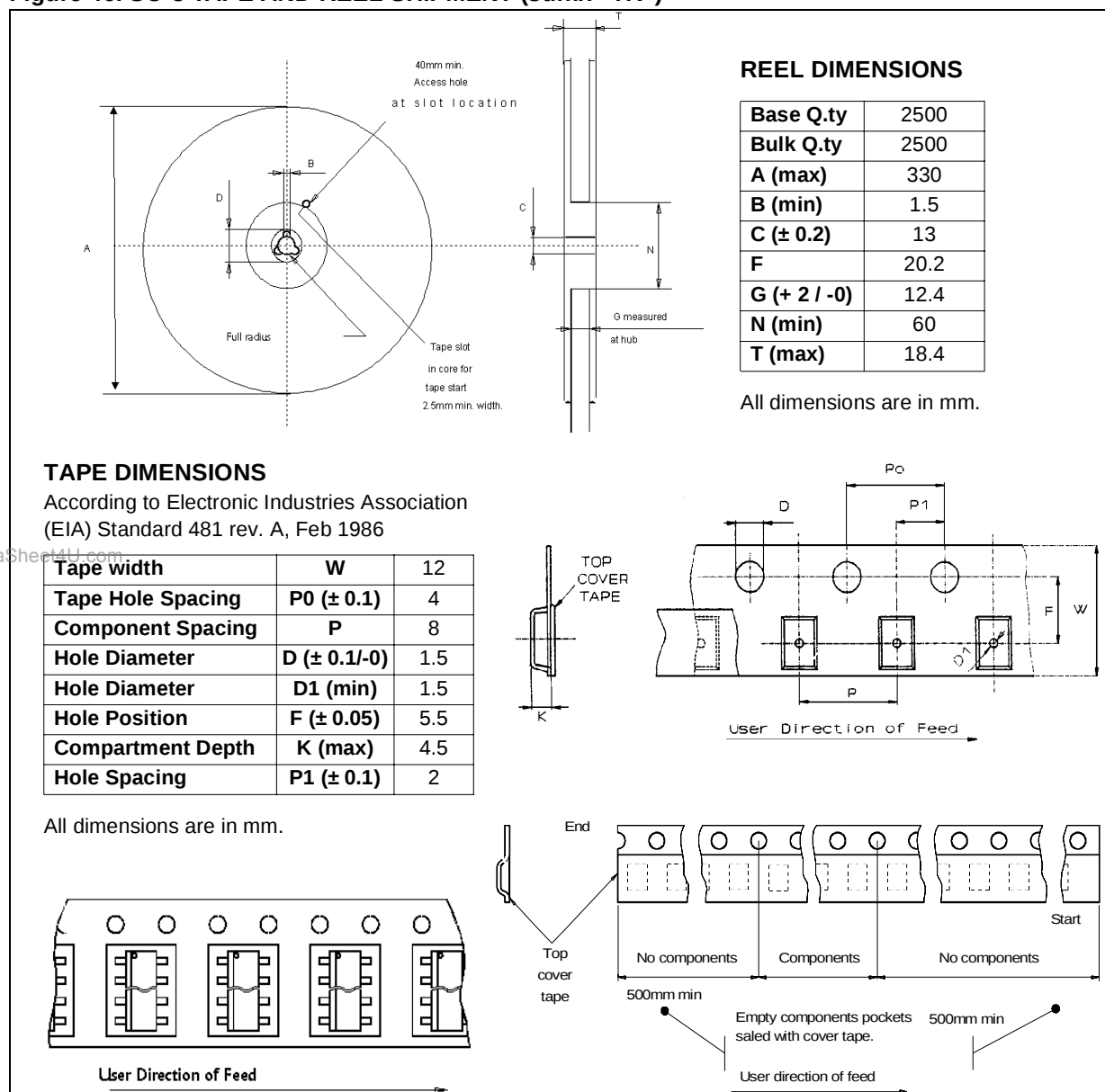
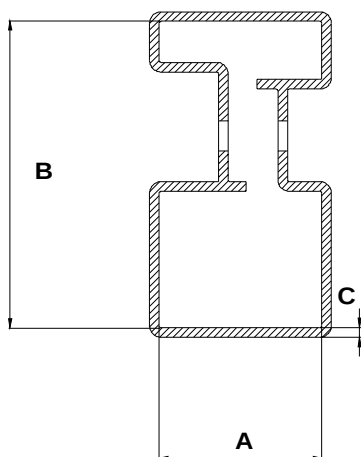


Figure 46. SO-8 TAPE AND REEL SHIPMENT (suffix "TR")



VN750-E / VN750S-E / VN750PT-E / VN750B5-E

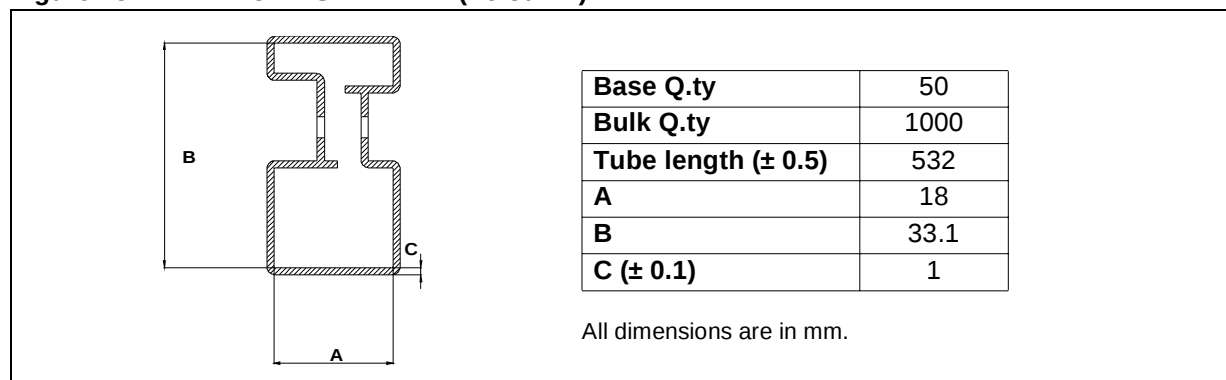
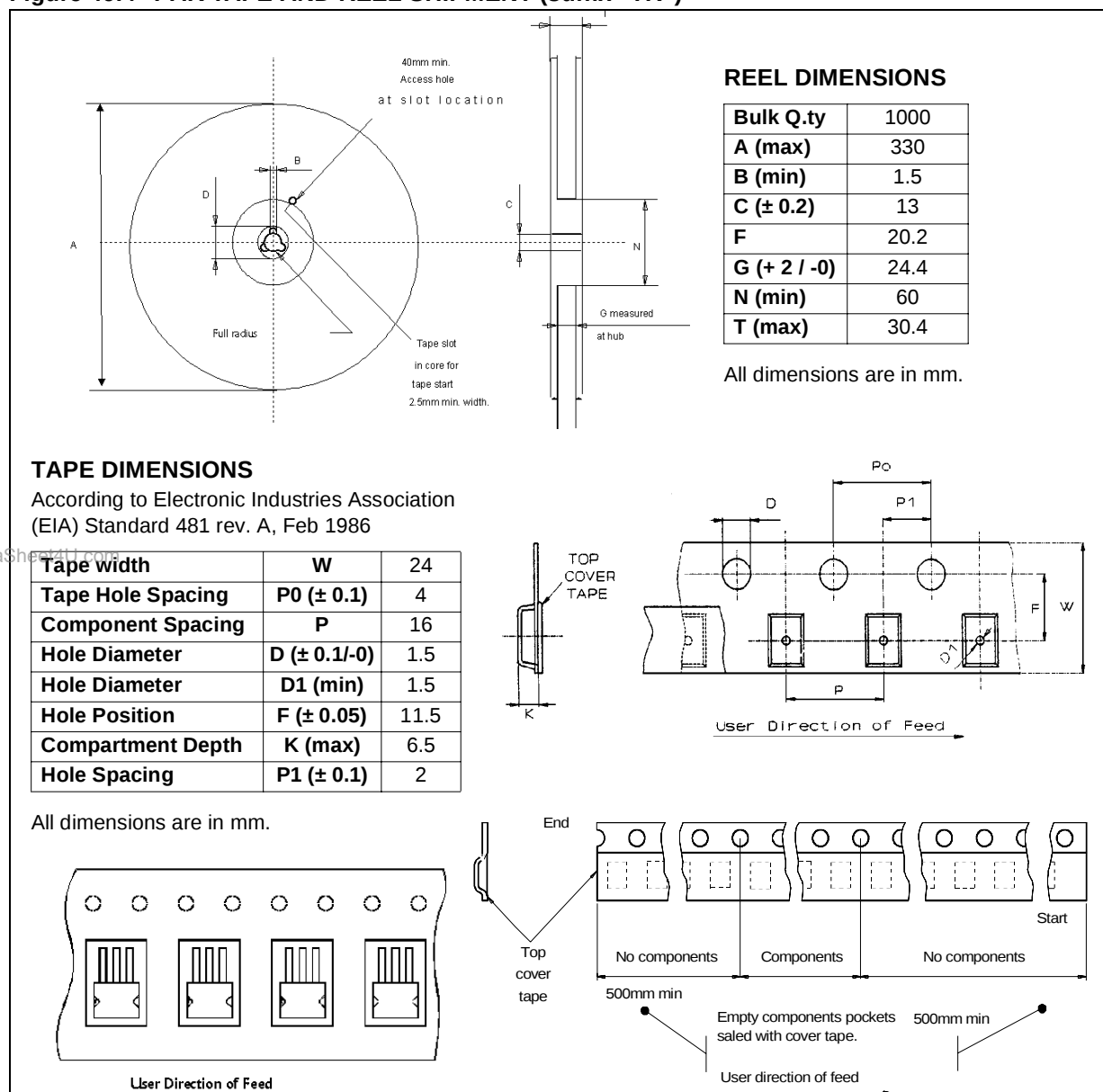
Figure 47. PENTAWAT TUBE SHIPMENT (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

VN750-E / VN750S-E / VN750PT-E / VN750B5-E

Figure 48. P²PAK TUBE SHIPMENT (no suffix)Figure 49. P²PAK TAPE AND REEL SHIPMENT (suffix "TR")

VN750-E / VN750S-E / VN750PT-E / VN750B5-E

Figure 50. PPAK SUGGESTED PAD LAYOUT and TUBE SHIPMENT (no suffix)

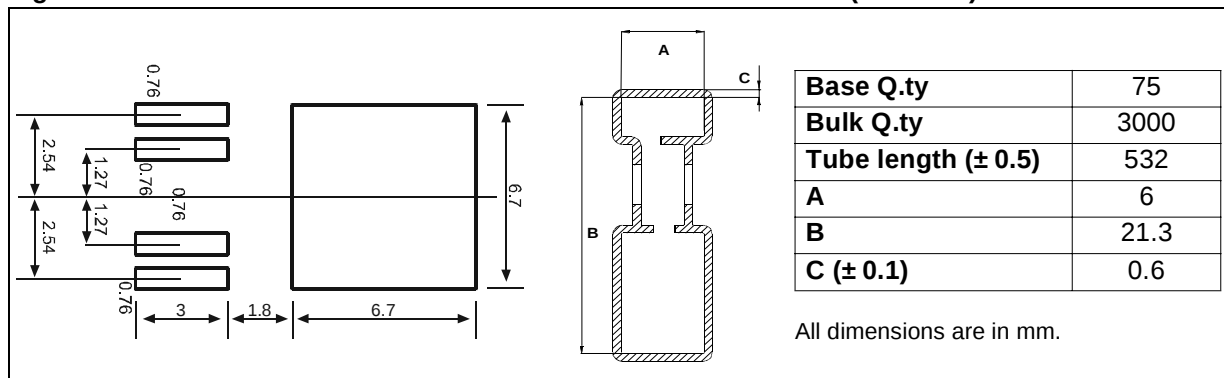
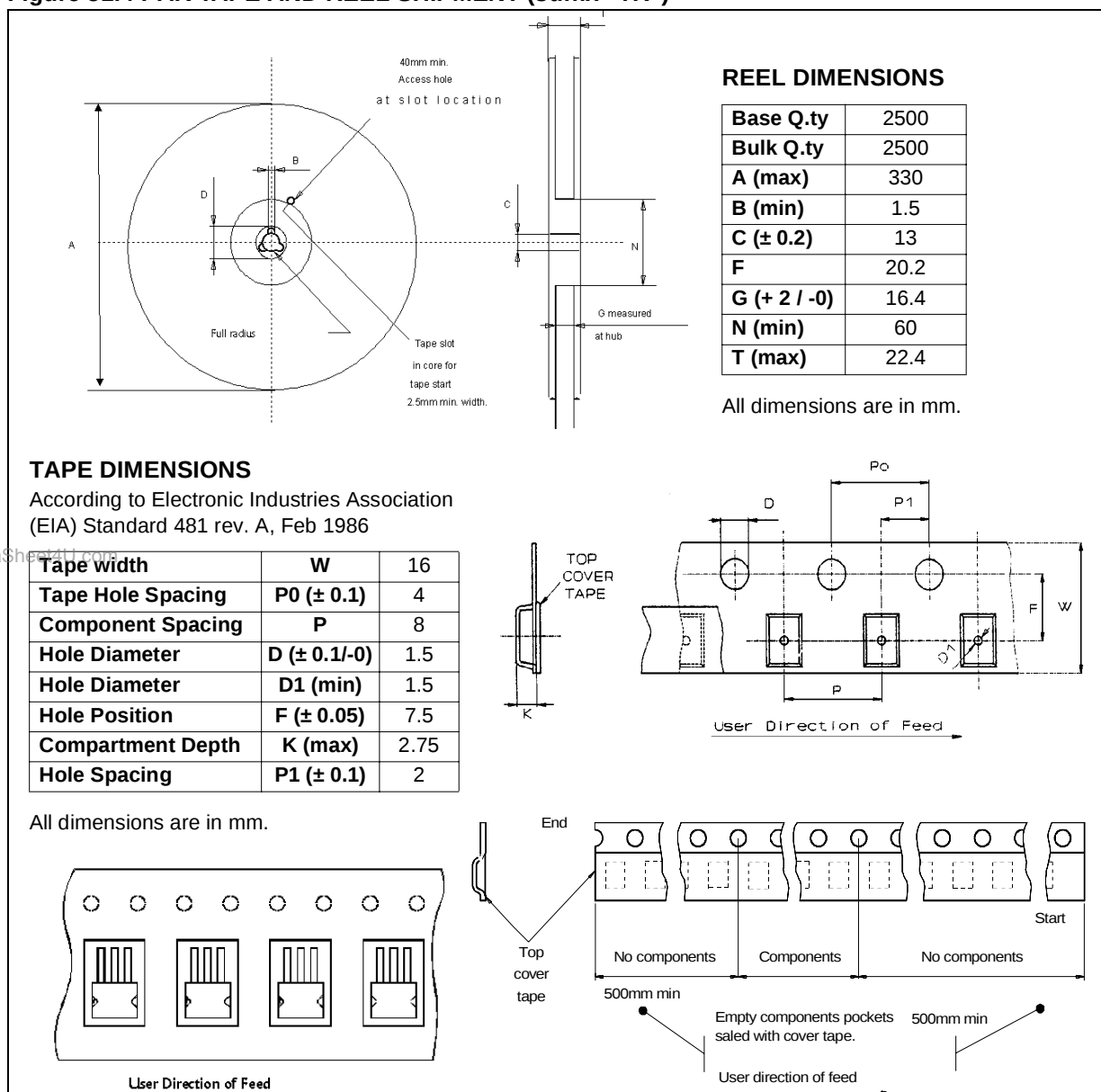


Figure 51. PPAK TAPE AND REEL SHIPMENT (suffix "TR")



VN750-E / VN750S-E / VN750PT-E / VN750B5-E

REVISION HISTORY**Table 21. Revision History**

Date	Revision	Description of Changes
Oct. 2004	1	- First Issue.

VN750-E / VN750S-E / VN750PT-E / VN750B5-E

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