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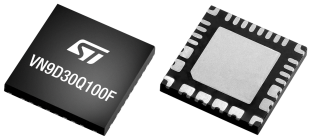
VN9D30Q100F

Datasheet

6-channel high-side driver with 24-bit SPI interface for automotive applications



QFN 6x6

Product status link
VN9D30Q100F

Product summary	
Order code	VN9D30Q100FTR
Package	QFN 6X6
Packing	Tape and reel

Features

Channel	V_{CC}	R_{ON} typ.	I_{LIMH} typ.
0, 5	28 V	33 mΩ	31.5 A
1, 2, 3, 4	28 V	90 mΩ	14 A

- AEC-Q100 qualified
- General
  - Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
  - 24-bit ST-SPI for full diagnostic and digital current sense feedback
  - Integrated 10-bit ADC for digital current sense
  - Integrated PWM engine with independent phase shift and frequency generation (for each channel)
  - Programmable Bulb/LED mode for all channels
  - Advanced limp-home functions for robust fail-safe system
  - Very low standby current
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Control through direct inputs and/or SPI
  - Compliant with European directive 2002/95/EC
- Diagnostic functions
  - Digital proportional load current sense
  - Synchronous diagnostic of over load and short to GND, output shorted to V_{CC} and OFF-state open-load
  - Programmable case overtemperature warning
- Protection
  - Two levels load current limitation
  - Self limiting of fast thermal transients
  - Undervoltage shutdown
  - Overvoltage clamp
  - Latch-off or programmable time limited auto restart (power limitation and overtemperature shutdown)
  - Load dump protected
  - Protection against loss of ground

Description

The VN9D30Q100F is a device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads directly connected to ground. The device is protected against voltage transient on V_{CC} pin.

Programming, control and diagnostics are implemented via the SPI bus.

A digital current sense feedback for each channel is provided through an integrated 10-bit ADC with 0.1% of FSR. Dedicated trimming bits allow to adjust the ADC reference current.

The device is equipped with 6 outputs controllable via SPI or with the 2-OTP assignable direct inputs.

The device detects open-load in OFF-state conditions.

Real time diagnostic is available through the SPI bus (open-load, output short to V_{CC}, overtemperature, communication error, power limitation or latch off).

Output current limitation protects the device in an overload condition. The device can limit the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown can be configured as latched off or programmable time limited auto restart.

The device enters a limp-home mode in case of loss of digital supply (V_{DD}), reset of digital memory or watchdog monitoring time-out event. In limp-home mode each output is set according to the programmed register: to be always OFF, or according to the 2x direct inputs pins.

1 Block diagram and pin description

Figure 1. Block diagram

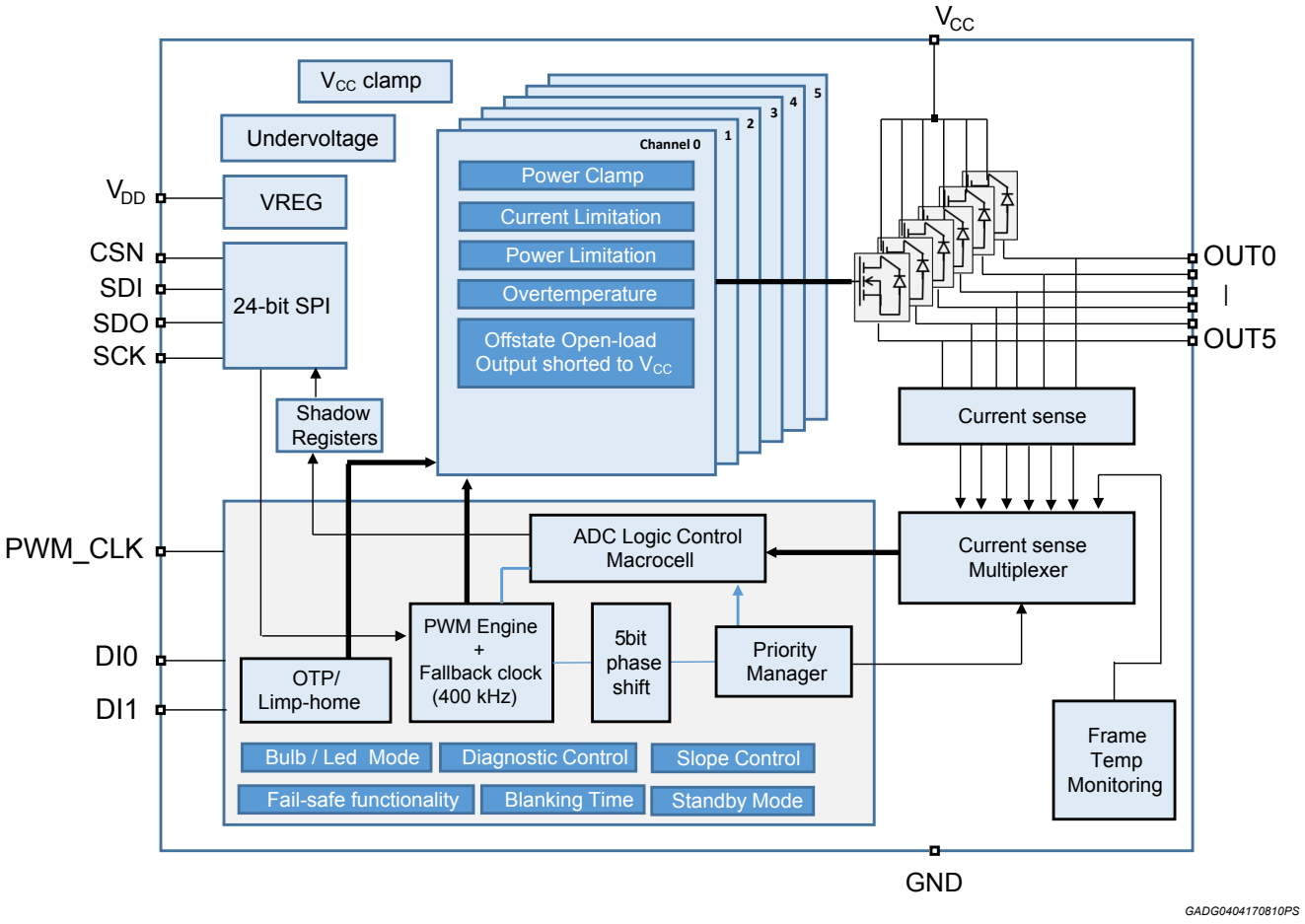
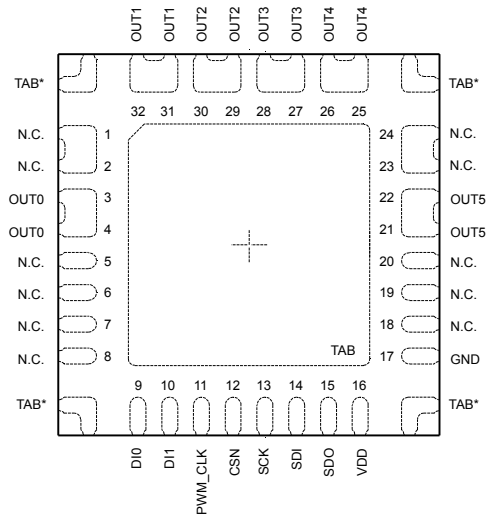


Figure 2. Connection diagram (top through view)



*: Electrically connected to TAB. Those pins are intended for thermo-mechanical purposes only. They have to be soldered, but must be electrically isolated at PCB level.

Table 1. Pin functionality description

Pin #	Name	Function
Tab	V_{CC}	Battery connection. This is the backside TAB and is the direct connection to drain Power MOSFET switches.
1-2	N.C.	Not connected pin
3-4	OUT0	Power OUTPUT 0. It is the direct connection to the source Power MOSFET switch No. 0.
5-8	N.C.	Not connected pin
9-10	DI0, DI1	Direct Input. Direct control for OUTx in limp-home mode through OTP programmed Direct Input assignment. Configurable as OR combination with the relevant SPI OUTx Control bit in Normal mode.
11	PWM_CLK	PWM external clock. The frequency of the internal PWM signal is divided according to the programmed ratio. It is possible to select one of the 4xPWM divider ratios: from 1/512 to 1/4096.
12	CSN	Chip select not (active low). It is the selection pin of the device. It is a CMOS compatible input.
13	SCK	Serial clock. It is a CMOS compatible input.
14	SDI	Serial data input. Transfers data to be written serially into the device on SCK rising edge.
15	SDO	Serial data output. Transfers data serially out of the device on SCK falling edge.
16	VDD	DC supply input for the digital control part and SPI interface. 3.3 V and 5 V compatible, this is the input of the internal Voltage Regulator.
17	GND	Ground connection. This pin serves as the ground connection for the logic part of the device.
18-20	N.C.	Not connected pin
21-22	OUT5	Power OUTPUT 5. It is the direct connection to the source Power MOSFET switch No. 5.
23-24	N.C.	Not connected pin
25-26	OUT4	Power OUTPUT 4. It is the direct connection to the source Power MOSFET switch No. 4.
27-28	OUT3	Power OUTPUT 3. It is the direct connection to the source Power MOSFET switch No. 3.
29-30	OUT2	Power OUTPUT 2. It is the direct connection to the source Power MOSFET switch No. 2.
31-32	OUT1	Power OUTPUT 1. It is the direct connection to the source Power MOSFET switch No. 1.

2 Functional description

2.1 Device interfaces

- SPI: bidirectional interface, accessing RAM/ROM registers (CSN, SCK, SDI, SDO)
- DIx: input pins for outputs control while the device is in fail-safe mode, standby mode, or reset mode (usable also in normal mode according to "Direct input enable control register" - DIENCR, setting)
- V_{DD}: 5 V or 3.3 V supply. The internal regulator block that delivers the internal logic supply voltage from the V_{DD} input is able to handle both 3.3 V and 5 V.

2.2 Operating modes

The device can operate in seven different modes:

- Reset mode
- Fail-safe mode
- Normal mode
- Standby mode
- Sleep mode 1
- Sleep mode 2
- Battery undervoltage mode

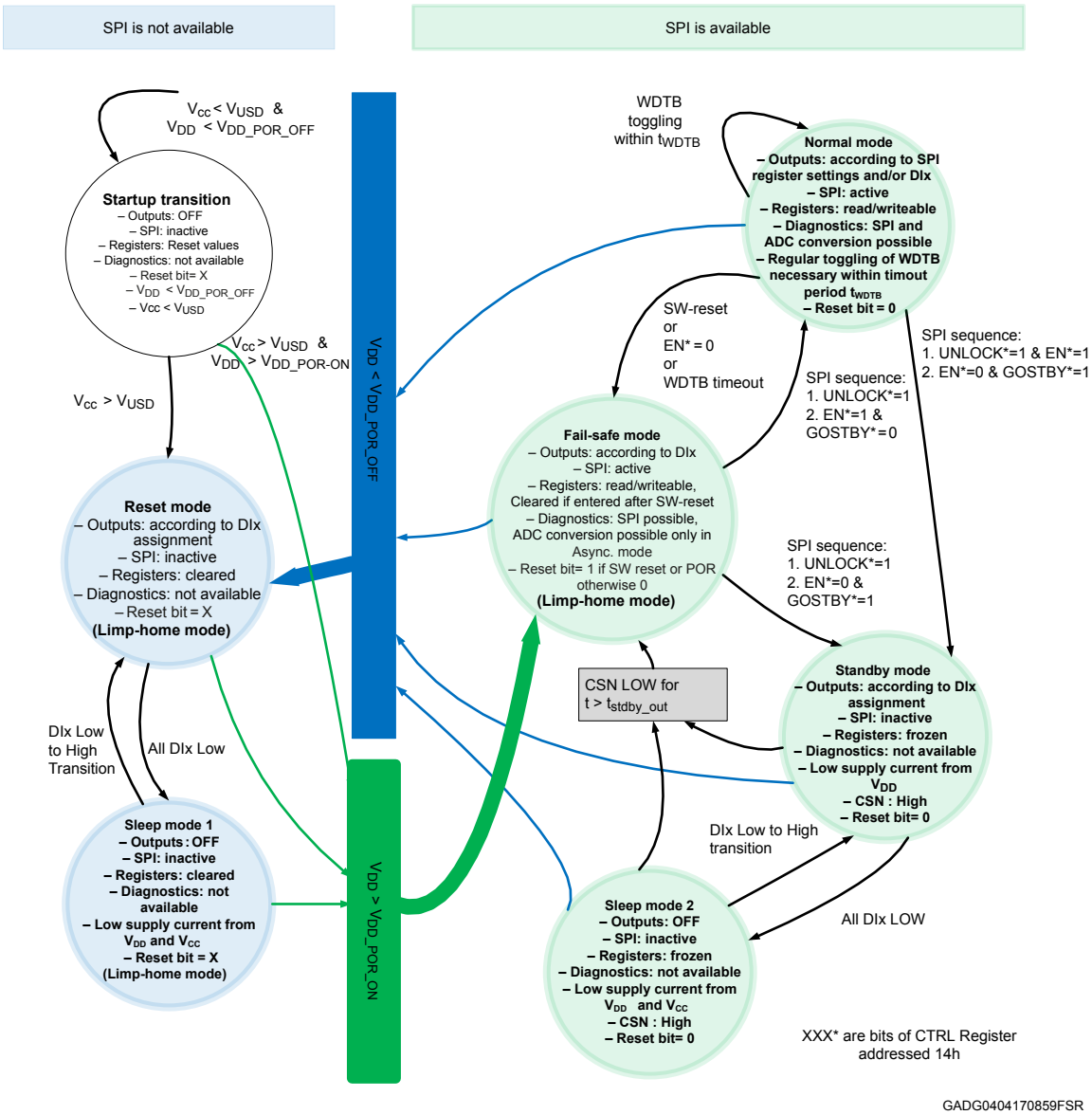
The reset mode, the fail-safe mode, and the sleep mode 1 are combined into the limp-home mode. In this mode, the chip is able to operate without the connection to the SPI. All transitions between the states in limp-home mode are driven by V_{DD} and DIx. The outputs are controlled by the direct inputs DIx according to the internally programmed outputs assignment. By default, DI0 drives OUTPUT0, 5 (medium power channels), DI1 drives OUTPUT1, 2, 3, 4 (low power channels).

Table 2. Operating modes

Operating mode	Entering conditions	Leaving conditions	Characteristics
Startup transition (this is not an operating mode)		• V_{CC} > V_{USD}: reset • (V_{DD} > $V_{DD\_POR\_ON}$) and (V_{CC} > V_{USD}): fail-safe	• Outputs: OFF • SPI: inactive • Registers: reset values • Diagnostics: not available • Reset bit = X
Reset (limp-home mode)	• Startup mode: V_{CC} > V_{USD} • Sleep 1: • DIx low to high • Any other mode: V_{DD} < $V_{DD\_POR\_OFF}$	• All DIx low: sleep 1 • V_{DD} > $V_{DD\_POR\_ON}$: fail-safe	• Outputs: according to DIx • SPI: inactive • Registers: reset values • Diagnostics: not available • Reset bit = X
Sleep 1 (limp-home mode)	Reset: all DIx = 0	• V_{DD} > $V_{DD\_POR\_ON}$: fail-safe • DIx low to high: reset	• Outputs: OFF • SPI: inactive • Registers: reset values • Diagnostics: not available • Low supply current from V_{CC} • Reset bit = X
Fail-safe (limp-home mode)	• Reset or sleep 1: V_{DD} > $V_{DD\_POR\_ON}$ • Standby or sleep 2: CSN low for t > t_{stdby_out} • Normal: EN = 0 or WDTB toggling timeout or SW-reset	• V_{DD} < $V_{DD\_POR\_OFF}$: reset • SPI sequence 1. UNLOCK = 1 2. GOSTBY = 0 and EN = 1: normal • SPI sequence 1. UNLOCK = 1 2. GOSTBY = 1 and EN = 0: standby	• Outputs: according to DIx • SPI: active • Registers: read/write possible, cleared if entered after SW reset • Diagnostics: SPI possible, ADC conversion possible only in asynchronous mode • Reset bit = 1 if entered after SW reset or POR, else reset bit = 0
Normal	• Fail-safe: SPI sequence 1. UNLOCK = 1 2. GOSTBY = 0 and EN = 1	• V_{DD} < $V_{DD\_POR\_OFF}$: reset • SPI sequence 1. UNLOCK = 1 & EN = 1 2. GOSTBY = 1 and EN = 0: standby • EN = 0 or WDTB time-out or SW reset: fail-safe	• Outputs: according to SPI register settings and/or DIx • SPI: active • Registers: read/write is possible • Diagnostics: SPI and ADC conversion in all modes (sampled and asynchronous) are possible • Regular toggling of WDTB is necessary within timeout period t_{WDTB} • Reset bit = 0
Standby	• Normal: SPI sequence 1. UNLOCK = 1 & EN = 1 2. GOSTBY = 1 and EN = 0 • Fail-safe: SPI sequence 1. UNLOCK = 1 2. GOSTBY = 1 and EN = 0 • Sleep 2: DIx low to high	• V_{DD} < $V_{DD\_POR\_OFF}$: reset • CSN low for t > t_{stdby_out}: fail-safe • All DIx low: sleep 2	• Outputs: according to DIx • SPI: inactive • Registers: frozen • Diagnostics: not available • Low supply current from V_{DD} • CSN: High • Reset bit = 0
Sleep 2	Standby: all DIx = 0	• V_{DD} < $V_{DD\_POR\_OFF}$: reset • CSN low for t > t_{stdby_out}: fail-safe • DIx low to high: standby	• Outputs: OFF • SPI: inactive • Registers: frozen • Diagnostics: not available

Operating mode	Entering conditions	Leaving conditions	Characteristics
			• Low supply current from V_{DD} and V_{CC} • CSN: high • Reset bit = 0
Battery undervoltage (this is not an operating mode)	Any mode: $V_{CC} < V_{USD}$	$V_{CC} > V_{USD} + V_{USDhyst}$: back to last mode	• Outputs: OFF and independent from DIx and SPI • SPI: as the last mode • Reset bit: as the last mode

Figure 3. Device state diagram



For an overview over the operating modes and the triggering conditions, refer to Section 6.4: Limp-home mode.

2.2.1 Startup transition phase

This is not an operation mode but a transition step to reset operation mode from the power-ON. In this phase, neither the digital supply voltage V_{DD} nor VCC is available ($V_{DD} < V_{DD\_POR\_ON}$ and $V_{CC} < V_{USD}$).

This phase does not have to be confused with undervoltage mode where also the power supply is not available ($V_{CC} < V_{USD}$) after an operation mode. The device leaves this phase to reset mode as soon as $V_{CC} > V_{USD}$. In case ($V_{CC} < V_{USD}$) but ($V_{DD} > V_{DD\_POR\_ON}$) then the device leaves this phase to fail-safe mode.

2.2.2 Reset mode

The device is in limp-home state.

Reset mode is entered after startup but also each time the digital supply voltage V_{DD} falls below $V_{DD\_POR\_OFF}$ ($V_{DD} < V_{DD\_POR\_OFF}$ and $V_{CC} > V_{USD}$).

The outputs are controlled by the direct inputs DIx according to the internally programmed outputs assignment. At least one DIx is in logic high.

The SPI is inactive (no read/write possible) and the diagnostic is not available. The registers have the reset values.

The device leaves this mode if only if $V_{DD} > V_{DD\_POR\_ON}$ or all DIx go to low.

The reset bit inside the global status byte is unreadable since the SPI is inactive (for more information refer to the Section 4.3.1: Global status byte description).

The diagnostics is not available, but the protections are fully functional. In case of overtemperature or power limitation, the outputs work in unlimited auto restart.

The device enters reset mode under three conditions:

- Automatically during startup
- If it is in any other mode and if V_{DD} falls below $V_{DD\_POR\_OFF}$
- If it is in sleep mode 1 and if one input DIx is set to 1

The device exits reset mode under two conditions:

- If V_{DD} rises above $V_{DD\_POR\_ON}$, the device enters fail-safe mode
- If all inputs DIx are 0, the device enters sleep mode 1.

2.2.3 Fail-safe mode

The device is in limp-home state.

The digital supply voltage V_{DD} is available. ($V_{DD} > V_{DD\_POR\_ON}$) and the SPI registers are active (SPI read/write).

In fail-safe mode, the digital current sense is available only in asynchronous mode and the digital fault diagnostic is available through the SPI bus.

The outputs are controlled by the direct inputs DIx regardless of the SPI commands.

The registers are cleared to their reset value if fail-safe is entered through an SW reset.

The reset bit is 1 if the last state was reset mode or the last command was an SW reset and it is reset to 0 after the first SPI access (for more information refer to Section 4.3.1: Global status byte description).

The SPI diagnostics is available.

The protections are fully functional. In case of overtemperature or power limitation, the outputs work in unlimited auto restart.

The device enters fail-safe mode under the following conditions:

- If it is in reset mode or in sleep mode 1 and V_{DD} rises above $V_{DD\_POR\_ON}$, ($V_{DD} > V_{DD\_POR\_ON}$)
- If it is in standby mode or in sleep mode 2 and CSN is low for $t > t_{stdby\_out}$
- If it is in normal mode and bit EN is cleared
- If it is in normal mode and WDTB is not toggled within t_{WDTB} (watchdog timeout)
- If it is in normal mode and the SPI sends an SW reset

The device exits fail-safe mode under three conditions:

- If the SPI sends the goto normal mode sequence, the device enters normal mode:
  - In a first communication set bit UNLOCK = 1
  - In the consecutive communication set bit GOSTBY = 0 and bit EN = 1

This mechanism avoids entering the normal mode unintentionally.

- If the SPI sends the goto standby mode sequence, the device enters standby mode:
  - In a first communication set bit UNLOCK = 1
  - In the consecutive communication set bit GOSTBY = 1 and bit EN = 0

This mechanism avoids entering the standby mode unintentionally.

- If V_{DD} falls below $V_{DD\_POR\_OFF}$, the device enters reset mode.

Transition to fail-safe mode from normal mode, using the SPI register

Only one frame is needed: Write “CTRL” 0x0001.

Table 3. Frame 1 (write CTRL 0x0001)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	0	0	0	0	0	0	0
DATA2	Not used	Not used	Lockbit3	Lockbit2	Lockbit1	Lockbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	1

Transition to fail-safe mode from normal mode by SW-Reset

SPI reset occurs by using the “Read device information” command (applicable only on ROM area) at the reserved ROM address 0x3F. This is equivalent to sending a 0xFF command.

Only one frame is needed: **read “ROM” 0x3F**.

Table 4. Frame 1: read (ROM) 0x3F 0x--

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	1	1	1	1	1	1	1	1
DATA1	x(1)	x	x	x	x	x	x	x
	0	0	0	0	0	0	0	0
DATA2	x	x	x	x	x	x	x	x
	0	0	0	0	0	0	0	0

1. *X: do not care. At least one of these bits must be zero, as 0xFFFF frame is not allowed.*

The entry to the fail-safe mode can occur due to the CSN timeout.

In this specific case, the following procedure must be executed to leave the fail-safe mode:

- Removing the cause of the CSN stuck
- Toggling the CSN pin for a min t_{SHCH} (time to release the SDO line), see parameter in Table 48. Dynamic characteristics.
- Sending the SPI frames

If the above procedure is not respected, the first SPI frame is rejected and the state transition fails.

2.2.4 Normal mode

In this mode, all device functions are available. The transition to this mode is only possible from a previous fail-safe mode.

Outputs can be driven by SPI commands or a combination of SPI commands and direct inputs DIx.

To maintain the device in normal mode, the watchdog toggle bit in register CONFIG has to be toggled within the watchdog timeout period t_{WDTB} (see Table 48. Dynamic characteristics).

Diagnosis and current sense are available through the SPI bus (digital).

The protections are fully functional. The outputs can be set to latch-off or programmable time limited auto restart.

- In time limited, auto restart the outputs are switched on again automatically after an overtemperature or power limitation event within the limited programmed time frame (refer to Section 6.2: Blanking window values).
- In latch mode, the relevant status register has to be cleared to switch the outputs on again (refer to Section 6.2: Blanking window values).

The device enters normal mode under one condition:

- If it is in fail-safe mode and the SPI sends the goto normal mode sequence:
  - In a first communication set bit UNLOCK = 1–write “CTRL” 0x4000;
  - In the consecutive communication set bit GOSTBY = 0 and bit EN = 1–write “CTRL” 0x0800;

The transition from fail-safe mode to normal mode is performed by two special SPI sequences

Table 5. Frame 1 (write CTRL 0x4000)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	1	0	0	0	0	0	0
DATA2	Not used	Not used	Lockbit3	Lockbit2	Lockbit1	Lockbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

Table 6. Frame 2 (write CTRL 0x0800)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	0	0	0	1	0	0	0
DATA2	Not used	Not used	Lockbit3	Lockbit2	Lockbit1	Lockbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

The device exits normal mode under five conditions:

- If V_{DD} falls below $V_{DD\_POR\_OFF}$, the device enters reset mode.
- If the SPI sends the goto standby sequence, the device enters standby mode:
  - In a first communication set UNLOCK = 1
  - In the consecutive communication set GOSTBY = 1 and EN = 0

This mechanism avoids entering standby mode unintentionally.

- If the SPI clears the EN bit (EN = 0), the device enters fail-safe mode.
- Watchdog time out: If WDTB is not toggled within the monitoring timeout period t_{WDTB}, the device enters fail-safe mode.
- If the SPI sends an SW reset command (command byte = 0xFFh), all registers are cleared and the device enters fail-safe mode.

2.2.5 Standby mode

The device is in the low consumption state of the digital part.

The outputs are controlled by the direct inputs DIx only.

The current from V_{DD} is nearly 0.

The digital supply voltage V_{DD} is available. (V_{DD} > $V_{DD\_POR\_ON}$) but SPI is inactive (no read/write is possible, the SPI registers are frozen to their last state before entering standby mode).

During standby mode, the above conditions are kept if at least one DIx is in logic high.

CSN is inactive high state (independent of MCU).

The diagnostics is not available.

The protections are fully functional. The outputs are set to unlimited auto restart mode.

The device enters standby mode under three conditions:

- If it is in fail-safe mode and the SPI sends the goto standby sequence:
  - In a first communication set UNLOCK = 1
  - In the consecutive communication set GOSTBY = 1 and EN = 0

  This mechanism avoids entering standby mode unintentionally.
- If it is in normal mode and the SPI sends the goto standby sequence:
  - In a first communication set UNLOCK = 1
  - In the consecutive communication set GOSTBY = 1 and EN = 0

  This mechanism avoids entering standby mode unintentionally.
- If it is in sleep mode 2 and one input DIx is set to one.

The device exits standby mode under three conditions:

- If V_{DD} falls below $V_{DD\_POR\_OFF}$, the device enters reset mode.
- If CSN is low for t > t_{stdby_out}, the device wakes up. As the device is in fail-safe mode, the outputs are controlled through DIx pins, the ADC conversion is possible only in asynchronous mode and the digital diagnostic is available through the SPI bus.
- If all direct inputs DIx are 0, the device enters sleep mode 2 resulting in minimal supply current from V_{CC} and V_{DD}.

Transition from fail-safe mode to standby mode using SPI: two frames needed.

- Frame 1: write “CTRL” 0x4000
- Frame 2: write “CTRL” 0x8000

Table 7. Frame 1 (write CTRL 0x4000)–fail-safe mode to standby mode

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	1	0	0	0	0	0	0
DATA2	Not used	Not used	Lockbit3	Lockbit2	Lockbit1	Lockbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

Table 8. Frame 2 (write CTRL 0x8000)–fail-safe mode to standby mode

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	1	0	0	0	0	0	0	0
DATA2	Not used	Not used	Lockbit3	Lockbit2	Lockbit1	Lockbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

Transition from normal mode to standby mode using SPI: two frames needed

- Frame 1: write “CTRL” 0x4801
- Frame 2: write “CTRL” 0x8000

Table 9. Frame 2 (write CTRL 0x4801)–normal mode to standby mode

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	1	0	0	1	0	0	0
DATA2	Not used	Not used	Lockbit3	Lockbit2	Lockbit1	Lockbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	1

Table 10. Frame 2 (write CTRL 0x8000)–normal mode to standby mode

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	1	0	0	0	0	0	0	0
DATA2	Not used	Not used	Lockbit3	Lockbit2	Lockbit1	Lockbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

2.2.6 Sleep mode 1

The device is in limp-home state.

The device has very low consumption for both digital and power parts. Current consumption from the digital part is nearly zero and the current consumption on V_{CC} is supply current in sleep mode 1.

The digital supply voltage V_{DD} is not available ($V_{DD} < V_{DD\_POR\_OFF}$) and SPI is inactive (the read and write functions are not possible and all registers are cleared and have the reset values).

- The diagnostics is not available.
- The output stages are all off.
- Protections are inactive.

The device enters sleep mode 1 under one condition:

- If from reset mode, all direct inputs DIx are going low.

The device exits sleep mode 1 under two conditions:

- If V_{DD} rises above $V_{DD\_POR\_ON}$, the device enters fail-safe mode.
- If one of the inputs DNx is set to 1, the device enters reset mode.

2.2.7 Sleep mode 2

The device is in very low consumption state for both digital and power parts. Current consumption from the digital part is I_{DDstd} and the current consumption on V_{CC} is supply current in sleep mode 2.

The digital supply voltage V_{DD} is available ($V_{DD} > V_{DD\_POR\_ON}$) but SPI is not active (the read and write functions are not possible and all registers are frozen).

CSN is inactive high state (independent of MCU).

In sleep mode 2 the following limitations must be considered:

- The diagnostics is not available.
- The output stages are all off.
- Protections are inactive.

The device enters sleep mode 2 under one condition:

- If from standby mode, all direct inputs DIx are going low.

The device exits sleep mode 2 under three conditions:

- If V_{DD} falls below $V_{DD\_POR\_OFF}$, the device enters reset mode.
- If CSN is low for t > t_{stdby_out}, the device enters fail-safe mode.
- If one of the inputs DIx is set to 1, the device enters standby mode.

2.2.8 Battery undervoltage mode

This is not an operation mode but a transition step, where the power supply voltage is (V_{CC} < V_{USD}).

If the battery supply voltage V_{CC} falls below the undervoltage shutdown threshold (V_{CC} < V_{USD}) the device enters battery undervoltage mode.

The current sense diagnostic is not available.

The output stages are off regardless of SPI status or DIx.

Three different cases occur, depending on the operating mode:

1. **From normal mode and from fail-safe mode:**
   In this mode, the digital supply voltage V_{DD} is available (V_{DD} > $V_{DD\_POR\_ON}$). The SPI is active and read/write functions are possible. The SPI diagnostics is available. After entering to the undervoltage mode, the information about the undervoltage is saved in a flag (VCCUV) in the OUTSRx register, the SPI register contents are retained. The SPI register reading is always possible.
   If V_{CC} rises above the threshold (V_{USD} + $V_{USDhyst}$) the device returns to the last mode and the flag is cleared (VCCUV).
   If during this state V_{DD} decreases to V_{DD} < $V_{DD\_POR\_OFF}$, the device is reset completely. The last operation mode information is lost. The device logic part is unpowered, therefore after increasing the supply voltage to (V_{CC} > V_{USD} + $V_{USDhyst}$) the operation mode is reset mode.
   If during this state, the DIx is changed, the operation mode is not changed and the output state is changed accordingly after V_{CC} recovering.
2. **From standby and sleep mode 2 modes:**
   In this mode, the digital supply voltage V_{DD} is available (V_{DD} > $V_{DD\_POR\_ON}$). The SPI is not active and the registers are frozen. The SPI diagnostics is not available. After entering to the undervoltage mode, the information about the undervoltage is not saved in a flag (VCCUV).
   If V_{CC} rises above the threshold (V_{USD} + $V_{USDhyst}$) the device returns to the last mode.
   If during this state (undervoltage mode) V_{DD} decreases to V_{DD} < $V_{DD\_POR\_OFF}$, the device is reset completely. The last operation mode information is lost. The device logic part is unpowered, therefore after increasing the supply voltage to (V_{CC} > V_{USD} + $V_{USDhyst}$) the operation mode is reset mode.
   If during this state (under voltage mode) the DIx is changed, the operation mode is also changed. After V_{CC} recovering, this new operation mode is taken into account.
3. **From reset mode or sleep mode1:**
   In this mode, the digital supply voltage V_{DD} is not available (V_{DD} < $V_{DD\_POR\_OFF}$) and SPI is not active. It is not possible to read/write via SPI. All SPI registers have the reset values. After entering to the undervoltage mode, the information about the undervoltage is not saved in a flag (VCCUV).
   If V_{CC} rises above the threshold V_{USD} + $V_{USDhyst}$, the device returns to the last mode.
   If during this state V_{DD} increases to V_{DD} > $V_{DD\_POR\_ON}$, the device is completely reset. After V_{CC} recovering (V_{CC} > V_{USD} + $V_{USDhyst}$), there will be a startup transition.

The undervoltage flag (VCCUV) is not saved in the following operation modes:

- Reset mode,
- Sleep mode 1,
- Sleep mode 2,
- Standby mode.

Figure 4. **Battery undervoltage shutdown diagram**

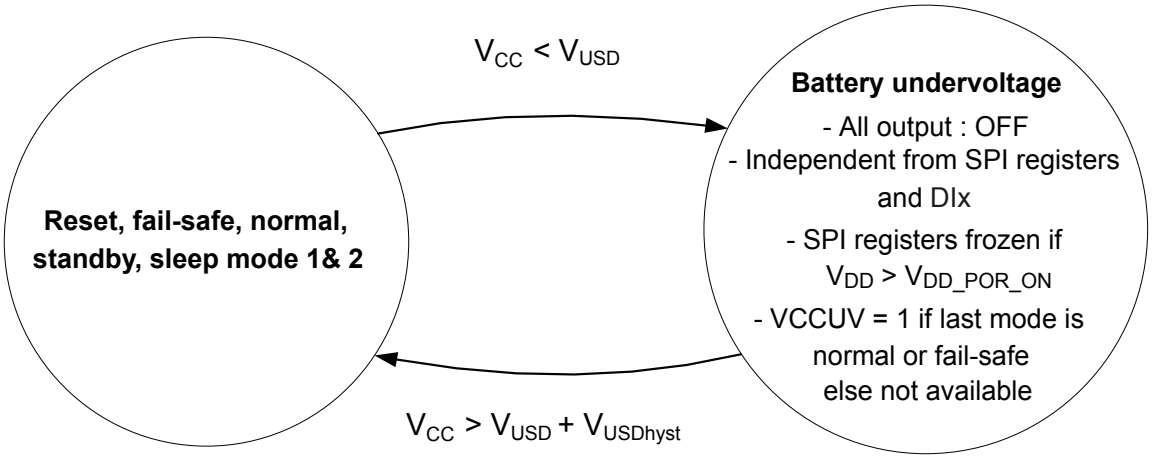
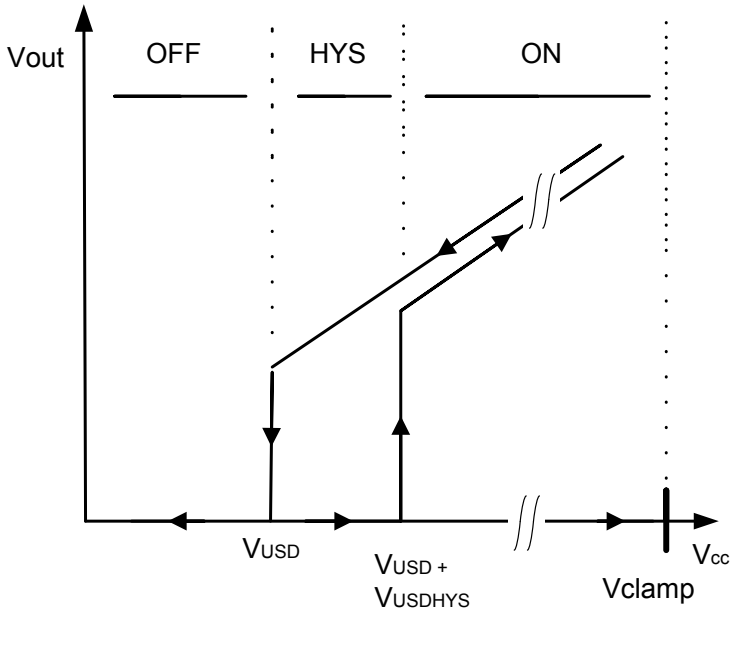


Figure 5. **Undervoltage shutdown**



2.2.9 Limp-home mode

The reset mode, the fail-safe mode, and the sleep mode 1 are combined into the limp-home mode. In this mode, the chip is able to operate without the connection to the SPI. All transitions between the states in limp-home mode are driven by V_{DD} and DIx. The outputs are controlled by the direct inputs DIx.

The DIx inputs can be driven by either an MCU I/O port or directly by KL15 (12 V) through series resistance. Each output has an OTP programmed direct input assignment for limp-home operation. Any output can be programmed to be always OFF in limp-home, or according to DI0 pin state or according to DI1 pin state.

Default configuration is:

- DI0 drivers OUT 0, 5
- DI1 drivers OUT 1, 2, 3, 4

For a direct entry to the limp-home mode during normal operating mode, the MCU uses the watchdog toggle bit (WDTB) or a dedicated SPI command. Changing the polarity of the WDTB within watchdog timeout (t_{WDTB}) keeps the device in normal mode.

3 Protections

3.1 Pre-warning

If the case-temperature rises above the case-thermal detection pre-warning threshold T_{CSD}, the bit T_{CASE} in the Global Status Byte is set. T_{CASE} is cleared automatically when the case-temperature drops below the case-temperature reset threshold T_{CR}.

3.2 Junction overtemperature (OT)

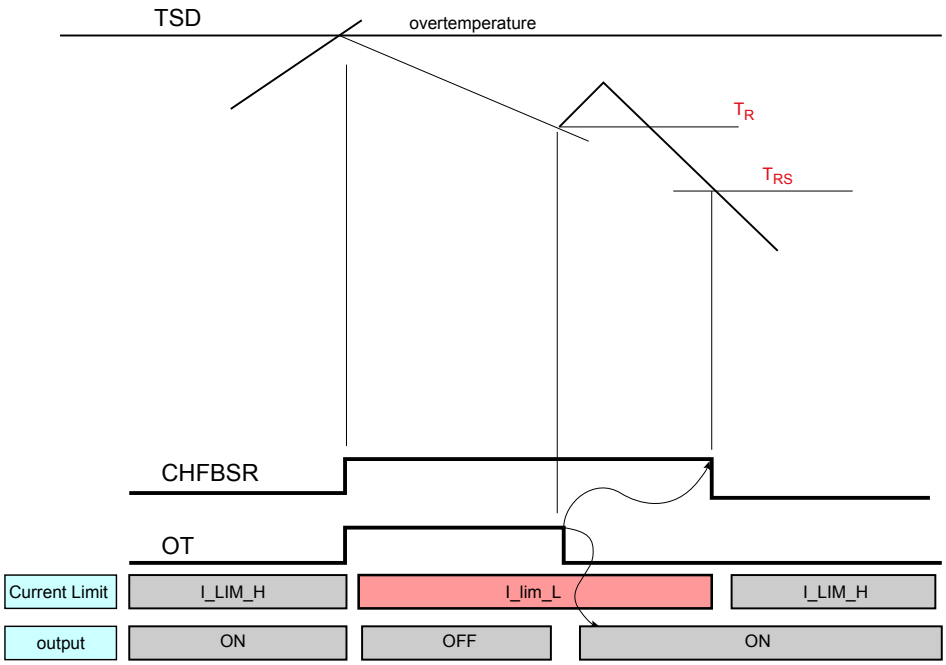
If the junction temperature of one channel rises above the shutdown temperature T_{TSD}, an overtemperature event (OT) is detected.

The channel is switched OFF and the corresponding bit in the address OUTSRx register - channel feedback status register (CHFBSRx) is set. Consequently, the thermal shutdown bit (bit 4) in the global status byte is set.

Each output channel can be either set as latch-off or programmable time limited auto restart operations in case of junction overtemperature event.

- In latched OFF operation, the output remains switched OFF and the corresponding bit “CHLOFFSRx” in the OUTSRx register is set, until the junction temperature falls below T_{RS} and a write command to the addressed latched OFF channel is sent (CHLOFFTCRx). The action clears the corresponding bit “CHLOFFSRx” in the OUTSRx register and bit 4 in the global status byte. Bit 4 only remains stuck at logic high if another fault condition is present at the same time.
- In time limited auto restart, during the programmed time, the output is switched off as described and switches on again automatically when the junction temperature falls below the reset temperature T_{RS}. The status bit “CHFBSRx“in the OUTSRx register is latched during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared when the junction temperature falls below the thermal reset temperature of the OT detection T_{RS}. After the programmed time expiration, the output remains switched OFF and acts as the above described latch-off mode.

Figure 6. Thermal shutdown



3.3 Power limitation (PL)

If the difference between junction temperature and case temperature ($\Delta T = T_J - T_C$) rises above the power limitation threshold ΔT_{PLIM}, a power limitation event is detected.

The corresponding bit CHFBSR (channel feedback status) in the OUTSRx register is set. The channel is switched OFF and therefore the bit 4 in the global status byte is set.

Each output channel can be either set as latch-off or programmable time limited auto restart operations in case of the power limitation event.

- In latched OFF operation, the output remains switched OFF and the corresponding bit “CHLOFFSRx” in the OUTSRx register is set, until the junction temperature falls below T_R and a write command to the addressed latched OFF channel is sent (CHLOFFTCRx). The action clears the corresponding bit “CHLOFFSRx” in the OUTSRx register and bit 4 in the global status byte. Bit 4 only remains stuck at logic high if another fault condition is present at the same time.
- In time limited auto restart, during the programmed time, the output is switched off as described and switches on again automatically when the difference of junction temperature and case temperature ($\Delta T = T_J - T_C$) decreases below ΔT_R. The status bit "CHFBSRx" in the OUTSRx register is set during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared when the difference of junction temperature and case temperature ($\Delta T = T_J - T_C$) decreases below ΔT_{RS}. After the programmed time expiration, the output remains switched OFF and acts as the above described latch-off mode.

4 SPI functional description

4.1 SPI communication

The SPI communication is based on a standard ST-SPI 24-bit interface using CSN, SDI, SDO and SCK signal lines.

Input data are shifted into SDI, MSB first while output data are shifted out on SDO, MSB first.

4.1.1 Signal description

During all operations, V_{DD} must be held stable and within the specified valid range: V_{DD} min to V_{DD} max.

Table 11. SPI signal description

Name	Function
Serial clock SCK	This input signal provides the timing of the serial interface. Data present at serial data input (SDI) are latched on the rising edge of the serial clock (SCK). Data on serial data output (SDO) change after the falling edge of the serial clock (SCK).
Serial data input SDI	This input signal is used to transfer data serially into the device. It receives data to be written. Values are sampled on the rising edge of the serial clock (SCK).
Serial data output SDO	This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of the serial clock (SCK).
Chip select CSN	When this input signal is High, the device is deselected and serial data output (SDO) is high-Z. Driving this input Low enables the communication. The communication must start on a Low level of serial clock (SCK). Data are accepted only if exactly 24 bits have been shifted in. **Note**: as per the ST_SPI standard, in case of failing communication: • Stuck at HIGH: – If the device is in normal mode, a WDTB timeout forces the device into fail-safe mode. The serial data-out (SDO) will stay in high-Z (high-Z). Any valid communication arrived after this event is accepted by the device. • Stuck at LOW: – in this case and whatever the mode of the device, a CSN timeout protection is activated and force the device to release the SPI bus. Then the serial data-out (SDO) will go into high-Z (high-Z). A reset of the CSN timeout (described as t_{SHCH} parameter in Table 48. Dynamic characteristics) is activated with a transition Low to High on CSN pin (or with a power on reset or software reset). With this reset, the serial data-out (SDO) is released and any valid communication will be accepted by the device. Without this reset, next communication is not taken into account by the device.

4.1.2 Connecting to the SPI bus

A schematic view of the architecture between the bus and devices can be seen in Figure 8. Bus master and two devices in a normal configuration.

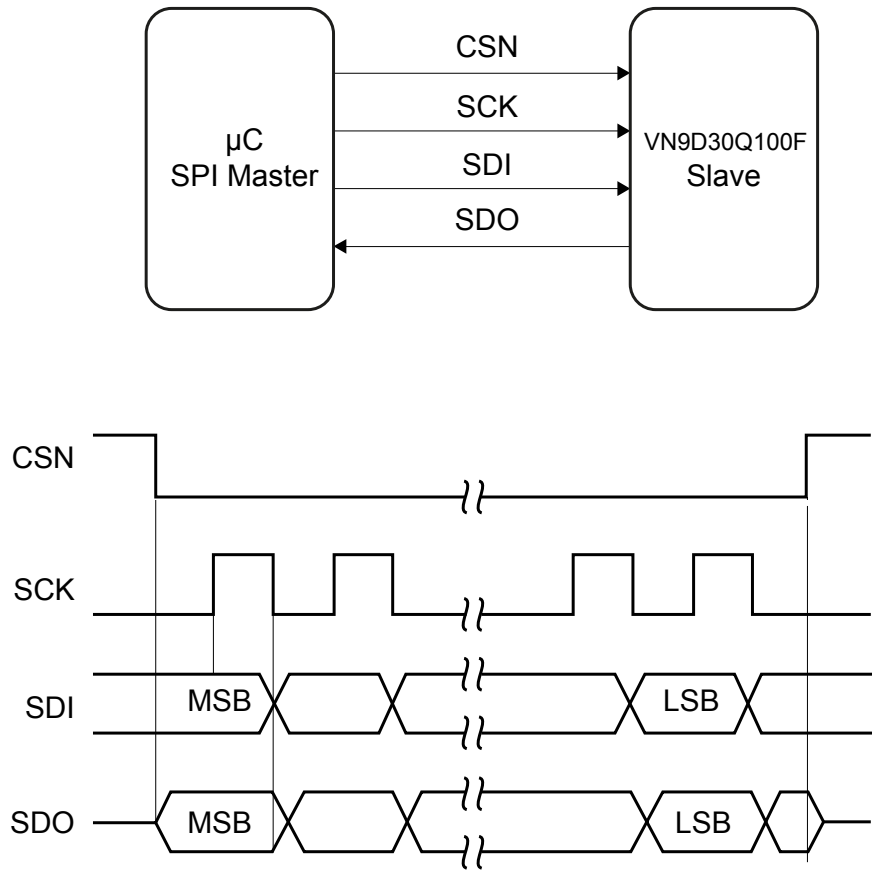
All input data bytes are shifted into the device, MSB first. The Serial Data Input (SDI) is sampled on the first rising edge of the Serial Clock (SCK) after Chip Select (CSN) goes low.

All output data bytes are shifted out of the device on the falling edge of SCK, MSB first on the first falling edge of the Chip Select (CSN).

4.1.3 SPI mode

Supported SPI mode during a communication phase can be seen in the following figure:

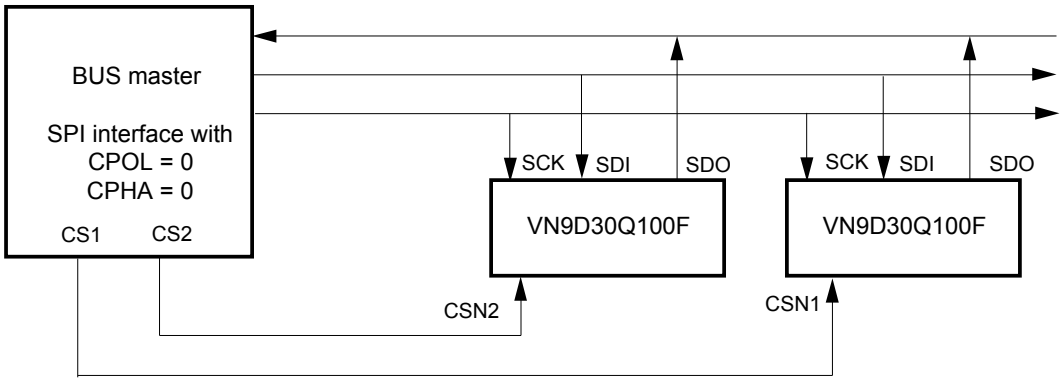
Figure 7. Supported SPI mode



This device can be driven by a micro controller with its SPI peripheral running in the following mode:

- CPOL = 0, CPHA = 0

Figure 8. Bus master and two devices in a normal configuration



4.2 SPI protocol

4.2.1 SDI, SDO format

SDI format during each communication frame starts with a command byte. It begins with two bits of operating code (OC0, OC1) which specify the type of operation (read, write, read and clear status, read device information) and it is followed by a 6-bit address (A0:A5). The command byte is followed by two input data bytes (D15:D8) and (D7:D0).

Table 12. Command byte

MSB							LSB
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 13. Input data byte 1

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 14. Input data byte 2

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0[1]

1. *D0 is the parity bit.*

SDO format during each communication frame starts with a specific byte called Global Status Byte (see Table 22. Global status byte for more details on bit0-bit7). This byte is followed by two output data bytes (D15:D8) and (D7:D0).

Table 15. Global status byte

MSB							LSB
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Table 16. Output data byte 1

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 17. Output data byte 2

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

4.2.2 Operating code definition

The SPI interface features four different addressing modes which are listed in Table 18. Operating codes.

Table 18. Operating codes

OC1	OC0	Meaning
0	0	Write operation
0	1	Read operation

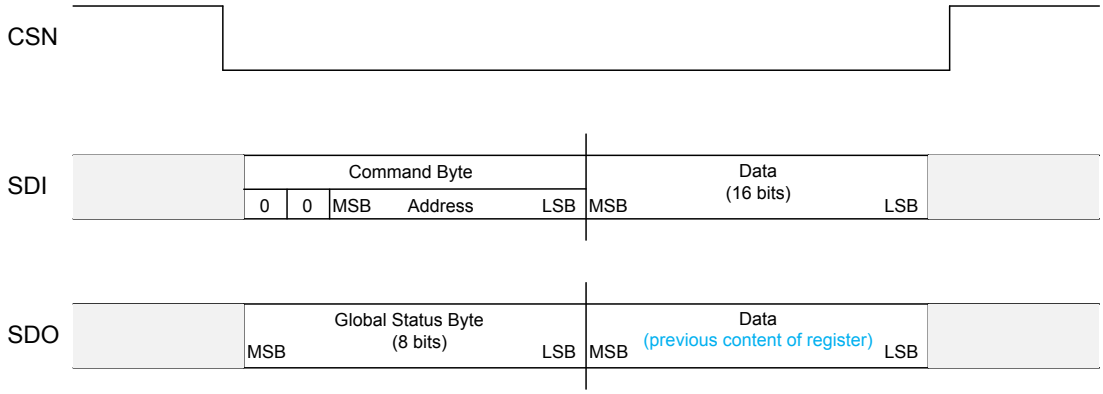
OC1	OC0	Meaning
1	0	Read and clear status operation
1	1	Read device information

Write mode

The write mode of the device allows to write the content of the input data byte into the addressed register (see list of registers in Table 23. RAM memory map). Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence the outgoing data are shifted out MSB first on the falling edge of the CSN pin and the subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte, second and third bytes to the previous content of the addressed register.

Figure 9. SPI write operation



GADG1010171330PS

Read mode

The read mode of the device allows to read and to check the state of any register.

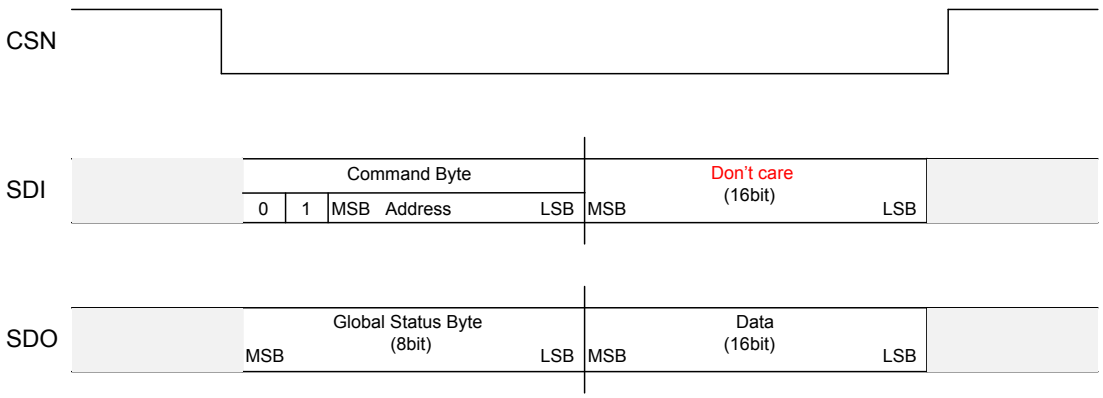
Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

The command byte allows to determine which register content is read, whilst the other two data bytes are "don't care".

In case of a read mode on an unused address, the global status/error byte on the SDO pin is followed by 0x0000 word.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during the SPI communication.

Figure 10. SPI read operation



GADG1010171333PS

Read and clear status command

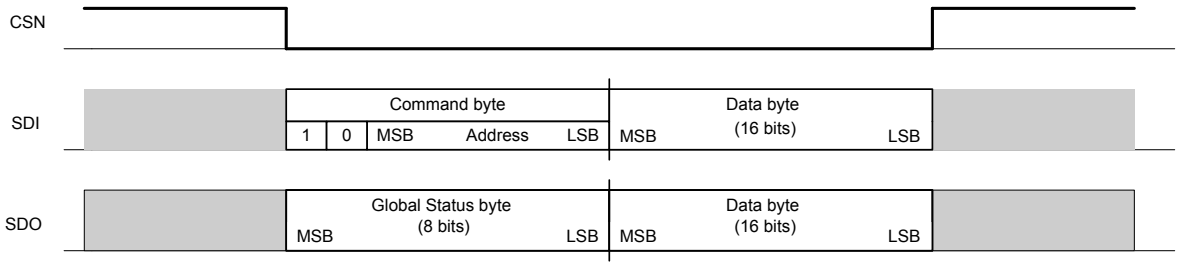
The read and clear status operation is used to clear the content of the addressed status register (see Table 23. RAM memory map). A read and clear status operation with address 0x3Fh clears all Status registers simultaneously.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read and the payload bits set to 1 into the data byte determine the bits into the register which have to be cleared.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte, second and third bytes to the content of the addressed register.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 11. SPI read and clear operation



Read device information

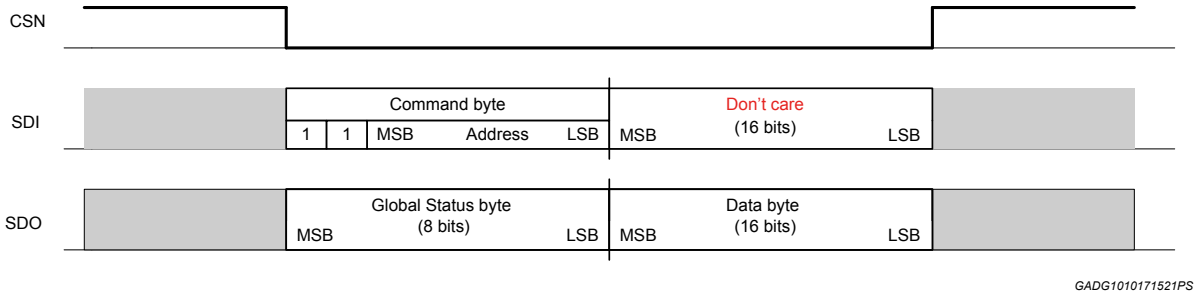
Specific information can be read but not modified during this mode. Accessible data can be seen in Table 24. ROM memory map.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read, whilst the other two data bytes are "don't care".

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte, second byte to the content of the addressed register and the third byte is 0x00.

Note: ROM is based on the 8-bit registers, then even if 16-bit are returned, only the second byte contains the addressed ROM register.

Figure 12. SPI read device information



4.2.3 Special commands

0xFF — SW-Reset: set all control registers to default

An Opcode ‘11’ (read device information) addressed at ‘111111’ forces a Software Reset of the device, second and third bytes are "don't care" provided that at least one bit is zero.

Note: An OpCode '11' at address '111111' with data field equal to '1111111111111111' on the SPI frame is recognized as a frame error and SPIE bit of GSB is set.

Table 19. 0xFF: SW_Reset

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	1	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care*

0xBF — clear all status registers (RAM access)

When an OpCode ‘10’ (read and clear operation) at address b’111111 is performed.

Table 20. Clear all status registers (RAM access)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	0	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care*

Note: Reset value = the value of the register after a power on.
Default value = the default value of the register. Currently this is equivalent to the Reset value.
Cleared register = explicitly read and clear of the register, if it is not write protected.

4.3 Register map

The device contains a set of RAM registers used for device configuration, the device status and ROM registers for device identification. Since ST-SPI is used, Global Status byte defines the device status, containing fault information.

4.3.1 Global status byte description

The data shifted out on SDO during each communication starts with a specific byte called global status byte. This one is used to inform the microcontroller about global faults that can happen at channel-side level (that is, like thermal shutdown, OLOFF...) or on the SPI interface (like watchdog monitoring timeout event, communication error,...). This specific register has the following format:

Table 21. Global status byte (GSB)

MSB							LSB
GSBN	RSTB	SPIE	TSD/OTOVL	T_{CASE}	LOFF	OLOFF	FS

Table 22. Global status byte

Bit	Name	Reset	Content
7	Global status bit not	0	The GSBN is a logically NOR combination of bit 0 to bit 6. This bit can also be used as the global status flag without starting a complete communication frame as it is present directly after pulling CSN low.
6	Reset bit	1	The RSTB indicates a device reset. In case this bit is set, all internal control registers are set to default and kept in that state until the bit is cleared. The reset bit is automatically cleared by any valid SPI communication
5	SPI error	0	The SPIE is a logical OR combination of errors related to a wrong SPI communication (SCK count and SDI stuck at errors). The SPIE bit is automatically set when SDI is stuck at High or Low. The SPIE is automatically cleared by a valid SPI communication.
4	Thermal shutdown (OT) or Power limitation (PL) or VDS	0	This bit is set in case of thermal shutdown, power limitation or in case of high VDS (VDS) at turn-off detected on any channel. The contribution of high VDS failure is maskable.
3	T_{CASE}	0	This bit is set if the frame temperature is greater than the threshold and can be used as a temperature prewarning. The bit is cleared automatically when the frame temperature drops below the case-temperature reset threshold (TCR).
2	Latch OFF (LOFF)	0	The device error bit is set in case when one or more channels are latched OFF
1	Open-load at off-state or output shorted to V_{CC} (OLOFF)	0	The open-load at the off state bit is set when an open-load off state or an output shorted to V_{CC} condition is detected on any channel
0	Fail-safe	1	The bit is set in case the device operates in fail-safe mode. A detailed description of these root-causes and the *fail-safe state* itself is specified in the paragraph *"Fail-safe mode"*

Note: The FFh or 00h combinations for the global status byte are not possible, due to the active low of the global status bit (bit 7), an exclusive combination exists between bit 7 and bit 0 - bit 6. Consequently, a FFh or 00h combination for the global status byte must be detected by the microcontroller as a failure (SDO stuck to GND or to V_{DD} or loss of SCK).

4.3.2 RAM

RAM registers can be separated according to the frequency of usage:

- Init - register is read/write during the initialization phase (single shot action)
- Continuous - read/write/read and clear registers often accessed, applying outputs control and diagnostic
- Rare - read/read and clear status of device registers accessed on demand (in case of failure)

Table 23. RAM memory map

Address	Name	Access	Content	Access type	Reset value
CONTROL REGISTERS					
00h	OUTCTRCR0	Read/Write	Output control configuration register channel 0	Init	0x0000
01h	OUTCTRCR1	Read/Write	Output control configuration register channel 1	Init	0x0000
02h	OUTCTRCR2	Read/Write	Output control configuration register channel 2	Init	0x0000
03h	OUTCTRCR3	Read/Write	Output control configuration register channel 3	Init	0x0000
04h	OUTCTRCR4	Read/Write	Output control configuration register channel 4	Init	0x0000
05h	OUTCTRCR5	Read/Write	Output control configuration register channel 5	Init	0x0000
08h	OUTCFGR0	Read/Write	Output configuration register 0	Init	0x0000
09h	OUTCFGR1	Read/Write	Output configuration register 1	Init	0x0000
0Ah	OUTCFGR2	Read/Write	Output configuration register 2	Init	0x0000
0Bh	OUTCFGR3	Read/Write	Output configuration register 3	Init	0x0000
0Ch	OUTCFGR4	Read/Write	Output configuration register 4	Init	0x0000
0Dh	OUTCFGR5	Read/Write	Output configuration register 5	Init	0x0000
10h	CHLOFFTCR0	Read/Write	Channel latch-off timing control register 0 (channels 2, 1, 0)	Init	0x0000
11h	CHLOFFTCR1	Read/Write	Channel latch-off timing control register 1 (channels 5, 4, 3)	Init	0x0000
13h	SOCR	Read/Write	Channel control register	Init	0x0000
14h	CTRL	Read/Write	Control register	Init	0x0000
... not used area					
STATUS REGISTERS					
20h	OUTSR0	Read/Clear	Output status register channel 0	Rare	0x0000

Address	Name	Access	Content	Access type	Reset value
21h	OUTSR1	Read/Clear	Output status register channel 1	Rare	0x0000
22h	OUTSR2	Read/Clear	Output status register channel 2	Rare	0x0000
23h	OUTSR3	Read/Clear	Output status register channel 3	Rare	0x0000
24h	OUTSR4	Read/Clear	Output status register channel4	Rare	0x0000
25h	OUTSR5	Read/Clear	Output status register channel 5	Rare	0x0000
28h	ADC0SR	Read	Digital current sense channel 0	Continuous	0x0000
29h	ADC1SR	Read	Digital current sense channel 1	Continuous	0x0000
2Ah	ADC2SR	Read	Digital current sense channel 2	Continuous	0x0000
2Bh	ADC3SR	Read	Digital current sense channel 3	Continuous	0x0000
2Ch	ADC4SR	Read	Digital current sense channel 4	Continuous	0x0000
2Dh	ADC5SR	Read	Digital current sense channel 5	Continuous	0x0000
31h	ADC9SR	Read	Digital frame temperature sense	Continuous	0x0000

Note: Any command (write, read, or read and clear status) executed on a “not used” RAM register, that is, a not assigned address, does not have any effect: there is no change in the global status byte (no communication error, no error flag). The data written to this address is ignored. The data read from this address contains 0000h, independent of what has been written previously to this address.

A write command on “don’t care” bits of an assigned RAM register address does not have any effect: there is no change on the global status byte. The data written to the “don’t care bits” is ignored. The content of the “don’t care bits” remains at “0” independent of the data written to these bits.

4.3.3 ROM

This memory is used for device identification.

Table 24. ROM memory map

Address	Name	Description	Access	Content
00h	Company code	Indicates the code of STMicroelectronics company	Read only	00H
01h	Device family	indicates the product family	Read only	01H
02h	Product code 1	Indicates the first code of the product	Read only	58H
03h	Product code 2	Indicates the second code of the product	Read only	56H
04h	Product code 3	Indicates the third code of the product	Read only	63H
0Ah	Version	Silicon version	Read only	42H
… not used area				
10h	SPI mode	Different modes of the SPI (see Section 4.1.3: SPI mode)	Read only	A1H
11h	WD type 1	Indicates the type of watchdog used in the product	Read only	46H
13h	WD bit position 1	Indicates the address of the register containing the WD toggle bit	Read only	40H
14h	WD bit position 2	Indicates the position of the WD toggle bit	Read only	C1H
… not used area				
20h	SPI CPHA	Indicates the polarity and phase of the SPI interface	Read only	55H
3Eh	GSB options	Options of GSB byte (standard GSB definition)	Read only	00H
3Fh	Advanced OP. code			

4.3.4 SPI Modes

By reading out the <SPI Mode> register general information of SPI usage of the Device Application Registers can be read.

Table 25. SPI Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Content
BR	DL2	DL1	DL0	SPI8	0	S1	S0	A1H

SPI Burst Read

Table 26. SPI Burst Read

Bit 7	Description
0	BR disabled
1	BR enabled

Burst Read is implemented in this product so this bit is enabled.

SPI Data Length

The SPI Data Length value indicates the length of the SCK count monitor which is running for all the accesses to the Device Application Registers. In case a communication frame with a SCK count is not equal to the reported one, the device will lead to a SPI Error and the data will be rejected.

The Frame Length is specified on 3 bits in the SPI Mode register located in the ROM part.

The 24-bit SPI communication is implemented in this product so these bits are ‘010’.

Table 27. SPI Data Length

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	
0	0	0	Invalid
0	0	1	16bit SPI
0	1	0	24bit SPI
...			…
1	1	1	64bit SPI

Data Consistency Check (Parity/CRC)

For some devices a Data Consistency Check is required. Therefore either a parity-check or for very sensitive systems a CRC may be implemented.

It is defined on 2 bits, in the SPI Mode register located in the ROM Part. A check is then applied on the incoming frame (SDI) while a calculation elaborated on one/multiple bits is done and integrated on the outgoing frame (SDO).

Table 28. SPI Data Consistency Check

Bit 1	Bit 0	Description
S1	S0	
0	0	not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

In case either the Parity or the CRC check is implemented it is always located at the end of the communication.

The device is equipped with the parity control check. In the Tx device, the parity bit is calculated based on first 23 bits: even number of "1" will set the parity bit to "1", whilst odd number of "1" will set the parity bit to "0". In the Rx device, parity bit is calculated in the same way and compared with the received one. In case of different parity bit, the received SPI frame is discharged.

4.4 Outputs control

Depending on the actual device mode, outputs can be controlled by the SPI register or the direct input DIx.

1. SPI register SOCR - in normal mode outputs can be turned ON/OFF, applying Bit[n] = 1/0

[n]: is the related channel, n = 0 for the channel 0, and n = 5 for channel 5

Example 1:

Turning ON channel 1 and 2 while turning OFF the others (without taking PWM or phase shifting into account)

Table 29. **Write SOCR 0x13**

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
0	0	0	0	1	1	0	1
D15	Data 1						D8
Not used	Not used	SOCR5	SOCR4	SOCR3	SOCR2	SOCR1	SOCR0
x	x	0	0	0	1	1	0
D7	Data 2						D0
Not used	Not used	Not used	Not used	Not used	Not used	WDTB	Parity
x	x	x	x	x	x	1/0	0

4.4.1 Procedure to turn on the outputs in PWM operations

PWM operation

The status of the output drivers is configured via the SPI output control register (SOCR), the direct input enable bit “DIENCRx” in the OUTCFGRx register and the PWM mode control bits, PWMFCY0 and PWMFCY1, in OUTCFGRx register. The DIENCR selects if the OUTPUTX outputs are controlled also by the direct inputs IN_x or only by the SOCR. The PWMFCY bit selects the channel frequency. Refer to the following Table 30 for details in normal mode.

Table 30. **Output control truth table**

DIENCR (OUTCFGRx)	INx	SOCRx	DUTYCR	OUTPUTx
0	X	0	X%	OFF
0	X	1	X%	PWM(1)
1	L	0	X%	OFF
1	L	1	X%	PWM (1)
1	H	X	X%	PWM (1)

1. *In case of DUTYCR = 100%, PWM = DC ON .*

Note: In normal mode, outputs can be driven by SPI commands or a combination of SPI commands and direct inputs IN_x.

Note: In fail-safe mode, the outputs are controlled by the direct inputs IN_x regardless of SPI commands. It is possible to apply the PWM through the DIx inputs. The PWM unit is not active in fail safe-mode, it is still possible to access the relevant registers and to configure them.

To turn on channels, information must be entered into the following registers:

- Select the PWM frequency by using the 2 bits PWMFCYx;
- Select the PHASE information by using the 5 bits CHPHAx;
- Select the switching slope by using the 2 bits SLOPECRx;
- Select the channels configuration Bulb/LED by using the bit CCR;
- Select the DUTYCYCLE information by using the 10 bits of the OUTCTRCRx registers;
- Select the channel through the dedicated register “SOCR” in the channel control register.
- Select the PWM triggering mode by using the single bit PWM_TRIG of the CTRL register

The PWMSYNC bit resets the internal 12 bits clock counter. This allows having a known time base and to synchronize different devices among each other.

The signal on the PWM_CLK is divided internally by a factor from 4096 to 512 depending on the PWMFCY register to generate the base frequency for the output.

- PWM signal is generated by properly selecting 10 of 12 bits on the clock counter. PWM engine has a virtual 10-bit granularity except when the PWM divider is set to 512, in this case only a 9-bit granularity is possible (LSB of 10-bit generated PWM is fixed to zero). Duty cycle step can be modified with the granularity related to the 9-bit register.

The duty cycle of the output signal is configured for each OUTPUTx with the OUTCTRCR register using 10 bits (MSB first).

- Programming an output duty cycle at 000h results in a 0% duty cycle that means the channel is always OFF depending on the SOCR/DIx bit setting.
- Programming an output duty cycle, at 3FFh results in a 100% duty cycle (4095/4096), that means the channel is always ON when the SOCR/DIx bit is set.
  - In normal mode the outputs are driven according to the SPI register setting and the INx pins (DIx in OR with SPI) if the related DIENCR bit is set.

Set PWMSYNC bit in the control register “CTRL” (to synchronize the internal PWM counter to the selected channels). The internal PWM counter has a 12 bits depth, it is active whatever the state of the channels if VDD > VDD_POR_ON. The setting of the PWMSYNC bit allows resetting the PWM counter.

Setting the PWM_TRIG bit in the control register “CTRL” forces the device to calculate the falling edge of the PWM window in advance compared with the end of the PWM period, while with a reset value for this bit, the rising edge of the PWM window will be calculated through a delay at the start of the PWM period.

- PWM_TRIG = 0 means channel switch on = PWM counter + phase shift counter (see examples 1 to 3)
- PWM_TRIG = 1 means channel switch off = PWM counter (max) - phase shift counter - duty cycle (see example 4)

The phase shift of the output signal is configured for each OUTPUTx by internally concatenating the CHPHAx 5 bits with '00000' in order to get 10 bits. Granularity of the phase shift is 5 bits. CHPHA = 00000b means a phase shift of 0 (internal 10bit phase shift is 0x000=0000000000b), while CHPHA = 11111b results in a maximum phase shift of 31/32 =(internal 10bit phase shift is 0x3E0=0000000000_b)

The phase shift is relative to the base frequency of the selected channel. Thus, the exact point in time when the channel switches on also depends on the operating mode of the selected channel.

Table 31. Phase shift configuration

Phase shift (%)	5 bits Register (H)	10 bits Register (H)	Phase shift (ms) PWM = 400 kHz Divider = 2048	Phase shift (ms) PWM = 400 kHz Divider = 1024	Phase shift (ms) PWM = 400 kHz Divider = 512
9.4	03	60	0.481	0.24	0.12
28.1	09	120	1.439	0.719	0.360
46.9	0F	1E0	2.40	1.2	0.6
75	17	2E0	3.84	1.92	0.96
90	1C	380	4.608	2.304	1.152

A change in phase/duty will be taken in account after the next zero-crossing of the PWM counter.

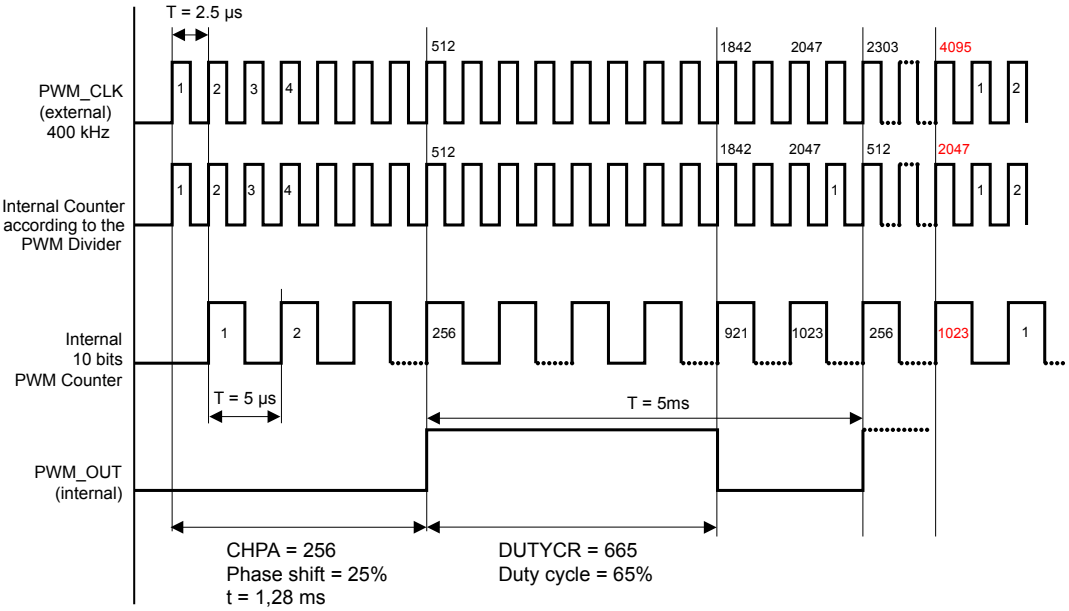
Note: If the frequency on PWM_CLK is too low (f < PWM_CLK), the device falls back to an internally generated PWM frequency of approximately 400 kHz. In this case, the PWMCLOCKLOW bit in OUTSRx is set.

Example 1:

Below, an example with a 65% duty cycle, PWM divider = 2048 and a 25% phase is given with a PWM sampling mode on the rising edge (PWM_TRIG=0):

- 65% duty cycle results in a DUTYCRx register content equal to 665 = Ch (65% x 1023 = 665 - 299).
- 25% phase results in a CHPA register content equal to 8 (25% x 31 = 8), equivalent to a content of 256 = 100h for a 10 bit register.
- With an input frequency at PWM_CLK pin of 400 kHz, the output frequency is 195 Hz.

Figure 13. **Resulting waveform 1**



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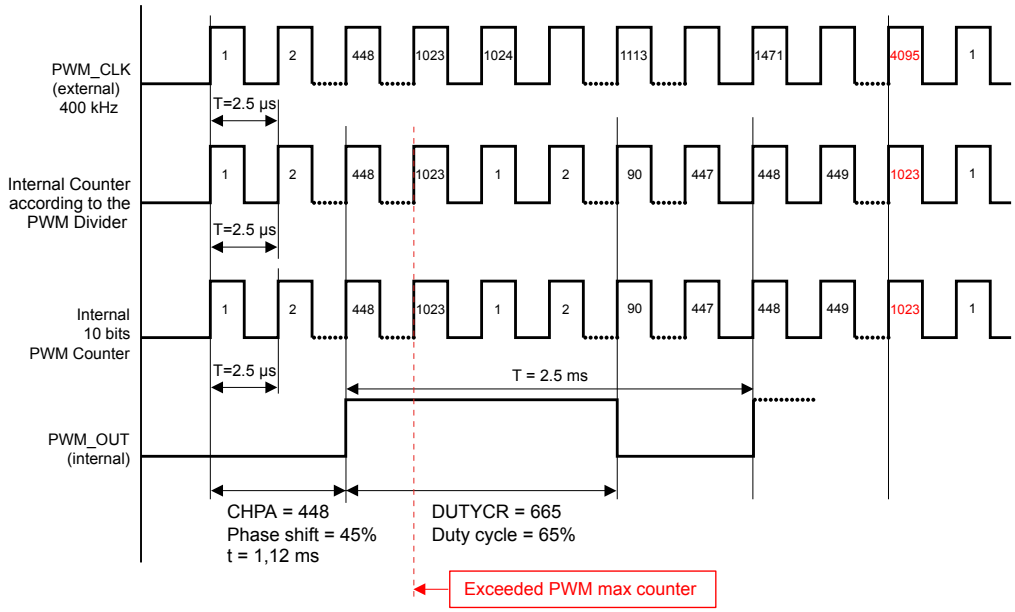
Example 2:

Below, an example with a 65% duty cycle, PWM divider = 1024 and a 45% phase is given with a PWM sampling mode on the rising edge (PWM_TRIG=0):

- 65% duty cycle results in a DUTYCRx register content equal to 665 = Ch (65% x 1023 = 665 - 299).
- 45% phase results in a CHPA register content equal to 14 (45% x 31 = 14), equivalent to a content of 448 = 1C0h for a 10 bit register.
- With an input frequency at PWM_CLK pin of 400 kHz, the output frequency is 390 Hz.

Figure 14. **Resulting waveform 2**



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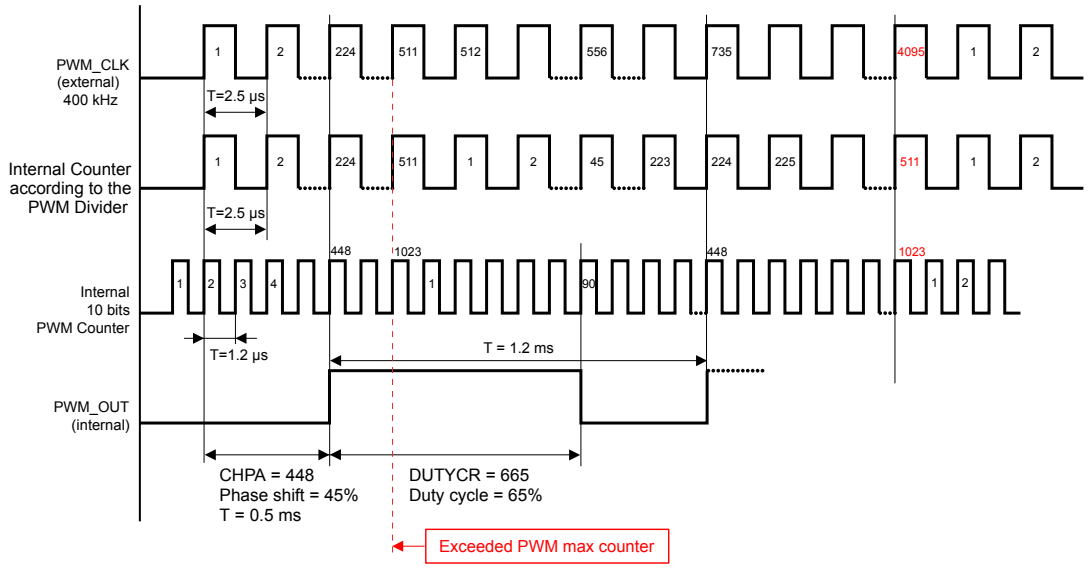
Example 3:

Below, an example with a 65% duty cycle, PWM divider = 512 and a 45% phase is given with a PWM sampling mode on the rising edge (PWM_TRIG = 0):

- 65% duty cycle results in a DUTYCRx register content equal to 665 = Ch (65% x 1023 = 665 - 299).
- 45% phase results in a CHPA register content equal to 14 (45% x 31 = 14), equivalent to a content of 448 = 1C0h for a 10 bit register.
- With an input frequency at PWM_CLK pin of 400 kHz, the output frequency is 781 Hz.

Figure 15. Resulting waveform 3



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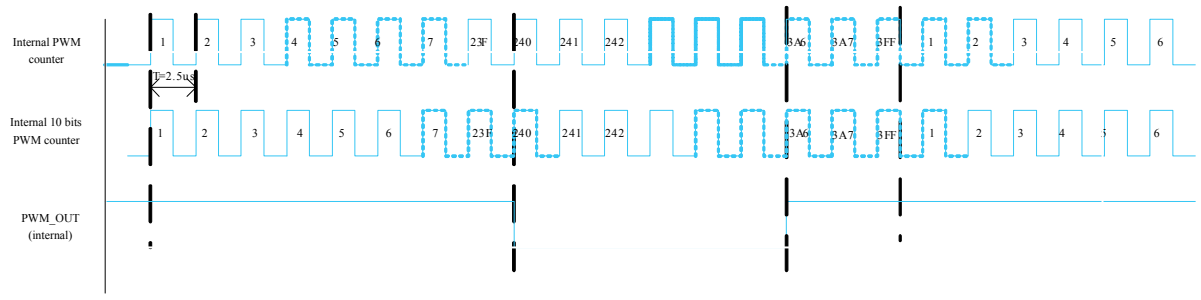
Example 4:

Below, an example with a 65% duty cycle, PWM divider = 512 and a 45% phase is given with a PWM sampling mode on the falling edge (PWM_TRIG=1):

- 65% duty cycle results in a DUTYCRx register content equal to 665 (65% x 1023 = 665) equivalent to a content of 299h.
- 45% phase results in a CHPA register content equal to 14 (45% x 31 = 14), equivalent to a content of 448 = 1C0h for a 10-bit register.
- With an input frequency at PWM_CLK pin of 400 kHz, the output frequency is 400/1024 = 390 Hz
- Due to PWM sampling mode on the falling edge, the PWM window has a start at 3A6h (not (299h +1C0h)) and a stop at 23Fh (not 1C0h).

Figure 16. Resulting waveform 4



4.4.2 OTP programming

The Direct Input assignment to Output through the OTP programming, is achievable by setting the two dedicated bits per channel in the OTP memory map according to the following table:

Table 32. OTP Memory Map

OTP memory map	bit 1, bit 0	bit 1, bit 0	bit 1, bit 0	bit 1, bit 0
	00	01	10	11
CH5	DI0	DI0	DI1	OFF
CH4	DI1	DI0	DI1	OFF
CH3	DI1	DI0	DI1	OFF
CH2	DI1	DI0	DI1	OFF
CH1	DI1	DI0	DI1	OFF
CH0	DI0	DI0	DI1	OFF

Note: "00" represents the default configuration.

The device is provided with the default configuration corresponding to the first column in the previous table (00). A customized OTP configuration, for each channel, is possible by changing the two dedicated bits.

Table 33. OTP programming

DIx assignment											
Ch5		Ch4		Ch3		Ch2		Ch1		Ch0	
bit 1	bit 0	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0
n	n	n	n	n	n	n	n	n	n	n	n

Each Output Status Register (OUTSRx) per channel contains the bits DIOTP1, DIOTP0 which reports the assigned direct input signal to the channel.

The OTP programming mode can be entered by applying a dedicated procedure in order to ensure a very high safety level for the stored configurations and to prevent from unwanted changing.

Further information about the OTP programming mode is provided in the dedicated user manual.

4.4.3 Procedure to turn-ON the outputs with the direct input DIx

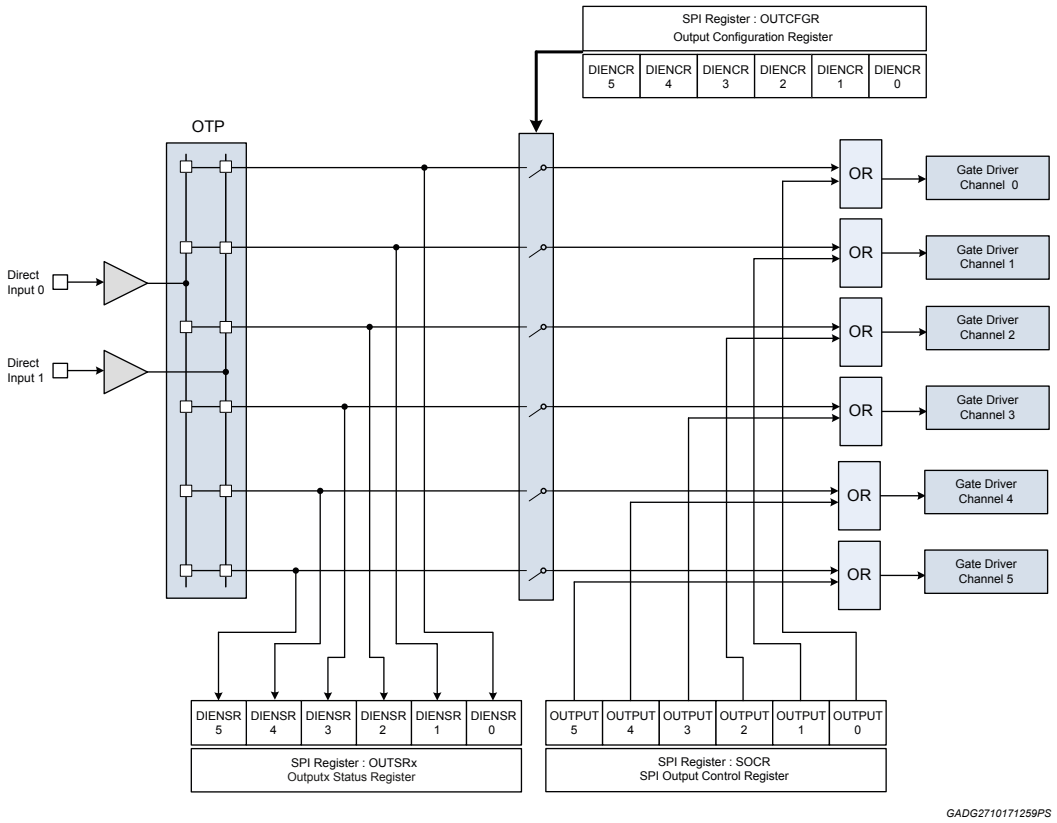
By applying logic level High/Low to pin, it turns ON/OFF the associated OTP selected outputs in fail-safe, standby and reset modes. In normal mode, DIx effect is ORed with SPI configuration when DIENCR bit is set. Then this truth table specifies the output state:

Table 34. Truth table

DIECRx	SOCRx	Related DIx logic status	OUTPUTx state
1	1	X	ON
1	0	L	OFF
1	0	H	ON
0	1	X	ON
0	0	X	OFF

The output channels can be configured to operate in bulb or LED mode using the channel control register (CCR). If the relevant bit in CCR is 0, the output is configured in bulb mode, if it is set to 1, the output is configured in LED mode (default value is 0).

Figure 17. **6-channel direct input block diagram**



4.5 Output switching slopes control

Output switching slopes are set by the two bits SLOPECR1, 2 in the OUTCFGCRx register (Address from 0x08h to 0x0Dh depending on the channel). The switching slopes are shown in the following table:

Table 35. **Switching slopes**

SLOPECRx	Channel 0,5 (V/µs)	Channel 1,2,3,4 (V/µs)
00	Standard	Standard
01	Fast	Fast
10	Faster	Faster
11	Fastest	Fastest

4.6 Control registers

OUTCTRCRx

Outputs control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	DUTYCR9	DUTYCR8	DUTYCR7	DUTYCR6	DUTYCR5	DUTYCR4	DUTYCR3	DUTYCR2	DUTYCR1	DUTYCR0	RESERVED	OLOFFCR	WDTB	PARITY
R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	R

Address: 0x00h to 0x05h

Type: RW

Reset: 0

Description: Outputs control register

[15:14]	RESERVED
[13:4]	DUTY_CR[9:0]: set the duty cycle value. Bit 9 (MSB) - Bit 0 (LSB)
[3]	RESERVED
[2]	OLOFFCR: enables an internal pull-up current generator to distinguish between the two faults: open-load OFF-state vs the output shorted to V_{CC} fault. 1: pull-up current generator enabled 0: pull-up current generator disabled
[1]	WDTB: watchdog toggle bit
[0]	PARITY: parity bit

OUTCFGRx

Outputs configuration register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOPECR1	SLOPECR0	RESERVED	CHPHA4	CHPHA3	CHPHA2	CHPHA1	CHPHA0	SPCR1	SPCR0	PWMFCY1	PWMFCY0	CCR	DIENCR	VDSMASK	PARITY
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R

Address: 0x08h to 0x0Dh

Type: RW

Reset: 0

Description: The “Output configuration register” allows setting the following important parameters for each channel:

- Switching related parameters
  - Switching slopes;
  - Phase of each channel;
  - PWM ratio;
- Channel configuration
  - Bulb/LED mode;
  - Control through SPI/DIx pins;
  - Masking the VDS control at turn-off;
- Diagnostic configuration
  - Set the current sampling point for the digital conversion;

[15:14]	SLOPECR[1:0]: Switching slope control bit 1 (MSB) and 0 (LSB)
[13]	RESERVED
[12:8]	CHPHA[4:0]: Set the Channel phase value[4:0] 00000: Resulting phase = 0/32 00001: Resulting phase = 1/32 .... 11110: Resulting phase = 30/32 11111: Resulting phase = 31/32
[7:6]	SPCR[1:0]: Current sampling Point[1:0] SPCR1:0 SPCR0:0 stop mode: authorizes digital conversion to be launched just before the end of on phase of the selected channel. SPCR1:0 SPCR0:1 START mode: authorizes digital conversion to be launched at each beginning of on phase of the selected channel. SPCR1:1 SPCR0:0 CONTINUOUS mode: authorizes digital conversion during all on phase of the selected channel. SPCR1:1 SPCR0:1 FILTERED mode: authorizes digital conversion like CONTINUOUS mode with the use of low pass filter to filter data coming from the conversion. It is useful at low level output current.

[5:4]	PWMFCY[1:0]: PWM frequency selection[1:0] Each output has a specific ratio for its PWM functionality. This mode is defined through two dedicated bits PWMFCY1 and PWMFCY0 of OUTCFGRx registers. PWMFCY1:0 PWMFCY0:0 = PWM freq ratio: 1024 PWMFCY1:0 PWMFCY0:1 = PWM freq ratio: 2048 PWMFCY1:1 PWMFCY0:0 = PWM freq ratio: 4096 PWMFCY1:1 PWMFCY0:1 = PWM freq ratio: 512 When a combination is selected, the output frequency of the selected channel will be the PWM clock input frequency divided by the defined ratio.
[3]	CCR: set the channel configuration (Bulb-LED) 0: Bulb mode 1: LED mode
[2]	DIENCR: Direct input signal enable in normal mode (according to OTP allocation) Each output has an OTP programmed direct input assignment for limp-home operation. Any output can be programmed to be always OFF in the limp-home, or according to DI0 pin state or according to DI1 pin state. This programmed assignment can be read from DIOTP bits of OUTSRx status register. When DIENCR bit is set, DIx pin state assigned to the output is ORed with the SOCR/PHASE/DUTYCYCLE combination to control output state. In fail-safe, standby and reset modes applying log.1/0 to pin turns ON/OFF the associated OTP selected outputs.
[1]	VDSMASK: VDS detection at turn-off masking bit
[0]	PARITY: parity bit

CHLOFFTCR0

Channel Latch OFF Timer Control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHLOFFTCR23	CHLOFFTCR22	CHLOFFTCR21	CHLOFFTCR20	CHLOFFTCR13	CHLOFFTCR12	CHLOFFTCR11	CHLOFFTCR10	CHLOFFTCR03	CHLOFFTCR02	CHLOFFTCR01	CHLOFFTCR00	RESERVED	RESERVED	RESERVED	PARITY
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R

Address: 0x10h

Type: RW

Reset: 0

Description: The output behavior in case of power limitation or thermal shut-down is programmable, as latch-off or Time limited auto-restart (tblanking). The default mode is the latch-off one which corresponds to have 0x0h in the register. In Time limited autorestart, when the channel is turned ON, after a transition from 0 to 1 of the corresponding SOCR bit or activation through associated DIx input when DIENCR bit is set, power limitation and thermal shutdown latches are inhibited for a programmed tblanking time.

See Section 6: Programmable blanking window (PBW) for more details.

Two Registers are used for setting the $t_{blanking}$ values for each channel:

- CHLOFFTCR0 for channels 2,1,0;
- CHLOFFTCR1 for channel 5,4,3.

[15:12]	CHLOFFTCR[23:20]: It configures the output behavior in case of power limitation for the corresponding channel 2.
[11:8]	CHLOFFTCR[13:10]: It configures the output behavior in case of power limitation for the corresponding channel 1.
[7:4]	CHLOFFTCR[03:00]: It configures the output behavior in case of power limitation for the corresponding channel 0.
[3:1]	RESERVED
[0]	PARITY: parity bit

CHLOFFTCR1

Channel Latch OFF Timer Control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHLOFFTCR53	CHLOFFTCR52	CHLOFFTCR51	CHLOFFTCR50	CHLOFFTCR43	CHLOFFTCR42	CHLOFFTCR41	CHLOFFTCR40	CHLOFFTCR33	CHLOFFTCR32	CHLOFFTCR31	CHLOFFTCR30	RESERVED	RESERVED	RESERVED	PARITY
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R

Address: 0x11h

Type: RW

Reset: 0

Description: The output behavior in case of power limitation or thermal shut-down is programmable, as latch-off or Time limited auto-restart (tblanking). The default mode is the latch-off one which corresponds to have 0x0h in the register. In Time limited autorestart, when the channel is turned ON, after a transition from 0 to 1 of the corresponding SOCR bit or activation through associated DIx input when DIENCR bit is set, power limitation and thermal shutdown latches are inhibited for a programmed tblanking time.

See Section 6: Programmable blanking window (PBW) for more details.

Two Registers are used for setting the $t_{blanking}$ values for each channel:

- CHLOFFTCR0 for channels 2,1,0;
- CHLOFFTCR1 for channel 3.

[15:12]	CHLOFFTCR[53:50]: It configures the output behavior in case of power limitation for the corresponding channel 5.
[11:8]	CHLOFFTCR[43:40]: It configures the output behavior in case of power limitation for the corresponding channel 4.
[7:4]	CHLOFFTCR[33:30]: It configures the output behavior in case of power limitation for the corresponding channel 3.
[3:1]	RESERVED
[0]	PARITY: parity bit

The blanking window duration in case of power limitation or thermal shutdown events can be set according to the following table:

Table 36. Programmable $t_{blanking}$ values

CHLOFFTCRx3	CHLOFFTCRx2	CHLOFFTCRx1	CHLOFFTCRx0		
0	0	0	0	0x0	latch OFF cfg (default)
0	0	0	1	0x1	16ms
0	0	1	0	0x2	32ms
.	.	.	.		
1	1	1	0	0xE	224ms
1	1	1	1	0xF	240ms

SOCR

Channel control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	SOCR5	SOCR4	SOCR3	SOCR2	SOCR1	SOCR0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	WDTB	PARITY
R	R	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	RW	R

Address: 0x13h

Type: RW

Reset: 0

Description: The SOCR register is used to turn ON/OFF the related channel. The WDTB bit that must be toggled within t_{WDBT} (watchdog timeout) to avoid entering in fail-safe mode. This bit is already present in the output control register and it is duplicated in the SOCR register to simplify the SPI usage.

[15:14]	RESERVED
[13]	SOCR5 bit controls output state of channel 5 1 - output enabled 0 - output disabled
[12]	SOCR4 bit controls output state of channel 4 1 - output enabled 0 - output disabled
[11]	SOCR3 bit controls output state of channel 3 1 - output enabled 0 - output disabled
[10]	SOCR2 bit controls output state of channel 2 1 - output enabled 0 - output disabled
[9]	SOCR1 bit controls output state of channel 1 1 - output enabled 0 - output disabled
[8]	SOCR0 bit controls output state of channel 0 1 - output enabled 0 - output disabled
[7:2]	RESERVED
[1]	Watchdog toggle bit
[0]	PARITY: parity bit

CTRL

Control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	PWM_TRIG	RESERVED	RESERVED	RESERVED	LOCKEN4	LOCKEN3	LOCKEN2	LOCKEN1	LOCKEN0	PWMSYNC	PARITY
RW	RW	RW	RW	RW	RW	R	R	R	RW	RW	RW	RW	RW	W	R

Address: 0x14h

Type: RW

Reset: 0

Description: Control register

[15]	GOSTBY: Go to standby. It is necessary to do 2 write accesses to enter standby: 1. Write UNLOCK = 1 2. Write GOSTBY = 1 and EN = 0
[14]	UNLOCK: unlock bit UNLOCK bit allows protected SPI transactions. It means that the next SPI communication will automatically clear this bit and prevent any change of protected data (like slope control or BULB/LED mode for example). As a consequence, modifying a protected data requires to set UNLOCK bit in a first communication and write the protected data during the next communication.
[13:12]	CTDTH[1:0]: Case thermal detection threshold. These bits allow to configure the case thermal detection of the device. Three temperature thresholds are available by programming these two bits. 1. CTDTH1:0 CTDTH0:0 = detection temperature:120 °C 2. CTDTH1:0 CTDTH0:1 = detection temperature:130 °C 3. CTDTH1:1 CTDTH0:X = detection temperature:140 °C
[11]	EN: enter normal mode 1: normal mode 0: fail-safe mode It is necessary to do 2 write accesses to enter normal mode: 1. Write UNLOCK = 1 2. Write EN = 1
[10]	PWM_TRIG: PWM triggering mode 0: PWM trigger according to the rising edge of PWM period and phase shift configuration 1: PWM trigger according to the falling edge of PWM period and phase shift configuration
[9:7]	RESERVED
[6:2]	LOCKEN[4:0]: Protected transaction mode LOCKEN4: Lock enable for slope control SLOPECRx LOCKEN3: Lock enable for BULB/LED mode CCRx LOCKEN2: Lock enable for phase shift CHPHAx LOCKEN1: Lock enable for configurable blanking time CHLOFFTCRx LOCKEN0: Lock enable for PWM clock synchronization When the bit is set (LOCKENx = 1), it is used to have a protected transaction: • setting UNLOCK bit • modify the relevant configuration register When LOCKENx=0 (reset value), the related configuration registers are altered with a simple write command.

[1]	PWMSYNC: PWM clock synchronization. PWMSYNC =1 clears PWM internal counter. It automatically resets at next SPI communication
[0]	PARITY: parity bit

OUTSRx

Output status channels 0 to 5 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIENSR	DIOTP1	DIOTP0	CHFBSRx	VDSFSRx	STKFLTRx	OLPUSRx	CHLOFFSRx	RST	SPIE	PWMCLOCKLOW	VCCUV	RESERVED	RESERVED	RESERVED	PARITY
R	R	R	RC	RC	RC	R	R	RC	RC	RC	R	R	R	R	R

Address: 0x20h to 0x25h

Type: RC

Reset: 0

Description: The output status register reports the status of the selected channel based on the configuration register and in case of fault condition.

[15]	DIENSR: direct input status, image of associated DI logic level according to OTP allocation.
[14]	DIOTP1: associated DIx input description bit 1
[13]	DIOTP0: associated DIx input description bit 0
[12]	CHFBSRx: channel feedback status. Channel feedback status. Combination of power limitation, OT, OVERLOAD detection (VDS at turn-off). The CHFBSRx provides a logical "OR" combination of VDS (overload), PL (power limitation), OT (overtemperature) failure flags related to OUTPUTx, and it is cleared by a read and clear command.
[11]	VDSFSRx: VDS feedback status. This bit is ‘1’ if VDS is high at turn-off, indicative of a potential overload condition
[10]	STKFLTRx: output stuck to V_{CC}/open-load off state status.
[9]	OLPUSRx: output pull-up generator status.
[8]	CHLOFFSRx: channel latch-off status. This bit is set when overload blanking time has elapsed and the channel is latched off.
[7]	RST: chip reset
[6]	SPIE: SPI error
[5]	PWMCLOCKLOW: PWM clock frequency too low.
[4]	VCCUV: V_{CC} undervoltage
[3:1]	RESERVED
[0]	PARITY: parity bit

ADCxSR

Digital Current Sense register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	ADCxSR9 (MSB)	ADCxSR8	ADCxSR7	ADCxSR6	ADCxSR5	ADCxSR4	ADCxSR3	ADCxSR2	ADCxSR1	ADCxSR0 (LSB)	RESERVED	SOCRx	UPDTSR	PARITY
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0x28h to 0x2Dh

Type: R

Reset: 0

Description: The register contains the digital value of the current flowing on the selected channel. It reports the result of the digital current conversion. It is updated according to the modes set by the two bits (SPCR1 and SPCR0) of the OUTCFGRx.

[15:14]	RESERVED
[13:4]	ADCxSR[9:0]: The 10 bit register contains the digital value of OUTPUTx current. ADCxSR9 (MSB) ADCxSR0 (LSB)
[3]	RESERVED
[2]	SOCRx: SOCR Bit controls output state of channel x. 1 - output enabled 0 - output disabled
[1]	UPDTSR: updated status bit. This bit is set when a value is updated and cleared when register is read.
[0]	PARITY: parity bit

ADC9SR

Digital Case Thermal Sensor Voltage register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	ADC9SR9 (MSB)	ADC9SR8	ADC9SR7	ADC9SR6	ADC9SR5	ADC9SR4	ADC9SR3	ADC9SR2	ADC9SR1	ADC9SR0 (LSB)	RESERVED	RESERVED	UPDTSR	PARITY
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0x31h

Type: R

Reset: 0

Description: The register contains the result of the digital conversion of the case temperature.

[15:14]	RESERVED
[13:4]	ADC9SR[9:0]: The 10 bit register contains the digital value of case temperature sensor voltage. ADC9SR9 (MSB) ADC9SR0 (LSB) T_{CASE} (typ.) = 401.8 °C -1.009 * ADC9SR[13:4]
[3:2]	RESERVED
[1]	UPDTSR: updated status bit. This bit is set when a value is updated and cleared when register is read.
[0]	PARITY: parity bit

OTP memory map (Reserved)

OTP is automatically read into registers at Reset.
OTP memory map contains Direct Inputs assignment to outputs,
Direct Inputs assignment data (2 bits per channel):

Table 37. OTP memory map (reserved)

DIx assignment bit 1	DIx assignment bit 0	CH5	CH4	CH3	CH2	CH1	CH0
0	0	DI0	DI1	DI1	DI1	DI0	DI0
0	1	DI0	DI0	DI0	DI0	DI0	DI0
1	0	DI1	DI1	DI1	DI1	DI1	DI1
1	1	OFF	OFF	OFF	OFF	OFF	OFF

5 Diagnostic

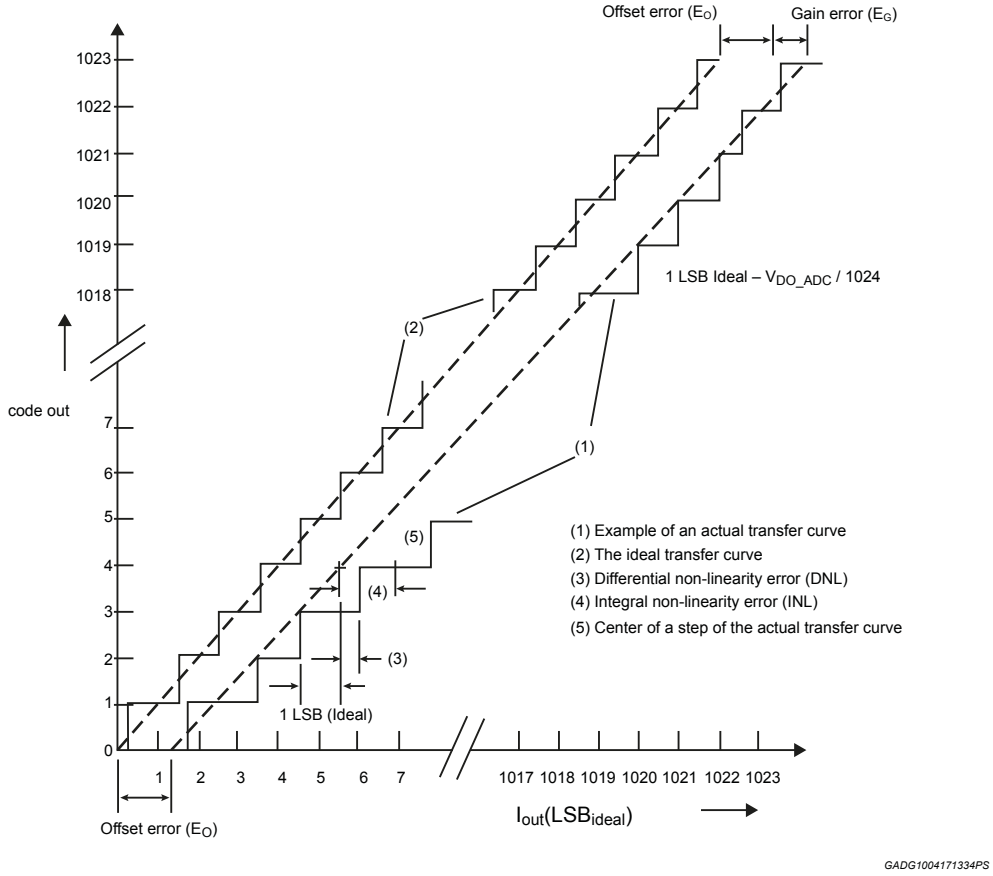
The device is capable of providing digital diagnostic information through the SPI interface.

5.1 Digital current sense diagnostic

5.1.1 ADC characteristics

Here are “Differential nonlinearity” and “Integral nonlinearity” typical curves for the 10-bit ADC converter.

Figure 18. ADC characteristics and error definition



5.1.2 ADC operating principle

The device provides a 10-bit successive approximation register (SAR) analog-to-digital converter. It is used to provide a digital information about the current sense feedback proportional to the output current and the temperature read by the internal sensor. An integrated LP (progressive average) filter can be used to filter data coming from the ADC conversion reducing the effect of random noise coming from the analog current sense amplifier.

Note: The internal ADC is able to work in both normal and fail-safe conditions.

The integrated ADC control logic is designed to lead to a good 10-bit approximation of current sense/temperature feedback.

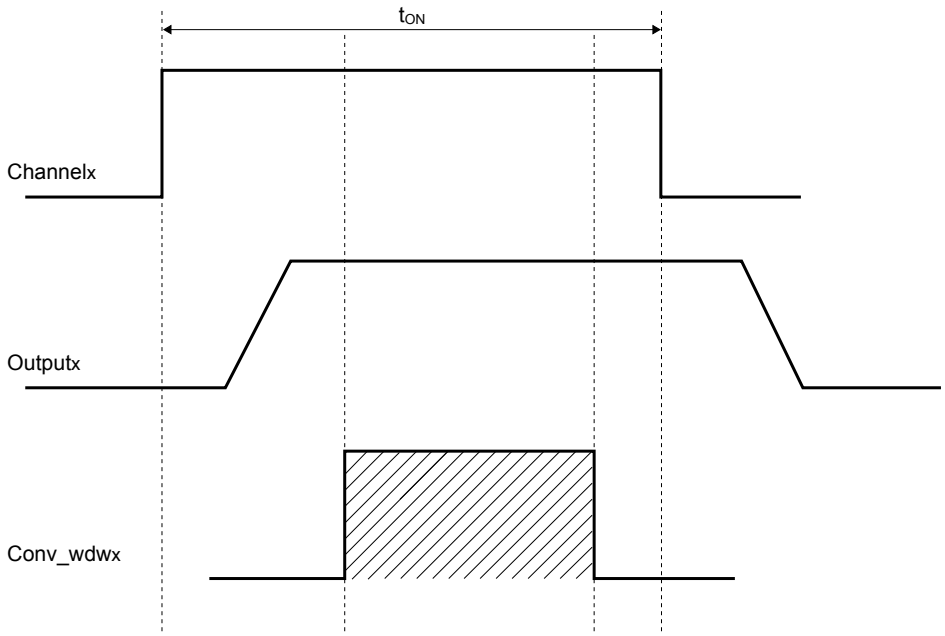
After each conversion, an updated bit “UPDTSR” is set to advise about new conversion data. This bit is reset after the Read process of the dedicated RAM register.

The data is maintained in the register until the next conversion results are available. The ADC register is refreshed at the end of each conversion and maintained during the conversion of the current sample. The data is converted on the 10-bit register, the formula is equal to:

Iout_conv = data (10bit)/K;

An analog multiplexer has been implemented to connect the different channels to the amplifier and the ADC block. Due to the current sense amplifier settling time when switching from the current sense mode of one channel, to the current sense mode of another channel, a priority management is implemented to control the time when the data conversion can be done in a safe/stable way and to arbitrate the concurrent ADC sampling requests (see next figures).

Figure 19. Conversion window generation



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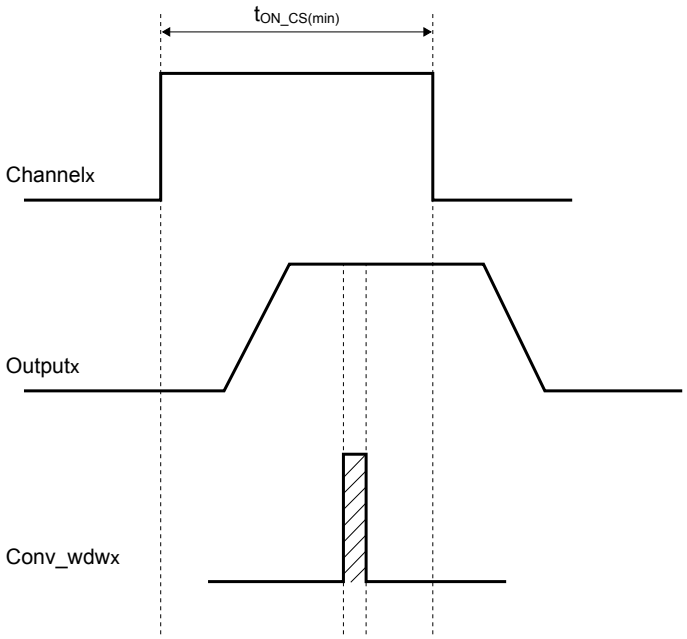
A minimum conversion time ($t_{ON\_CS(min)}$) is defined to allow the signal stabilization at the input of the ADC converter and considering the sampling time. The user should manage the phase shift in a way that maximum two channels can be sampled in the same time window.

Figure 20. Minimum ON time for digital current sense availability



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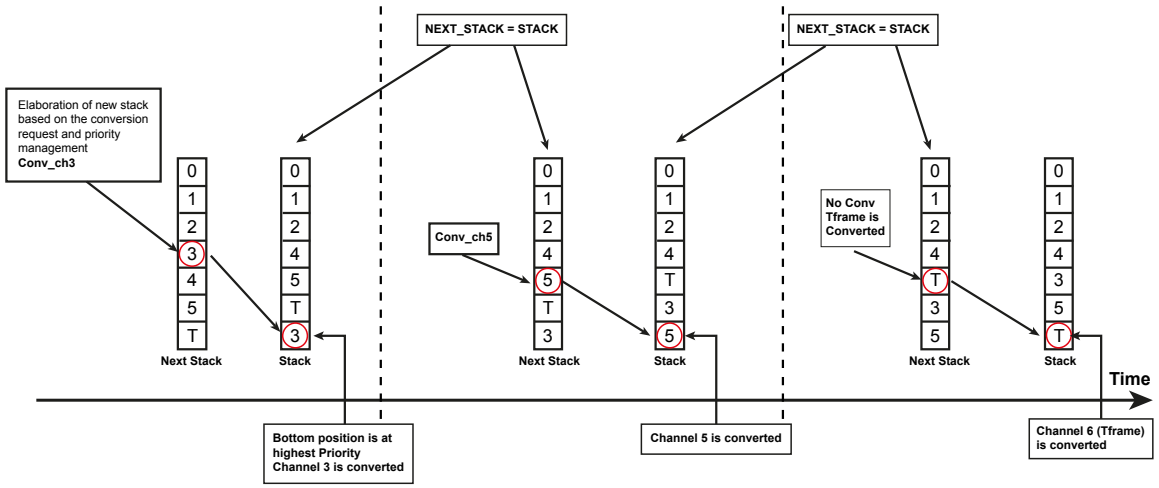
The sequence of channels to be converted is managed through an internal stack:

- Stack size is equal to the number of channels plus frame temperature sensor
- A conversion of the selected channel is done based on the information stored at the end of the stack (see Figure 21. Channel's sequence internal stack)
- After the reset of the device or when no channels are active, the conversion of the frame temperature sensor is done continuously
- When the conversion of a channel_x has to start, the channel_x is moved to the end of the stack while the other remaining channels are moved up

Figure 21. Channel's sequence internal stack



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Note: The figure above shows an example of how the priority is managed through a stack in a six channels device.

5.1.3 Registers

The results of the digital conversion are stored in the “Digital Current Sense Registers” Two registers are used for the digital conversion of the output current and case sense temperature respectively:

- **ADCxSR** (address from 28h to 2Dh) - for digital Outputx current (one register x channel)
- **ADC9SR** (address 31h) - Digital case temperature sensor voltage sense register

Table 38. Status registers

Register Name	Bit 15,14	Bit 13..4	Bit 3	Bit 2	Bit 1	Bit 0
ADCxSR 28h to 2Dh	Not Used	Digital Value of OUTx current	Not Used	SOCRx Possibility to control the Outx state (Read only)	UPDTSR Updated status bit. It is set when value is updated and cleared when register is read	Parity
ADC9SR 31h	Not Used	Digital Value of case temperature sensor voltage	Not Used	Not Used	UPDTSR Updated status bit. It is set when value is updated and cleared when register is read	Parity

5.1.4 Synchronous, Asynchronous Modes

5.1.4.1 Normal Mode

The ADC conversion can work in 4 different sampling modes (start, stop, continuous or filtered) according to the table below:

Two bits per channel “SPCR1” and “SPCR0” allocated in the Output Configuration Register “OUTCFGRx”, allow 4 different sampling modes:

Table 39. Sampling mode configuration

SPCR1	SPCR0	Sampling Mode
0	0	STOP Mode
0	1	START Mode
1	0	CONTINUOUS Mode
1	1	FILTERED Mode

5.1.4.2 Synchronous Mode

Synchronous Mode in PWM condition

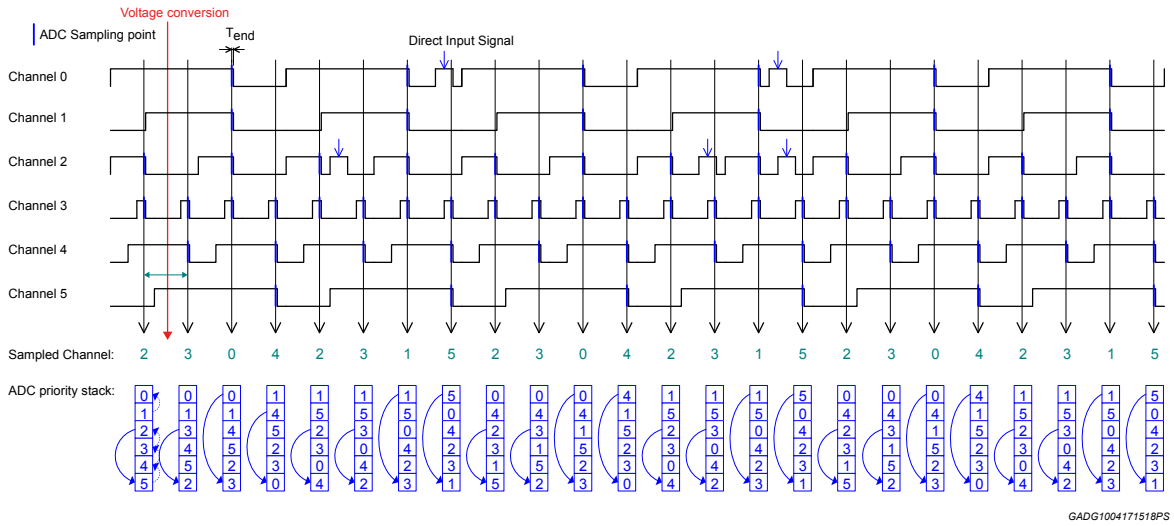
- Sampling is done according to the PWM rising and falling edge (see Figure 22. Sequence of channels). See Table 39. Sampling mode configuration for more details about the registers configuration.
- The sampling will be always assigned at the highest priority.

Registers Configuration

- SPCR10=0h: Synchronous triggered by falling edge of PWM. Conversion is executed on the rising edge of the conversion window (see Figure 22. Sequence of channels);
- The ADC real sampling is managed to trigger the sampling point with margin versus falling edge.
- SPCR10=1h: Synchronous triggered by rising edge of PWM signal. Conversion is executed on the falling edge of the conversion window (see Figure 22. Sequence of channels).

Note: The ADC real sampling is managed to trigger the sampling point with margin versus rising edge.

Figure 22. Sequence of channels



5.1.4.3 *Asynchronous mode*

In asynchronous mode the ADC result register is continuously refreshed, provided that the channel is commanded either through the direct input signal or the SOCR register. Conversion is executed during the complete conversion window except for the priority arbitration.

Since the ADC register is continuously refreshed, its conversion priority is always lower than the sampled channels.

Once the PWM counter reaches a value for which synchronous diagnostic of another channel is requested, the internal MUX switches to this channel and serves the ADC sampling request (channels in synchronous mode have higher priority compared to those in asynchronous mode). Once this sampling is completed the MUX switches back to the asynchronous sampling channel, provided that no higher priority sampling requests from other channels occur. If two or more channels are configured in asynchronous mode, the MUX will sequentially switch through those channels, always interrupted when higher priority synchronous sampling requests occur.

The thermal case sampling has always low priority for the ADC conversion and so it can be interrupted by any channel in sample mode.

Registers configuration:

SPCR10 = 2h and SOCRx = 1: asynchronous with continuous sampling:

Asynchronous mode, the ADC result register is continuously refreshed, provided that the channel is commanded either through the direct input signal or the SOCR register. Conversion is executed during the complete conversion window except for the priority arbitration. Since the ADC register is continuously refreshed, its conversion priority is always lower than sampled channels.

SPCR10 = 3h and SOCRx = 1: asynchronous with continuous sampling and digital LP filter:

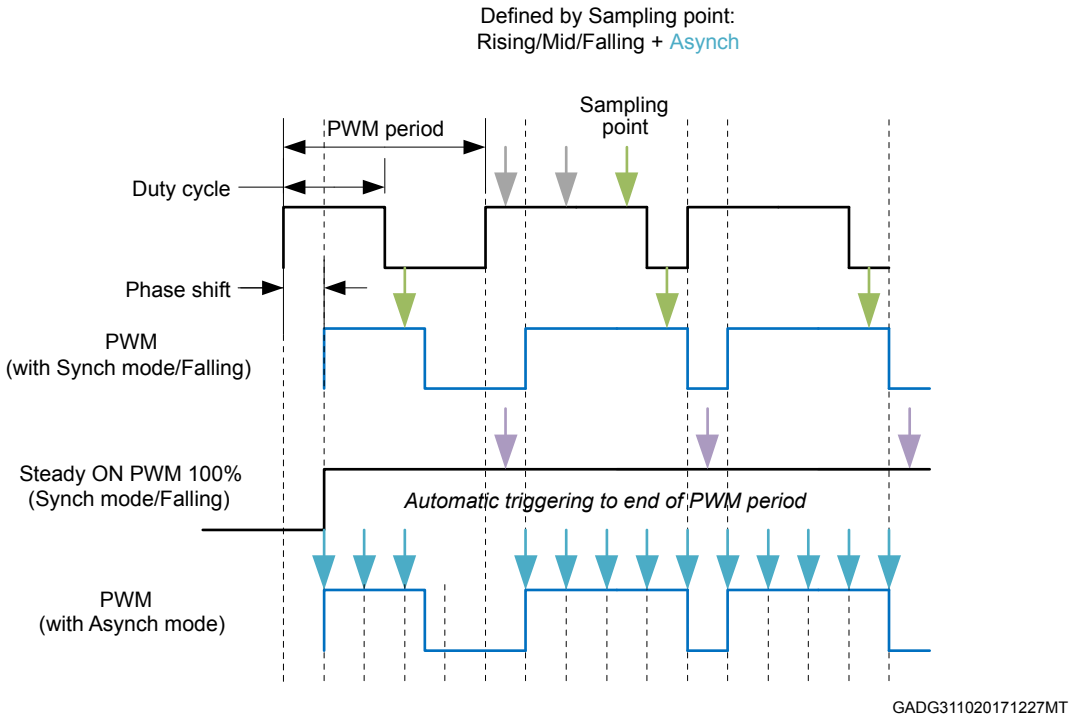
- The integrated LP filter is activated
- This component filters data coming from the ADC conversion reducing the effect of random noise coming from the analog current sense amplifier

SPCR10 = 3h, SOCRx = x and DIx = high: if a channel is commanded off through SOCR, but commanded on through the direct input, the asynchronous sampling mode is forced - asynchronous with continuous sampling.

The thermal case sampling has always low priority for the ADC conversion, and so it can be interrupted by any channel in simple mode. Thermal case conversion is always in asynchronous continuous mode. In fail-safe condition the ADC conversion is always in asynchronous/continuous mode.

- Conversion is executed during the complete conversion window.
- No priority management is applied, channels are converted according to their position in the stack. No interruption and no priority management are possible. In the case of multiple channels active at the same time, the conversion starts with the first one in the stack.

Figure 23. Asynchronous with continuous sampling



5.1.4.4 *Sampling concept*

- PWM mode (internal engine) → All the synchronous modes are available (start, stop, continuous or filtered)
- DC mode (internal engine) → ADC works in Continuous Mode. The conversion window follows the channel control input signal
  - DC mode by/without DI: No difference, since this condition is equivalent to PWM with 100% of duty (the sampling will be always in continuous mode).
- PWM mode by DI (external source) → the DIx information is combined (O-red) with the channel control signal. Sampling will be executed according to the PWM mode settings.
  - With SPCRx=2h,3h, sampling is possible (continuous/filtered mode).

5.1.4.5 *Synchronous mode in DC condition (PWM with 100% duty cycle)–equivalent to asynchronous mode*

This mode is equivalent to the asynchronous mode.

Table 40. ADC configuration registers

SOCrx	DIx	DutyCrx	SPCR1,0	Conversion mode	Feedback type
1	X	X	00	Synchronous triggered by falling edge on the internal PWM signal	Output current
1	X	X	01	Synchronous triggered by rising edge of the internal PWM signal	Output current
1	X	X	10	Asynchronous with continuous sampling	Output current
1	X	X	11	Asynchronous with continuous sampling and digital LP filter	Output current
0	1	X	X	(Fail-safe mode) Asynchronous with continuous sampling	Output current
X	X	X	X	Tframe conversion (Always lower priority than current sampled modes)	Tframe sensor voltage

5.2 Integrated LP (progressive average) filter

In asynchronous mode, when the filtered mode is selected through the dedicated bits “SPCR1 = 1” and “SPCR0 = 1”, the integrated LP filter is activated. This component filters the data coming from the ADC conversion reducing the effect of random noise coming from the analog current sense amplifier.

Features of the integrated LP filter:

- First order LP filter on 16 samples
- First result after one sample with progressive averaging of 16 successive samples

$$data\ (N) = \left(data\ (N-1) \cdot \frac{15}{16}\right) + data_i/16$$

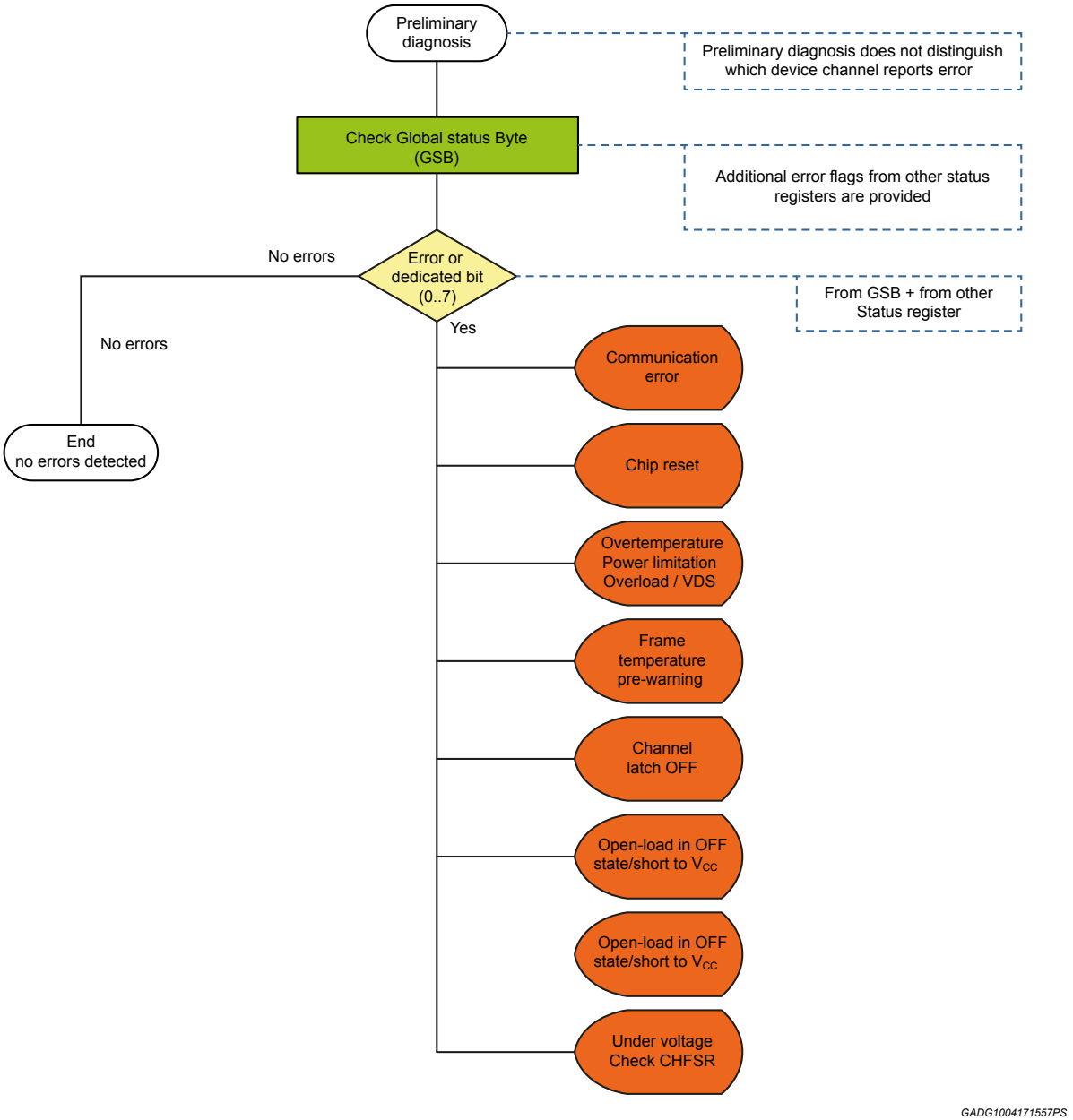
- Continues to accumulate samples during the PWM operation
- Keeps digitalized value when the channel is turned off

5.3 Digital diagnostic

The global status byte (GSB) provides preliminary status of the device every the SPI communication with the device. It informs about the device actual mode (normal/fail-safe).

By reading the additional status registers, more detailed information is provided. Status information is stored in the status registers.

Figure 24. Status registers



5.3.1 Status registers

Table 41. **Status registers**

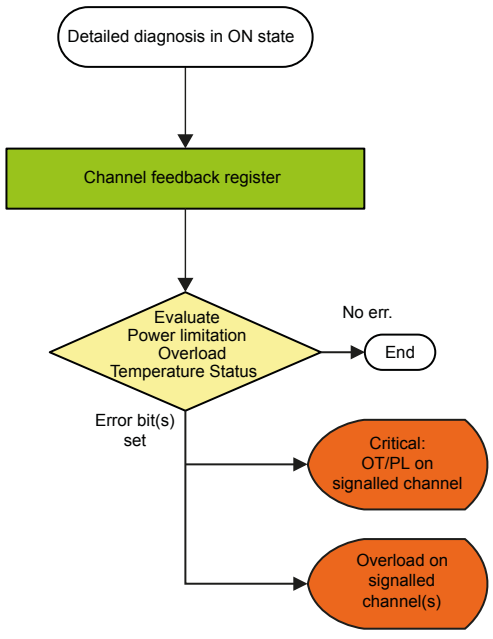
Address	Name	Access	Description
20h to 25h	OUTSR	Read/Clear	Outputs status Register from 0x20 (channel 0) to 0x25 (channel 5) (see register map for detailed description)
28h to 2Dh	ADCxSR	Read	Digital current sense registers. from 0x28 (channel 0) to 0x2D (channel 5)
31h	ADC9SR	Read	Digital case temperature sensor voltage sense register.

5.4 Overload (VDS high voltage, overload (OVL))

During low duty cycle PWM operation on a shorted load, the ON time is normally too short to allow power limitation or overtemperature detection, and the ADC output does not report the current flowing on the channel. In this situation, the detection of the overload condition is quite difficult. To overcome this, the voltage drop on the Power MOSFET (V_{DS}) is measured every time the channel is turned OFF. If V_{DS} (voltage across the Power MOSFET output stage) exceeds the threshold defined by the parameter V_{DS_OVL}, an overload condition is detected. The corresponding bit in the overload status register VDSFSR (address from 0x20 to 0x25 depending on the channel) of the OUTSRx register is set (see the Section 5.11: VDS feedback status register “VDSFSR” in the OUTSRx register).

Consequently, the bit 4 in the global status byte is set if it is not masked in the CONFIG register through the dedicated “VDSMASK” bit. The VDSFSR is a warning and the channel can be switched on again even if the VDSFSRx bit is set. The VDSFSRx bit remains unchanged until a read and clear command on VDSFSR is sent by the SPI or until the output is turned off the next time, when the VDS is evaluated again. In the case of low duty cycle PWM operation (that is, 3% typical at 200 Hz in bulb mode), if the output channel is switched ON for a very short time, V_{DS} might be greater than a threshold defined by the parameter V_{DS_OVL} even if the output is not in the overload state so that a false warning is issued.

Figure 25. **Diagnostics flowchart for digital overload detection**



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Refer to Global status byte description, CHFBSR: channel feedback status bit in OUTSRx register and VDS feedback status register “VDSFSR” in OUTSRx register.

5.5 Open-load ON-state detection

The open-load ON-state is performed by reading the digital current sense. In case the output is on and the reported ADC output value is below the requested defined threshold, the open-load condition can be reported.

5.6 Open-load OFF-state detection

After the channel is completely OFF, if the output voltage V_{OUT} exceeds the open-load detection threshold V_{OL}, an open-load in OFF state/stuck to V_{CC} event is reported.

As a consequence, the corresponding bit STKFLTR in the OUTSRx register (address 0x20 to 0x25) is set, the OL_{OFF} bit in the global status register, and the global status bit NOT are set accordingly.

The STKFLTRx bit is set in OFF-state if $V_{OUT} > V_{OL}$ and the t_{DOLOFF} (turn-off delay time) is elapsed. It gives information about the open-load or a stuck to V_{CC} that depends on the configuration of the OUTCTRCRx OLOFFCR bit. The bit is continuously refreshed in OFF-state and it is latched during ON-state. In order to clear the bit in ON-state, it is necessary to send a read and clear command.

STKFLTRx = 1: open-load in OFF-state or stuck to V_{CC} condition occurred for OUTPUTx.

STKFLTRx = 0: no fault detected.

To avoid false detection, the diagnosis starts after the turn-off of a channel with an additional delay t_{DOLOFF}. To distinguish between an open-load OFF-state event and a short to V_{CC} condition, an internal pull-up current generator can be enabled for each channel by setting the corresponding open-load off state bit OL_{OFFCR} (bit 2) in the outputs control registers “OUTCTRCR”(address from 0x00 to 0x05 depending on the channel).

The activated pull-up current generators are active in normal mode, in fail-safe mode, and in standby mode.

Differently, in sleep mode 2 the current generators are switched off. The register contents, however, are saved also in sleep mode 2, and consequently the current generators are reactivated after a return to standby or a wake-up to fail-safe mode. A hardware reset ($V_{DD} < V_{DD\_POR\_OFF}$) or a software reset (command byte = FFh) clears all register contents and hence the current generators are switched off.

Figure 26. Open-load OFF-state detection

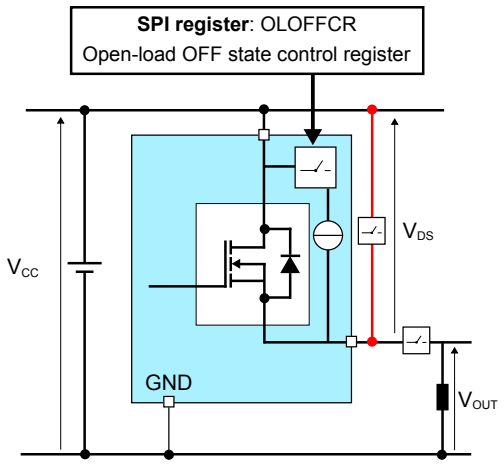

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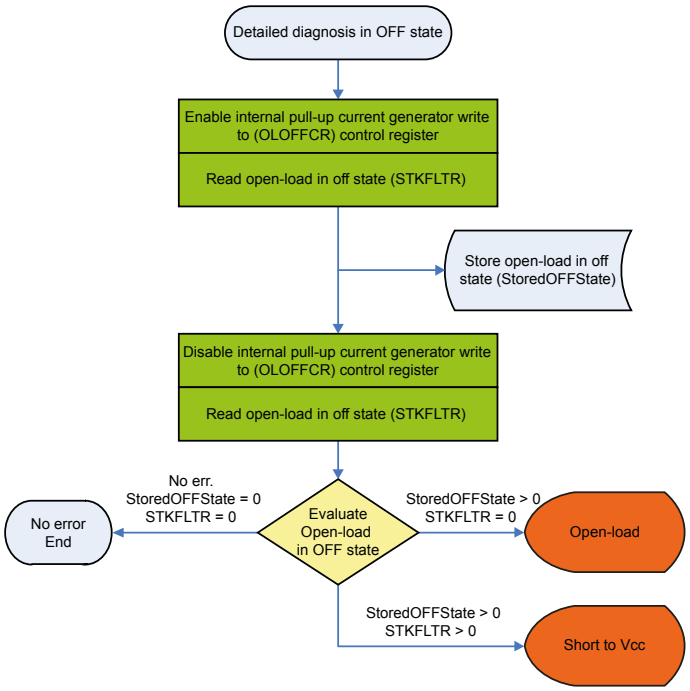
Table 42. STKFLTR state

	With internal pull-up generator	Without internal pull-up generator
Case 1: load connected	“0”/no fault	“0”/no fault
Case 2: no load	“1”/fault	“0”/no fault
Case 3: output shorted to V_{CC}	“1”/fault	“1”/fault

Figure 27. **Diagnostic flowchart for open-load off-state respectively stuck to V_{CC} failure**



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5.7 DIENSR: direct input status bit in OUTSRx register (address from 0x20 to 0x25)

DIENSR bits read back the logic level of the DIx input assigned through OTP to the specific channel. The DIx pins are used to control the outputs channel in case of fail-safe condition or in normal operation if the related “DIENCR” bit set.

5.8 CHFBSR: channel feedback status bit in OUTSRx register

The CHFBSRx provides a logical "OR" combination of VDS (overload), PL (power limitation), OT (overtemperature) failure flags related to OUTPUTx. The contributions of the VDS failure flags to the channel feedback status register and the global status byte can be maskable through the VDSMASK bit in the OUTCFGRx registers.

CHFBSRx = 1: channel OUTPUTx on failure

CHFBSRx = 0: channel OUTPUTx no failure

The bits are refreshed continuously in ON-state and latched in OFF-state.

In order to clear the bit in OFF-state, it is necessary to send a read and clear command.

5.9 Open-load in OFF-State / Stuck to V_{CC} status bit “STKFLTR” in OUTSRx register

This bit is set when the output voltage of the selected channel exceeds the detection threshold at turn-OFF.

The STKFLTRx bit is set in OFF-state if $V_{OUT} > V_{OL}$ and the t_{DOLOFF} (turn-off delay time) is elapsed. It gives information about open-load or a stuck to VCC that depends on the configuration of the OUTCTRCRx OLOFFCR bit register. The bit is continuously refreshed in OFF-state and it is latched during ON-state. In order to clear the bit in ON-state, it is necessary to send a read and clear command.

STKFLTRx = 1: open-load in OFF-state or stuck to V_{CC} condition occurred for OUTPUTx

STKFLTRx = 0: no fault detected

5.10 Channels latch-off status bit “CHLOFFSR” in OUTSRx register

The CHLOFFSR bit is set as soon as there is a fault condition identified as power limitation or overtemperature.

Latch OFF flag register. There is one bit per channel.

In case a latch-off condition occurs, the faulty channel can be reactivated after clearing the related CHLOFFSR bit through a write operation. An SW reset event clears the content of the register.

5.11 VDS feedback status register “VDSFSR” in the OUTSRx register

This bit represents the VDS feedback status. The device is equipped with one VDS bit per channel.

The bit is set in case an overload condition is detected on the related channel. The bit is set independently of the OT.PL. flag.

The VDSFSRx bit is set if, at the instant when the channel is commanded off or is latched off, the V_{CC} - V_{OUT} voltage drop exceeds the V_{DS_OVL} threshold. The bit is latched until the next turn OFF. In order to clear the bit, it is necessary to send a read and clear command.

The VDSFSRx bit is set to:

- 1: over load event occurred for OUTPUTx
- 0: no fault detected

Note: As the status register is not updated while CSN is low, it is possible that the update of the VDSFSR is delayed until the next time it is commanded off, if the Power MOSFET is turned off during an SPI frame.

The contributions of the “VDSFSR” failure flags to the channel feedback status register and the global status byte can be maskable through the VDSMASK bit in the OUTCFGRx registers.

6 Programmable blanking window (PBW)

Dedicated registers for each channel (CHLOFFTCR1 and CHLOFFTCR0) provide a variable and programmable blanking window in case of power limitation or overtemperature event. During this period, the corresponding channel is in auto-restart mode and the channel is allowed to stay in power-limitation and/or overtemperature state before latching off, once blanking time has expired, if the cause of the power limitation or overtemperature event is still present. In this case the channel latches off and the related flag in the latch-off error register (CHLOFFSR) is set. Latch-off flag is also reported in the Global Status Byte (see Section 4.3.1: Global status byte description).

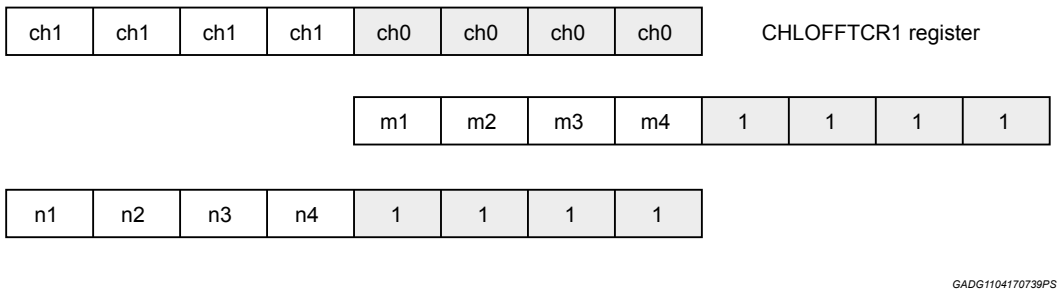
If during the blanking time the cause of power limitation and/or overtemperature event disappears, the timer stops then the rest of the blanking time will be available for another power limitation and/or overtemperature event. Therefore it is up to MCU to reset the timer by refreshing the programmed value in the dedicated register (CHLOFFTCR1 or CHLOFFTCR0).

MCU can keep the device in auto-restart mode artificially forever, by refreshing the programmed blanking time.

6.1 Timer

The 4-bit value per channel written in the registers CHLOFFTCR1 or CHLOFFTCR0 is translated internally into an 8-bit value. The four MSB of this 8-bit value correspond to the content of CHLOFFTCRx register, while the four LSB are filled with 0xF. The 8-bit value refers to an analog timer value.

Figure 28. Internal timer process



The granularity of the 8-bit counter is t_{STEP}. At each power limitation or overtemperature event, the 8-bit counter is decreased by the number of steps equal to the duration of the power limitation or overtemperature event. If the power limitation or overtemperature phase lasts for less than t_{STEP} the counter is decreased by one step.

After each downcount of the 8-bit register, the 4 MSB bits will be transferred to the 4 bits of the corresponding CHLOFFTCRx register in order to refresh this register to the new value of the timer. The microcontroller can only read the 4 MSB bits content of the register. Consequently, the microcontroller can detect a change of every 16 steps of downcounting.

The timer down-counts, if the flag is set as the consequence of the event of power limitation or overtemperature. At the end of the timer's step, the flag is checked. It is reset if the event is not present.

The timer stops down-counting, each time the event has disappeared, or if the channel has turned into OFF state. This does not include the one step down-counting if the flag is set for the first time.

If the event is not present, the timer stops down-counting and resets the flag.

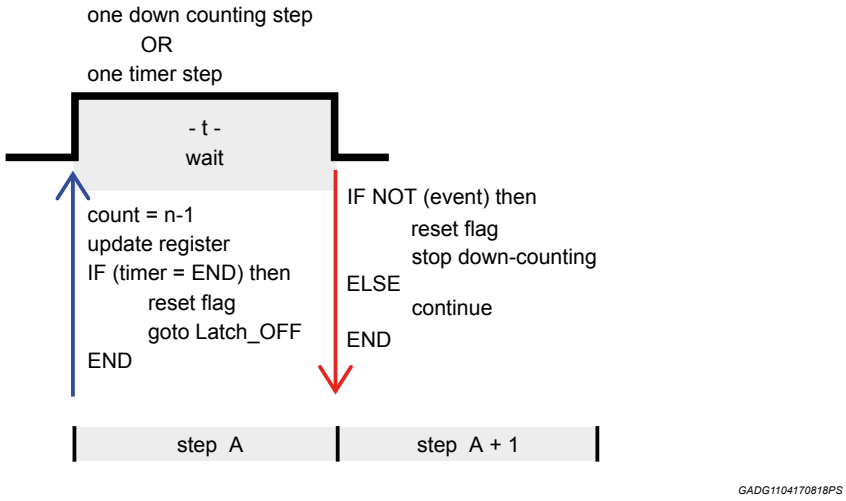
In case the timer reaches the ZERO, the system goes to the latching off state and the related flag in the latch-off error register is set.

Downcounting is stopped and the content of the 8-bit counter is frozen, when the channel is commanded off through the direct input or the SOCR register. The timer can stay with an already down-counted value for a long time. It is up to the MCU to reset it.

MCU can keep the device in autorestart mode artificially forever, by refreshing the timer register value in order not to reach zero.

Below is the figure related to the one timer step. The actions are performed after the rising and falling edges.

Figure 29. One timer step actions



6.2 Blanking window values

The range of the configurable blanking window is shown in Table 43. Time values written by MCU and their real value in timer register

Blanking window reserved values:

- 0x0: It configures the channel in Latch-OFF mode without blanking time. Consequently the channel will latch-off upon the first occurrence of power limitation or overtemperature event.
- 0x1 to 0xF: This value represents the time duration, it will be written by MCU in the register (latch-off timer register) “CHLOFFTCRx” (address 0x10 and 0x11). During this time, the device is allowed to stay in power-limitation and/or overtemperature state before latching off if the “event” is still active or present. The minimum value of the timer, known as zero, is 0x0F. When the timer reaches this value the latch-off action is triggered.

The following table shows the time values written by the MCU and their real value in the timer register.

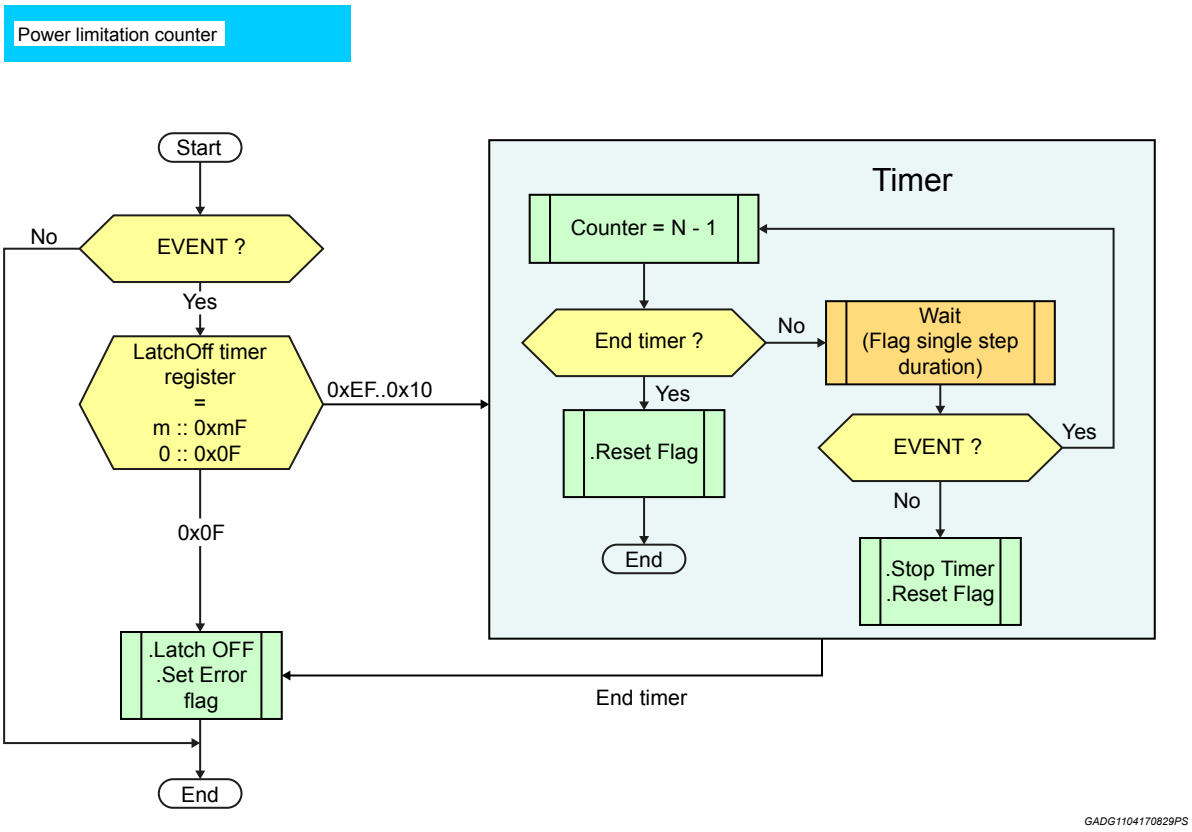
Table 43. Time values written by MCU and their real value in timer register

Bit 7 or bit 3	Bit 6 or bit 2	Bit 5 or bit 1	Bit 4 or bit 0	0xm	0xmF	Typical value of blanking time
0	0	0	0	0x0	0xF	Latch-OFF (ZERO)
0	0	0	1	0x1	0x1F	16 ms
0	0	1	0	0x2	0x2F	32 ms
0	0	1	1	0x3	0x3F	48 ms
....				0x4	0x4F	64 ms
....				…	…	…
1	1	1	0	0xE	0xEF	224 ms
1	1	1	1	0xF	0xFF	240 ms

6.3 Power limitation counter

The flowchart below displays the flow of the events and states. It does not include the timer update by MCU.

Figure 30. Power limitation counter flowchart



6.4 Limp-home mode

In limp-home mode, the device is in unlimited auto restart operation. The blanking time window has no effect on the duration of the auto restart. The timers in the limp-home mode are frozen and are inactive. This guarantees full independence of the limp-home mode operation.

6.5 Registers

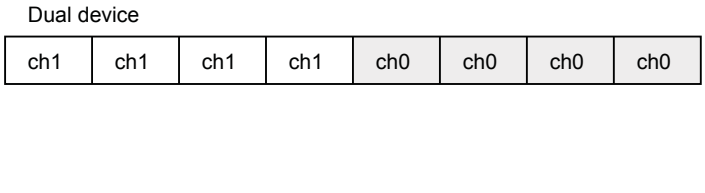
For more details, refer to the SPI register and diagnostics.

- Address 0x10h–channel latch OFF timer control register (CHLOFFTCR0)
- Address 0x11h–channel latch OFF timer control register (CHLOFFTCR1)

Two 16-bit registers (latch-OFF timer: R/W) are used for the channel behavior configuration and the timer value setting.

For each channel 4 bits are used. The value is written by MCU from 0x0 to 0xF.

Figure 31. Example of behavior channel configuration



Latch-Off timer register access

- **Write command**–store new value, read-back (during write command) old value equal to the timer down-counting.
  - Any write command clears the flag in the latch-OFF flag register and resets the timer.
  - This function is used by MCU to clear the flag in the Latch-OFF flag register, which is a read only register.
- **Read command**–reads currently down-counted timer value. If the channel was latched because of the timer expired, the channel is kept latched after the read command.
- **Channels latch-off status bit–CHLOFFSRx in OUTSRx** (address 0x20 to 0x25 depending on the channel). Each channel has one CHLOFFSR flag. In the case of latch-OFF of a channel, this flag is set and readable by MCU. This bit must be cleared to allow the channel to resume operation through a read/clear operation.

7 Electrical specifications

7.1 Absolute maximum ratings

Stressing the device above the rating listed in the Table 44. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 44. Absolute maximum ratings

Symbol	Parameter		Value	Unit
$V_{CC\ LSC}$	Maximum supply voltage for full short-circuit protection		18	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection		28	V
V_{CC}	DC supply voltage		36	V
$-V_{CC}$	Reverse DC supply voltage		0.3	V
$I_{OUT0,1,2,3,4,5}$	Maximum DC output current		Internally limited	A
$-I_{OUT0,5}$	Reverse DC output current		6.6	A
$-I_{OUT1,2,3,4}$			4.4	
I_{PWM_CLK}	DC current sense input current		+3/-1	mA
V_{SDO}	DC SPI pin voltage		V_{DD} + 0.3	A
$-V_{SDO}$	Reverse DC SPI pin voltage		0.3	
$I_{SDI,CSN,SCK}$	DC SPI pin current		+10/-1	A
V_{DD}	DC digital control supply voltage		6	V
$-V_{DD}$	Reverse DC digital control supply voltage		0.3	V
I_{DD}	DC digital control supply current		+10/-1	mA
$I_{DIN0,1}$	DC direct input current		+10/-1	mA
E_{MAX}	Maximum switching energy (single pulse); T_{Jstart} = 150 °C, $CH_{0,5}$, Bulb mode		10	mJ
	Maximum switching energy (single pulse); T_{Jstart} = 150 °C, $CH_{0,5}$, LED mode		3	
	Maximum switching energy (single pulse); T_{Jstart} = 150 °C, $CH_{1,2,3,4}$, Bulb mode		4	
	Maximum switching energy (single pulse); T_{Jstart} = 150 °C, $CH_{1,2,3,4}$, LED mode		1.5	
V_{ESD}	Electrostatic discharge (ANSI-ESDA-JEDEC-JS-001-2014)	DI0,1	1500	V
		V_{DD}	1500	
		PWM_CLK	1500	
		CSN, SDI, SCK, SDO	1500	
		OUT0,1,2,3,4,5	4000	
		V_{CC}	4000	
T_J	Operating junction temperature range		-40 to 150	°C
T_{stg}	Storage temperature range		-55 to 150	°C
I_{LAT}	Latch up current		±20	mA

7.2 Thermal data

Table 45. **Thermal data**

Symbol	Parameter	Typ. value	Unit
R_{thJB}	Thermal resistance, junction-to-board (JEDEC JESD 51-8)	8.9	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	(see Figure 43)	°C/W

7.3 SPI electrical characteristics

Mode 1: 2.7 V < V_{DD} < 5.5 V, -40 °C < T_J < 150 °C, unless otherwise specified.

Table 46. **DC characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD} pin						
$V_{DD\_POR\_ON}$	Power-on reset threshold. Device leaves the Reset mode. Supply of digital part is reset.	V_{DD} increasing; V_{CC} > V_{USD}	1.65	2.15	2.65	V
$V_{DD\_POR\_OFF}$	Power-on shutdown threshold. Device enters Reset mode. Supply of digital part in shutdown.	V_{DD} decreasing; V_{CC} > V_{USD}	1.4	1.9	2.4	V
V_{POR_HYST}	Power-on reset hysteresis			0.2		V
I_{DD}	Digital part supply current in normal mode	V_{DD} = 5 V; SPI active without frame communication		1	1.5	mA
I_{DDstd} at 5 V	Digital part supply current in standby state	V_{DD} = 5 V; T_J = 125 °C, INx = 0 V		5	35	µA
SDI, SCK, PWM_CLK pins						
I_{IL}	Low level Input current	$V_{SDI,SCK}$ = 0.3 V_{DD}	1		10	µA
I_{IH}	High level Input current	$V_{SDI,SCK}$ = 0.7 V_{DD}	1		10	µA
V_{IL}	Input low voltage				0.3V_{DD}	V
V_{IH}	Input high voltage		0.7V_{DD}			V
V_{I_HYST}	Input hysteresis voltage			0.5		V
V_{PWM_CLK}	PWM_CLK clamping voltage	I_{IN} = 3 mA	9		15	V
		I_{IN} = -1 mA		-0.7		V
V_{SDI_CL}	SDI clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V
V_{SCK_CL}	SCK clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V
SDO pin						
V_{OL}	Output low voltage	I_{SDO} = -5 mA; CSN low; fault condition			0.2V_{DD}	V
V_{OH}	Output high voltage	I_{SDO} = 5 mA; CSN low; no fault condition	0.8V_{DD}			V
I_{LO}	Output leakage current	V_{SDO} = 0 V or V_{DD}, CSN high	-5		5	µA
CSN pin						
I_{IL_CSN}	Low level Input current	V_{CSN} = 0.3 V_{DD}	-10		-1	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IH_CSN}	High level Input current	V_{CSN} = 0.7 V_{DD}	-10		-1	µA
V_{IL_CSN}	Output low voltage				0.3V_{DD}	V
V_{IH_CSN}	Output high voltage		0.7V_{DD}			V
V_{HYST_CSN}	Input hysteresis voltage			0.5		V
V_{CL_CSN}	CSN clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V

Table 47. AC characteristics (SDI, SCK, CSN, SDO, PWM_CLK pins) - Mode 1

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{OUT}(1)	Output capacitance (SDO)	V_{OUT} = 0 V to 5 V	-	-	10	pF
C_{IN}(1)	Input capacitance (SDI)	V_{IN} = 0 V to 5 V	-	-	10	pF
	Input capacitance (other pins)	V_{IN} = 0 V to 5 V	-	-	20	pF

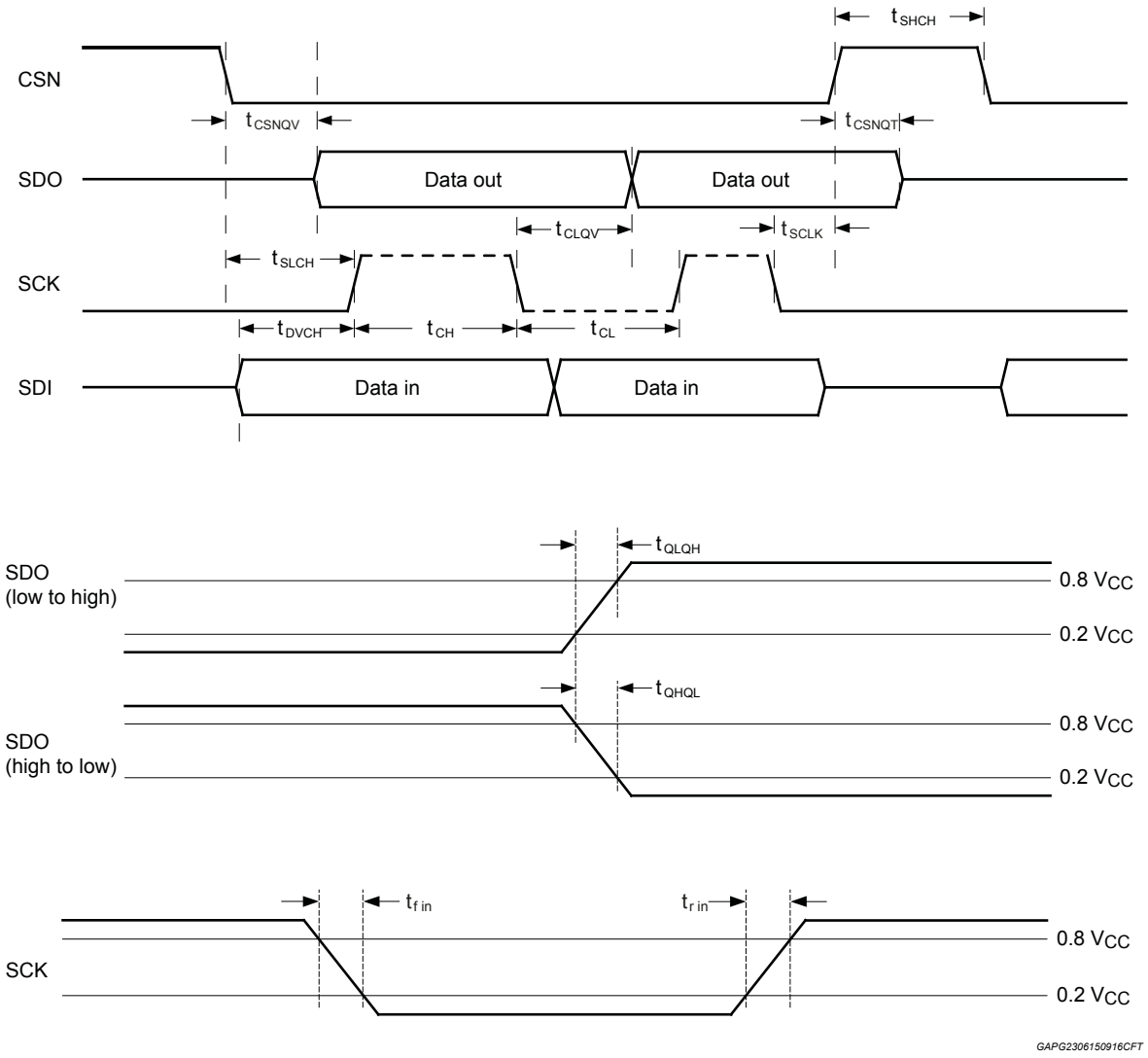
1. *Parameter specified by design, not tested in production.*

Table 48. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_C	Clock frequency	Duty cycle = 50 %	0		8	MHz
t_{WHCH}	CSN timeout: time to release SDO bus		30		70	ms
t_{WDTB}	Watchdog toggle bit timeout		30		70	ms
t_{SLCH}	CSN low setup time		60			ns
t_{SHCH}	CSN high setup time		600			ns
t_{DVCH}	Data in setup time		10			ns
t_{CHDX}	Data in hold time		15			ns
t_{CH}	Clock high time		60			ns
t_{CL}	Clock low time		60			ns
t_{CLQV}	Clock low to output valid	C_{OUT} = 1 nF		75		ns
t_{QLQH}	Output rise time	C_{OUT} = 1 nF		55		ns
t_{QHQL}	Output fall time	C_{OUT} = 1 nF		55		ns
t_{WU}	Rising edge of V_{DD} to first allowed communication		3		23	µs
t_{stdby_out}	Minimum time during which CSN must be toggled low to go out of STDBY mode		20	65	150	µs
t_{SCLK}(1)	SCK setup time before CSN rising		20			ns
t_{CSNQV}(1)	CSN low to output valid				200	ns
t_{CSNQT}(1)	CSN high to output tristate				200	ns

1. *Parameter specified by design, not tested in production.*

Figure 32. **SPI dynamic characteristics**



7.4 Electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_J < 150 °C, unless otherwise specified.

Table 49. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown	T_J = 25 °C			2.9	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.1		V
V_{clamp}	V_{CC} clamp voltage	I_{CC} = 20 mA; $I_{OUT0,1,2,3,4,5}$ = 0 A; T_J = -40 °C	35			V
		I_{CC} = 20 mA; $I_{OUT0,1,2,3,4,5}$ = 0 A; 25 °C < T_J < 150 °C	36	38	45	V
I_S	Supply current	Sleep mode1; V_{CC} = 13 V; T_J = 25 °C; V_{DD} = 0 V		0.1	0.5	µA
		Sleep mode2; V_{CC} = 13 V; T_J = 25 °C; V_{DD} = 5 V		0.1	0.5	µA
		ON-state (all channels OFF); V_{CC} = 13 V; V_{DD} = 5 V; I_{OUT} = 0 A		2.3	3.3	mA
ΔI_{Son}	Additional supply current for each output in ON state driving nominal current	ON-state (per channel); V_{CC} = 13 V; V_{DD} = 5 V $I_{OUT0,5}$ = 2.1 A; $I_{OUT1,2,3,4}$ = 0.7 A			1.7	mA
$I_{L(off)}$	OFF-state output current	V_{DD} = 0 V; V_{CC} = 13 V; T_J = 25 °C	0	0.01	0.5	µA
		V_{DD} = 0 V; V_{CC} = 13 V; T_J = 125 °C; Ch0,5 (per channel)	0		0.6	µA
		V_{DD} = 0 V; V_{CC} = 13 V; T_J = 125 °C; Ch1-4 (per channel)	0		0.2	µA
$V_{F0,5}$	Output V_{CC} diode voltage	V_{CC} = 13 V; I_{OUT} = 1.6 A; T_J = 150 °C			0.7	V
$V_{F1,2,3,4}$		V_{CC} = 13 V; I_{OUT} = 0.8 A; T_J = 150 °C			0.7	V

Table 50. Logic inputs (DI0,1 pins)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL0,1}$	Input low level voltage				0.9	V
$I_{IL0,1}$	Low level input current	V_{DIN} = 0.9 V	1			µA
$V_{IH0,1}$	Input high level voltage		2.1			V
$I_{IH0,1}$	High level input current	V_{DIN} = 2.1 V			10	µA
$V_{I(hyst)0,1,2,3}$	Input hysteresis voltage		0.2			V
$V_{ICL0,1}$	Input clamp voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V

Table 51. Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔT_{PLIM} (1)	Junction-case temperature difference triggering power limitation protection	V_{CC} = 13 V		70		°C
ΔT_{PLIMR}	Junction-case temperature difference resetting power limitation protection	V_{CC} = 13 V		45		°C
T_{TSD}	Shutdown temperature	V_{CC} = 13 V	150	175	210	°C
	Shutdown temperature (V_{CC} decreasing)	V_{CC} = 2.7 V	140			°C
T_R	Reset temperature(2)	V_{CC} = 13 V, latched off mode disabled	T_{RS}+1	T_{RS}+5		°C
T_{RS}	Thermal reset of CHFBSR fault detection(2)	V_{CC} = 13 V, latched off mode disabled	135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(2)	V_{CC} = 13 V, latched off mode disabled		10		°C
T_{CSD}	Case thermal detection pre-warning(2)	V_{CC} = 13 V (see CTRL)	T_{CSD} nom-10	T_{CSD} nom	T_{CSD} nom+10	°C
T_{CR}	Case thermal detection reset(2)	V_{CC} = 13 V		T_{CSD} nom-10		°C
V_{DS_OVL}	V_{DS} overload detection threshold		V_{CC} - 2	V_{CC} - 1.5	V_{CC} - 1	V
$t_{Blanking}$	Programmable blanking time		14.4		264	ms
t_{ON_MIN}	Minimum turn-on time per channel to avoid false VDS error flag	Bulb mode, ch0 and ch5			200	µs
		LED mode, ch0 and ch5			100	µs
		Bulb mode, ch1, ch2, ch3 and ch4			200	µs
		LED mode, ch1, ch2, ch3 and ch4			100	µs

1. *$Z_{thj\text{-}case}$ x P = ΔT_{PLIM}, $Z_{thj\text{-}case}$ is the thermal impedance, P is the Power.*
2. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 52. Open-load detection (7V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load OFF-state voltage detection threshold	CHx off	V_{CC} - 2	V_{CC} - 1.5	V_{CC} - 1	V
I_{PU}	Pull-up current generator for open-load at OFF-state detection	Pull-up current generator active, V_{OUT} = V_{CC} - 1.0 V	-0.5	-1	-1.5	mA
t_{DOLOFF}	Delay time after turn off to allow open-load OFF-state detection		100	170	250	µs

7.5 PWM unit

2.7 V < V_{DD} < 5.5 V; -40 °C < T_J < 150 °C, unless otherwise specified.

Table 53. PWM Unit

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PWM_Res	PWM resolution	PWM_Divider_1,2,3			0.1	%
		PWM_Divider_4			0.2	
PWM_Clk	PWM clock range		300	400	500	kHz
PWM_Clk_flbk	PWM clock fallback		300	400	500	kHz
PWM_Clk_flbk_del	PWM clock fallback delay		20		40	µs

Note: PWMCLOCKLOW warning flag is set only when the period of the clock signal externally applied to PWM_CLK pin is longer than PWM_Clk_flbk_del.

Consequently, if the PWM_CLK frequency is higher than 50 kHz (corresponding to a period of 20 µs, which is the minimum value of PWM_Clk_flbk_del) this flag is never set.

When PWMCLOCKLOW warning flag is set, an internal fallback clock (at a typical frequency of 400 kHz) is used to substitute the external one.

7.6 Bulb mode

Table 54. Bulb – power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON\_ch0,5}$(1)	ON-state resistance	I_{OUT} = 1.6 A; T_J = 25 °C	-	33		mΩ
		I_{OUT} = 1.6 A; T_J = 150 °C	-		72	mΩ
		I_{OUT} = 1.6 A; V_{CC} = 4 V; T_J = 25 °C	-		57	mΩ
		I_{OUT} = 0.3 A; V_{CC} = 2.9 V; V_{CC} decreasing; T_J = 25 °C	-		600	mΩ
$R_{ON\_ch1,2,3,4}$(1)	ON-state resistance	I_{OUT} = 0.8 A; T_J = 25 °C	-	90		mΩ
		I_{OUT} = 0.8 A; T_J = 150 °C	-		190	mΩ
		I_{OUT} = 0.8 A; V_{CC} = 4 V; T_J = 25 °C	-		165	mΩ
		I_{OUT} = 0.1 A; V_{CC} = 2.9 V; V_{CC} decreasing; T_J = 25 °C	-		1600	mΩ

1. *For each channel.*

Table 55. Bulb – switching (V_{CC} = 13 V; normal switch mode)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{don}(1)	Turn-on delay time $Ch_{0,5}$ at T_J = 25 °C to 150 °C	Fail-safe mode, bulb mode, from DIx rising to 20% V_{OUT}; R_L = 8.1 Ω; SLOPECRx = 00	4.5	28	50	µs
	Turn-on delay time $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	Fail-safe mode, bulb mode, from DIx rising to 20% V_{OUT}; R_L = 17 Ω; SLOPECRx = 00	6	26	45	µs
t_{doff}(1)	Turn-off delay time $Ch_{0,5}$ at T_J = 25 °C to 150 °C	Fail-safe mode, bulb mode, from DIx falling to 80% V_{OUT}; R_L = 8.1 Ω; SLOPECRx = 00	9	32	54	µs
	Turn-off delay time $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	Fail-safe mode, bulb mode, from DIx falling to 80% V_{OUT}; R_L = 17 Ω; SLOPECRx = 00	10	29	49	µs
t_{skew}(1)	Turn-off turn-on time $Ch_{0,5}$ at T_J = 25 °C to 150 °C	Differential pulse skew (t_{doff} - t_{don}); R_L = 8.1 Ω; SLOPECRx = 00	-50	0	+50	µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{skew}(1)	Turn-off turn-on time $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	Differential pulse skew (t_{doff} - t_{don}); R_L = 17 Ω; SLOPECRx = 00	-50	0	+50	µs
(dV_{OUT}/ $dt)_{on}$(1)	Turn-on voltage slope $Ch_{0,5}$ at T_J = 25 °C to 150 °C	V_{OUT} = 2.6 V to 7.8 V; R_L = 8.1 Ω SLOPECRx = 00	0.20	0.6	0.95	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 8.1 Ω SLOPECRx = 01	0.25	0.7	1.15	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 8.1 Ω SLOPECRx = 10	0.28	0.9	1.45	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 8.1 Ω SLOPECRx = 11	0.31	1.2	1.65	V/µs
	Turn-on voltage slope $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	V_{OUT} = 2.6 V to 7.8 V; R_L = 17 Ω SLOPECRx = 00	0.20	0.6	0.95	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 17 Ω SLOPECRx = 01	0.25	0.7	1.15	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 17 Ω SLOPECRx = 10	0.28	0.9	1.45	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 17 Ω SLOPECRx = 11	0.31	1.3	1.65	V/µs
(dV_{OUT}/ $dt)_{off}$(1)	Turn-off voltage slope $Ch_{0,5}$ at T_J = 25 °C to 150 °C	V_{OUT} = 10.4 V to 5.2 V; R_L = 8.1 Ω SLOPECRx = 00	0.13	0.6	0.84	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 8.1 Ω SLOPECRx = 01	0.18	0.7	0.97	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 8.1 Ω SLOPECRx = 10	0.30	0.8	1.60	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 8.1 Ω SLOPECRx = 11	0.34	1.2	1.78	V/µs
	Turn-off voltage slope $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	V_{OUT} = 10.4 V to 5.2 V; R_L = 17 Ω SLOPECRx = 00	0.13	0.6	0.84	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 17 Ω SLOPECRx = 01	0.18	0.7	0.97	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 17 Ω SLOPECRx = 10	0.30	0.8	1.60	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 17 Ω SLOPECRx = 11	0.34	1.2	1.78	V/µs
W_{ON}	Switching losses energy at turn-on $Ch_{0,5}$	R_L = 8.1 Ω; SLOPECRx = 00		0.1	0.3(2)	mJ
	Switching losses energy at turn-on $Ch_{1,2,3,4}$	R_L = 17 Ω; SLOPECRx = 00		0.05	0.15(2)	mJ
W_{OFF}	Switching losses energy at turn-off $Ch_{0,5}$	R_L = 8.1 Ω; SLOPECRx = 00		0.1	0.3(2)	mJ
	Switching losses energy at turn-off $Ch_{1,2,3,4}$	R_L = 17 Ω; SLOPECRx = 00		0.05	0.15(2)	mJ

1. See *Figure 33. Switching characteristics.*
2. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 56. Bulb – protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH\_ch0,5}$ (1)	DC short-circuit current	V_{CC} = 16 V, T_J = -40 °C	-15%	34.5	15%	A
		V_{CC} = 16 V, T_J = 150 °C	-15%	25	15%	A
$I_{limH\_ch0,5}$ at 19 V	DC short-circuit current	V_{CC} = 19 V, T_J = 25 °C		15		A
$I_{limL\_ch0,5}$	Short-circuit current during thermal cycling	V_{CC} =13 V, $T_R < T_J < T_{TSD}$		40% $I_{limH\_ch0,5}$		A
$I_{limH\_ch1,2,3,4}$ (2)	DC short-circuit current	V_{CC} = 16 V, T_J = -40 °C	-15%	15.5	15%	A
		V_{CC} = 16 V, T_J = 150 °C	-15%	11.5	15%	A
$I_{limH\_ch1,2,3,4}$ at 19 V	DC short-circuit current	V_{CC} = 19 V, T_J = 25 °C		6.5		A
$I_{limL\_ch1,2,3,4}$	Short-circuit current during thermal cycling	V_{CC} =13 V, $T_R < T_J < T_{TSD}$		40% $I_{limH\_ch1,2,3,4}$		A
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 0.85 A; $V_{IN0,5}$ = 0 V; L = 6 mH; 25 °C < T_J < 150 °C	V_{CC} - 36	V_{CC} - 38	V_{CC} - 45	V
		I_{OUT} = 0.4 A; $V_{IN1,2,3,4}$ = 0 V; L = 6 mH; 25 °C < T_J < 150 °C				

1. *$I_{limH\_ch0,5}$, guaranteed between 7 V and 16 V, -40 °C < T_J < 150 °C.*
2. *$I_{limH\_ch1,2,3,4}$, guaranteed between 7 V and 16 V, -40 °C < T_J < 150 °C.*

Table 57. Bulb – digital current sense (7 V < V_{CC} < 18 V, channel 0,5; T_J = -40 °C to 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 70 mA; T_J = -40 °C to 150 °C	-65%	112	65%	1/A
K_{LED}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 90 mA; T_J = -40 °C to 150 °C	-45%	112	45%	1/A
K_0	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 0.25 A; T_J = -40 °C to 150 °C	-20%	112	20%	1/A
K_1	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 1.25 A	-10%	112	10%	1/A
K_2	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 6 A	-7%	112	7%	1/A
I_{OUT_OFFSET} (1)	Output current offset	ISENSE = 000H	-35		35	mA
$I_{OUT\_SAT\_BULB}$	Output saturation current in bulb mode	ISENSE = 3FFH	8			A
$t_{ON\_CS(min)\_Bulb}$	Minimum ON time for digital current sense availability				280	µs

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 58. Bulb – digital current sense (7 V < V_{CC} < 18 V, channel 1,2,3,4; T_J = -40 °C to 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 30 mA; T_J = -40 °C to 150 °C	-65%	200	65%	1/A
K_{LED}	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 45 mA; T_J = -40 °C to 150 °C	-45%	200	45%	1/A
K_0	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 0.09 A;	-20%	200	20%	1/A

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		T_J = -40 °C to 150 °C				
K_1	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 0.45 A	-10%	200	10%	1/A
K_2	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 3.6 A	-7%	200	7%	1/A
I_{OUT_OFFSET}(1)	Output current offset	ISENSE = 000H	-15		15	mA
$I_{OUT\_SAT\_BULB}$	Output saturation current in bulb mode	ISENSE = 3FFH	4.5			A
$t_{ON\_CS(min)\_Bulb}$	Minimum ON time for digital current sense availability				280	µs

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

7.7 LED mode

7 V < V_{CC} < 18 V; -40 °C < T_J < 150 °C, unless otherwise specified.

Table 59. LED – power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON\_ ch0,5}$(1)	ON-state resistance	I_{OUT} = 0.5 A; T_J = 25 °C	-	130		mΩ
		I_{OUT} = 0.5 A; T_J = 150 °C	-		280	mΩ
		I_{OUT} = 0.5 A; V_{CC} = 4 V; T_J = 25 °C	-		225	mΩ
		I_{OUT} = 0.06 A; V_{CC} = 2.9 V; V_{CC} decreasing; T_J = 25 °C	-		2340	mΩ
$R_{ON\_ ch1,2,3,4}$(1)	ON-state resistance	I_{OUT} = 0.25 A; T_J = 25 °C	-	300		mΩ
		I_{OUT} = 0.25 A; T_J = 150 °C			660	mΩ
		I_{OUT} = 0.25 A; V_{CC} = 4 V; T_J = 25 °C	-		540	mΩ
		I_{OUT} = 0.03 A; V_{CC} = 2.9 V; V_{CC} decreasing; T_J = 25 °C	-		5400	mΩ

1. *For each channel.*

Table 60. LED – switching (V_{CC} = 13 V; Normal switch mode)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{don}(1)	Turn-on delay time $Ch_{0,5}$ at T_J = 25 °C to 150 °C	Failsafe mode, LED mode, from DIx rising to 20% V_{OUT}; R_L = 27 Ω; SLOPECRx = 00	1.5	13	30	µs
	Turn-on delay time $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	Failsafe mode, LED mode, from DIx rising to 20% V_{OUT}; R_L = 50 Ω; SLOPECRx = 00	1.5	13	30	µs
t_{doff}(1)	Turn-off delay time $Ch_{0,5}$ at T_J = 25 °C to 150 °C	Failsafe mode, Bulb mode, from DIx falling to 80% V_{OUT}; R_L = 27 Ω; SLOPECRx = 00	5	17	35	µs
	Turn-off delay time $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	Failsafe mode, Bulb mode, from DIx falling to 80% V_{OUT}; R_L = 50 Ω; SLOPECRx = 00	5	17	35	µs
t_{skew}(1)	Turn-off, turn-on time $Ch_{0,5}$ at T_J = 25 °C to 150 °C	Differential Pulse skew (tpHL-tpLH); R_L = 27 Ω; SLOPECRx = 00	-45	5	55	µs
	Turn-off, turn-on time $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	Differential Pulse skew (tpHL-tpLH); R_L = 50 Ω; SLOPECRx = 00	-45	5	55	µs
$(dV_{OUT}/dt)_{on}$(1)	Turn-on voltage slope $Ch_{0,5}$ at T_J = 25 °C to 150 °C	V_{OUT} = 2.6 V to 7.8 V; R_L = 27 Ω; SLOPECRx = 00	0.58	1.16	1.75	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 27 Ω;	0.60	1.25	1.90	V/µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$(dV_{OUT}/dt)_{on}$[1]	Turn-on voltage slope $Ch_{0,5}$ at T_J = 25 °C to 150 °C	SLOPECRx = 01				
		V_{OUT} = 2.6 V to 7.8 V; R_L = 27 Ω; SLOPECRx = 10	0.64	1.47	2.30	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 27 Ω; SLOPECRx = 11	0.70	1.80	2.90	V/µs
	Turn-on voltage slope $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	V_{OUT} = 2.6 V to 7.8 V; R_L = 50 Ω; SLOPECRx = 00	0.58	1.16	1.75	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 50 Ω; SLOPECRx = 01	0.60	1.25	1.90	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 50 Ω; SLOPECRx = 10	0.64	1.47	2.30	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 50 Ω; SLOPECRx = 11	0.70	1.80	2.90	V/µs
$(dV_{OUT}/dt)_{off}$[1]	Turn-off voltage slope $Ch_{0,5}$ at T_J = 25 °C to 150 °C	V_{OUT} = 10.4 V to 5.2 V; R_L = 27 Ω; SLOPECRx = 00	0.10	0.81	1.52	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 27 Ω; SLOPECRx = 01	0.17	0.91	1.65	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 27 Ω; SLOPECRx = 10	0.30	1.30	2.30	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 27 Ω; SLOPECRx = 11	0.47	1.68	2.90	V/µs
	Turn-off voltage slope $Ch_{1,2,3,4}$ at T_J = 25 °C to 150 °C	V_{OUT} = 10.4 V to 5.2 V; R_L = 50 Ω; SLOPECRx = 00	0.10	0.81	1.52	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 50 Ω; SLOPECRx = 01	0.17	0.91	1.65	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 50 Ω; SLOPECRx = 10	0.30	1.30	2.30	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 50 Ω; SLOPECRx = 11	0.47	1.68	2.90	V/µs
W_{ON}	Switching losses energy at turn-on $Ch_{0,5}$	R_L = 27 Ω; SLOPECRx = 00		0.018	0.04[2]	mJ
	Switching losses energy at turn-on $Ch_{1,2,3,4}$	R_L = 50 Ω; SLOPECRx = 00		0.01	0.025[2]	mJ
W_{OFF}	Switching losses energy at turn-off $Ch_{0,5}$	R_L = 27 Ω; SLOPECRx = 00		0.018	0.04[2]	mJ
	Switching losses energy at turn-off $Ch_{1,2,3,4}$	R_L = 50 Ω; SLOPECRx = 00		0.01	0.025[2]	mJ

1. *see Figure 33. Switching characteristics.*
2. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 61. LED – protection and diagnosis

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH\_ch0,5}$ (1)	DC short-circuit current	V_{CC} = 16 V, T_J = -40 °C	-15%	9.1	15%	A
		V_{CC} = 16 V, T_J = 150 °C	-15%	6.9	15%	A
$I_{limH\_ch0,5}$ at 19 V	DC short-circuit current	V_{CC} = 19 V, T_J = 25 °C		4		A
$I_{limL\_ch0,5}$	Short-circuit current during thermal cycling	V_{CC} =13 V, $T_R < T_J < T_{TSD}$		40% $I_{limH\_ch0,5}$		A
$I_{limH\_ch1,2,3,4}$ (2)	DC short- circuit current	V_{CC} = 16 V, T_J = -40 °C	-15%	4.3	15%	A
		V_{CC} = 16 V, T_J = 150 °C	-15%	3.2	15%	A
$I_{limH\_ch1,2,3,4}$ at 19 V	DC short-circuit current	V_{CC} = 19 V, T_J = 25 °C		1.75		A
$I_{limL\_ch1,2,3,4}$	Short-circuit current during thermal cycling	V_{CC} =13 V, $T_R < T_J < T_{TSD}$		40% $I_{limH\_ch1,2,3,4}$		A

1. *$I_{limH\_ch0,5}$, guaranteed between 7 V and 16 V, -40 °C < T_J < 150 °C.*
2. *$I_{limH\_ch1,2,3,4}$, guaranteed 7 V and 16 V, -40 °C < T_J < 150 °C.*

Table 62. LED – digital current sense (7 V < V_{CC} < 18 V, channel 0,5; T_J = -40 °C to 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 25 mA; T_J = -40 °C to 150 °C	-65%	420	65%	1/A
K_{LED}	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 30 mA; T_J = -40 °C to 150 °C	-45%	420	45%	1/A
K_0	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 80 mA; T_J = -40 °C to 150 °C	-20%	420	20%	1/A
K_1	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 400 mA	-10%	420	10%	1/A
K_2	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 1.8 A	-7%	420	7%	1/A
I_{OUT_OFFSET} (1)	Output current offset	ISENSE = 000H	-15		15	mA
$I_{OUT\_SAT\_LED}$	Output saturation current in LED mode	ISENSE = 3FFH	2			A
$t_{ON\_CS(min)\_LED}$	Minimum ON time for digital current sense availability				150	µs

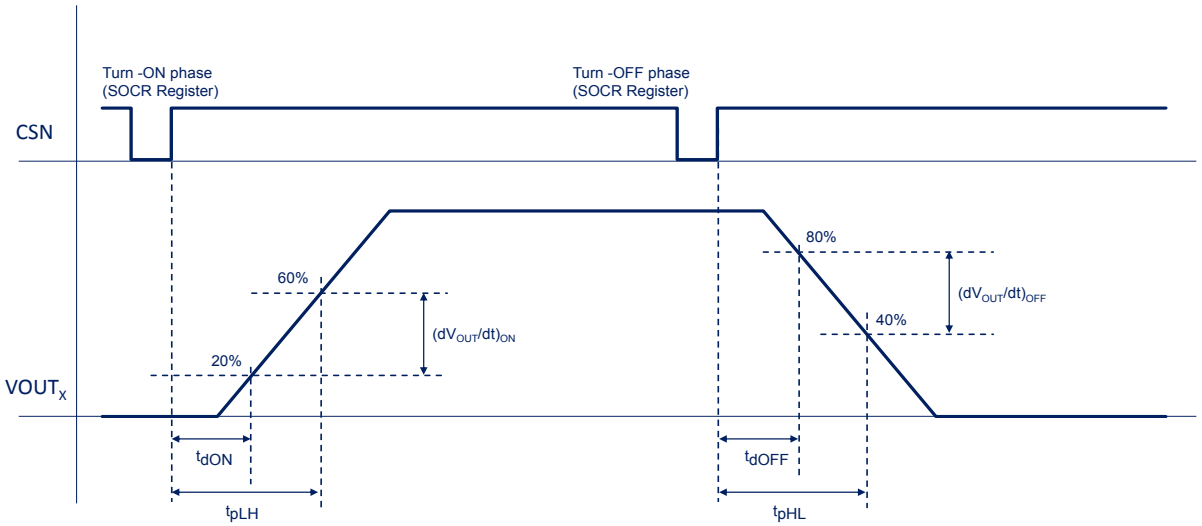
1. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 63. LED – digital current sense (7 V < V_{CC} < 18 V, channel 1,2,3,4; T_J = -40 °C to 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 10 mA; T_J = -40 °C to 150 °C	-65%	640	65%	1/A
K_{LED}	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 15 mA; T_J = -40 °C to 150 °C	-45%	640	45%	1/A
K_0	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 30 mA; T_J = -40 °C to 150 °C	-20%	640	20%	1/A
K_1	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 150 mA	-10%	640	10%	1/A
K_2	Digital current sense gain: ADC_{OUT} / I_{OUT}	I_{OUT} = 1.1 A	-7%	640	7	1/A
I_{OUT_OFFSET}(1)	Output current offset	ISENSE = 000H	-6		6	mA
$I_{OUT\_SAT\_LED}$	Output saturation current in LED mode	ISENSE = 3FFH	1.3			A
$t_{ON\_CS(min)\_LED}$	Minimum ON time for digital current sense availability				150	µs

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

Figure 33. Switching characteristics



8 ISO Pulse

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011(E) and ISO 16750-2:2010.

The related function performances status classification is shown in the Table 64.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, with external components as shown in Figure 34.

“Status II” is defined in ISO 7637-1 Function Performed Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 64. ISO 7637-2 - electrical transient conduction along supply line

Test pulse 2011(E)	Test pulse severity level with status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	Us(1)				
1	III	-112 V	500 pulses	0.5 s	5 s	2 ms, 10 Ω
2a(2)	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4(3)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B (2)		+87 V	5 pulse	1 min		400 ms, 2 Ω

1. *U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.*
2. *With 35 V external suppressor referred to ground (-40 °C < T_J < 150 °C).*
3. *Test pulse in ISO 7637-2:2004(E).*

9 Application schematics

Figure 34. **M0-9 SPI application schematic**

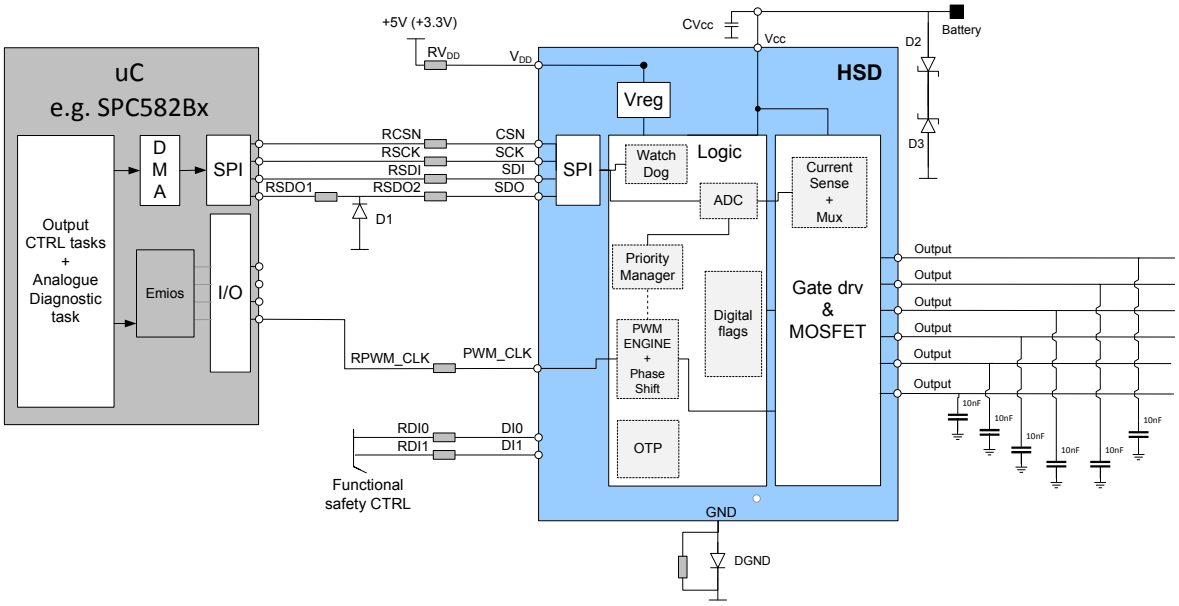


Table 65. **Component values**

Reference	Value	comment
RV_{DD}	330 Ω	Device logic protection
CV_{CC}	100 nF	Battery voltage spikes filtering mounted close to IC
RCSN	2.7 kΩ	Microcontroller protection during overvoltage and reverse polarity
RSCK	2.7 kΩ	Microcontroller protection during overvoltage and reverse polarity
RSDI	2.7 kΩ	Microcontroller protection during overvoltage and reverse polarity
RSDO2	220 Ω	Microcontroller protection during overvoltage and reverse polarity
RSDO1	50 Ω	Optional
D1	BAT54	Microcontroller protection during overvoltage and reverse polarity
RPWM_CLK	2.2 kΩ	Microcontroller protection during: overvoltage, reverse polarity and loss of GND
RDI0	15 kΩ	Microcontroller protection during: overvoltage, reverse polarity and loss of GND
RDI1	15 kΩ	Microcontroller protection during: overvoltage, reverse polarity and loss of GND
D2	Suppressor 20 V	Negative transient protection.
D3	Suppressor 36 V	Overvoltage protection.
RGND	4.7 kΩ	
DGND	BAS21 for V_{DD} = 5 V Schottky (i.e., BAT54-Y) for V_{DD} = 3.3 V	Reverse polarity protection. Usage of schottky or standard diode dependent on V_{DD}

10 Maximum demagnetization energy (V_{CC} = 16 V)

Figure 35. **Maximum turn off current versus inductance - Ch0,5 - Bulb mode**

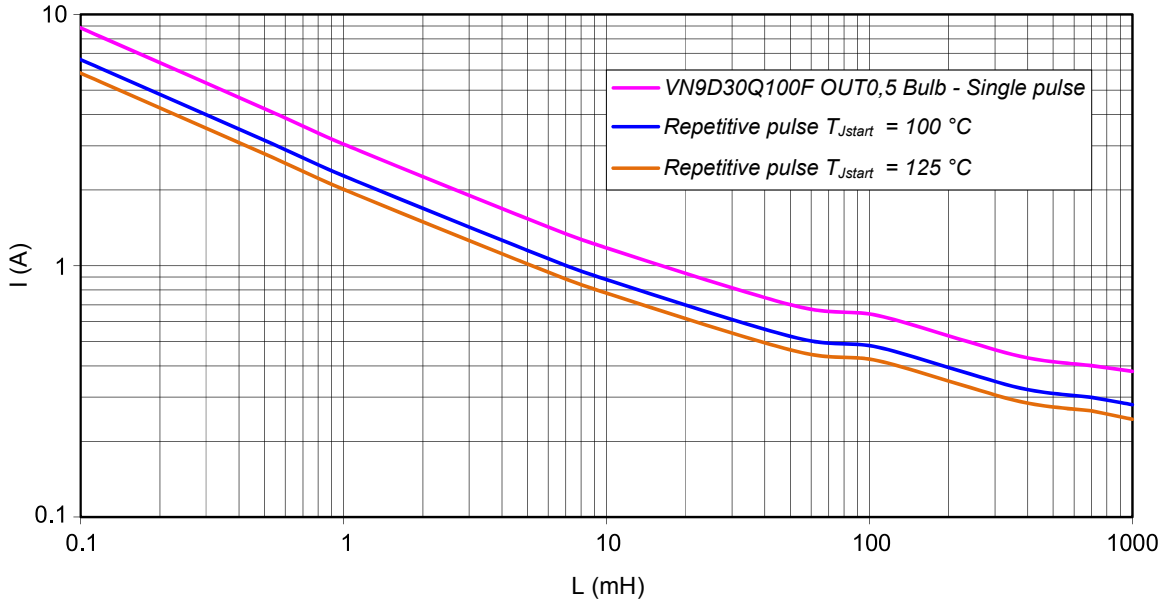


Figure 36. **Maximum turn off current versus inductance - Ch0,5 - LED mode**

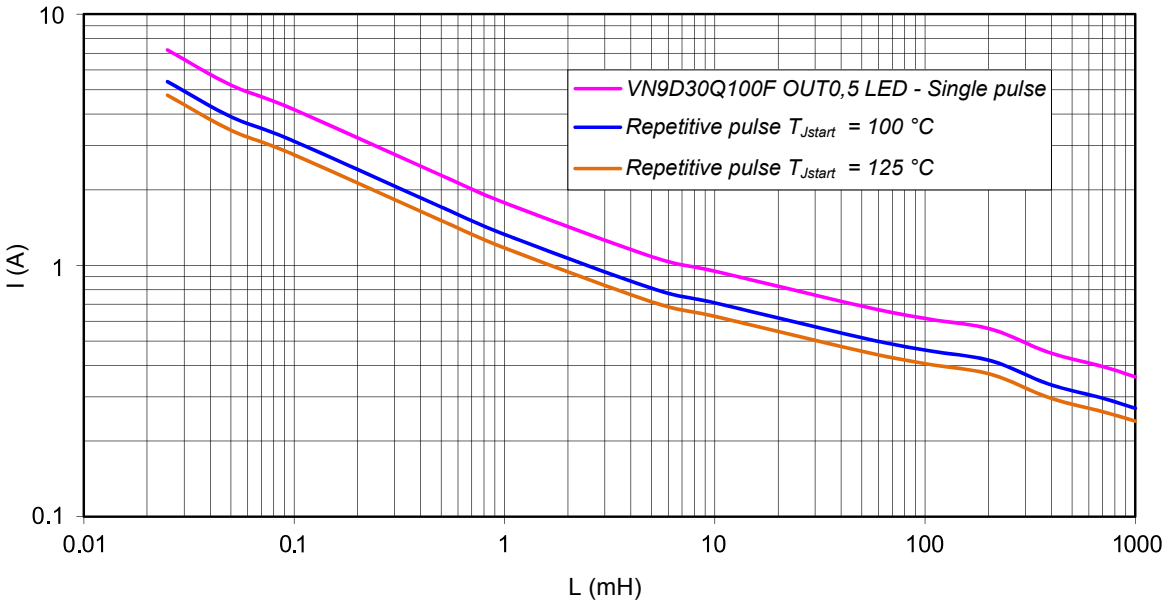


Figure 37. Maximum turn off current versus inductance - Ch1,2,3,4 - Bulb mode

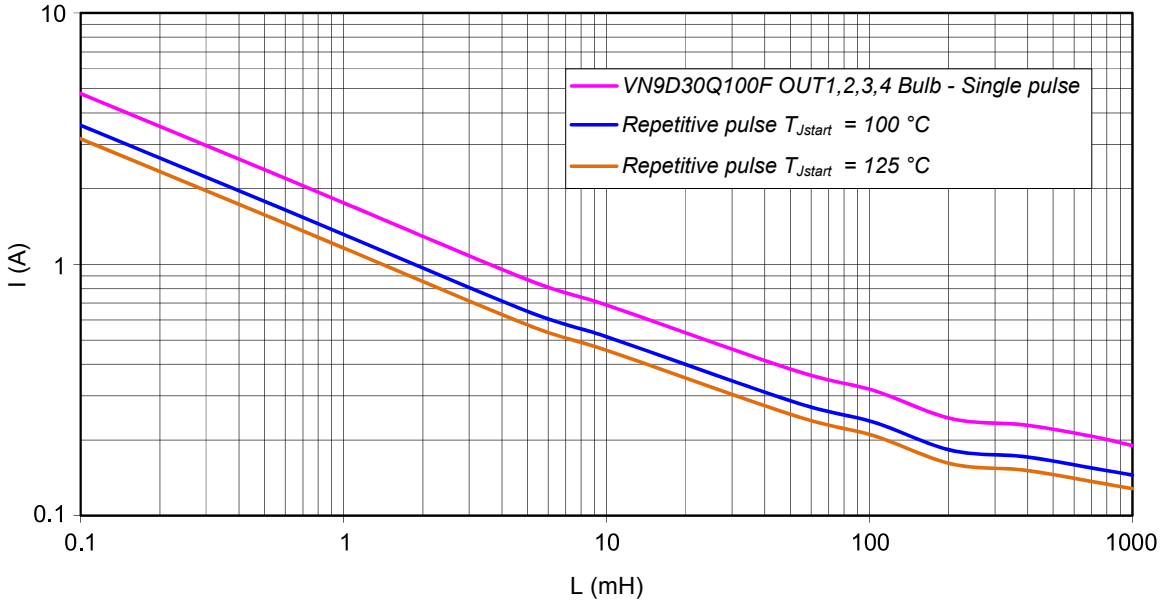
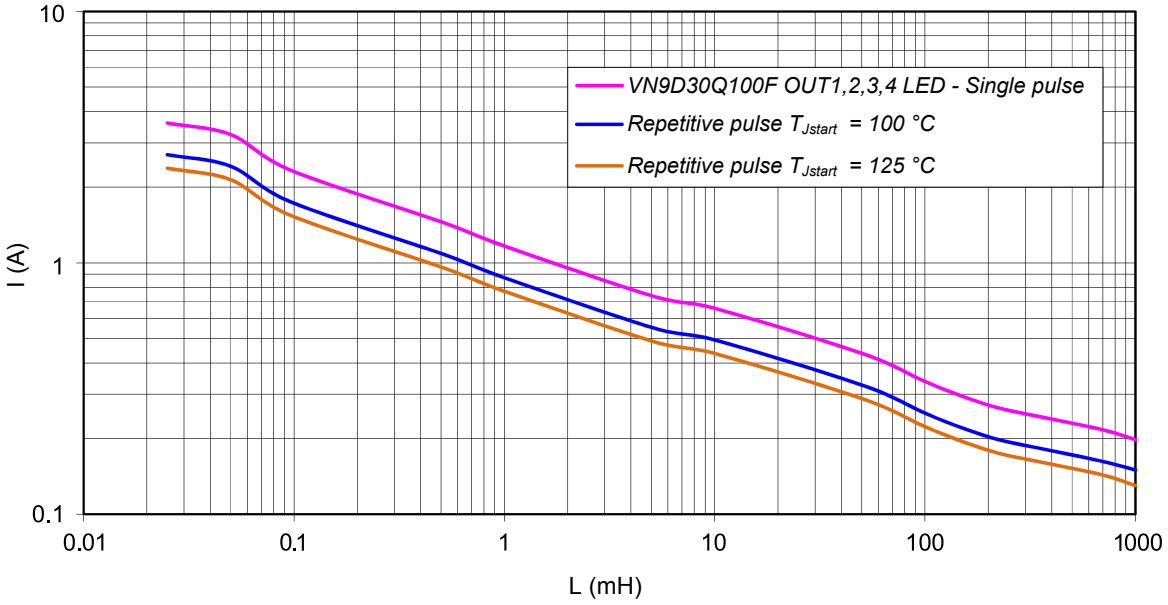


Figure 38. Maximum turn off current versus inductance - Ch1,2,3,4 - LED mode



Note: Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for repetitive curves.

11 Package and PCB thermal data

11.1 QFN 6x6 thermal data

Figure 39. **QFN 6x6 PCB footprint**

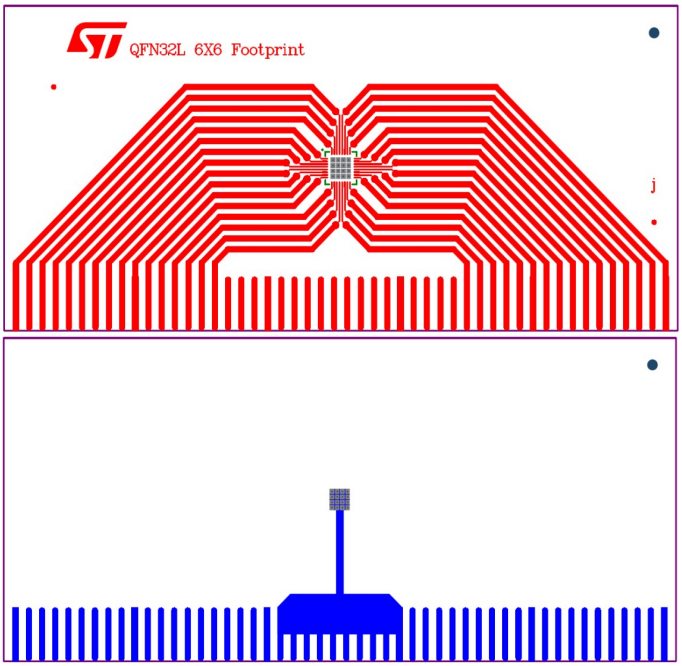


Figure 40. **QFN 6x6 PCB 2 cm²**

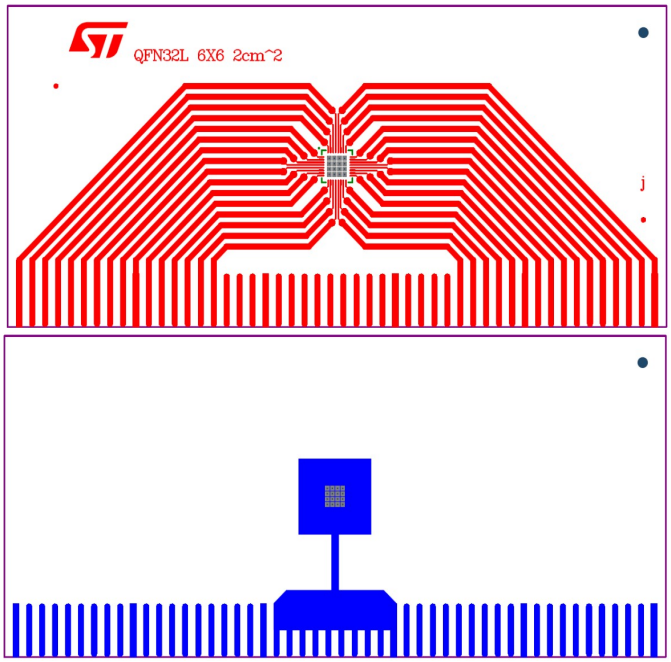


Figure 41. **QFN 6x6 PCB 8 cm²**

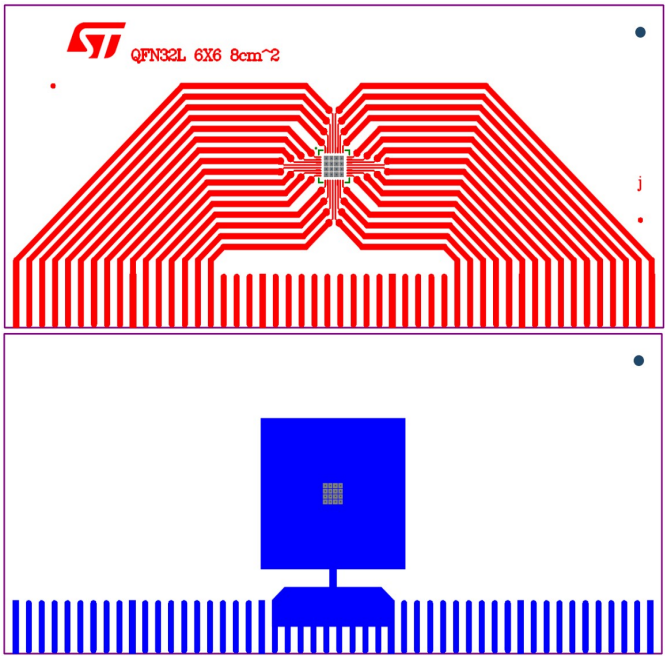


Figure 42. **QFN 6x6 PCB 4 layers**

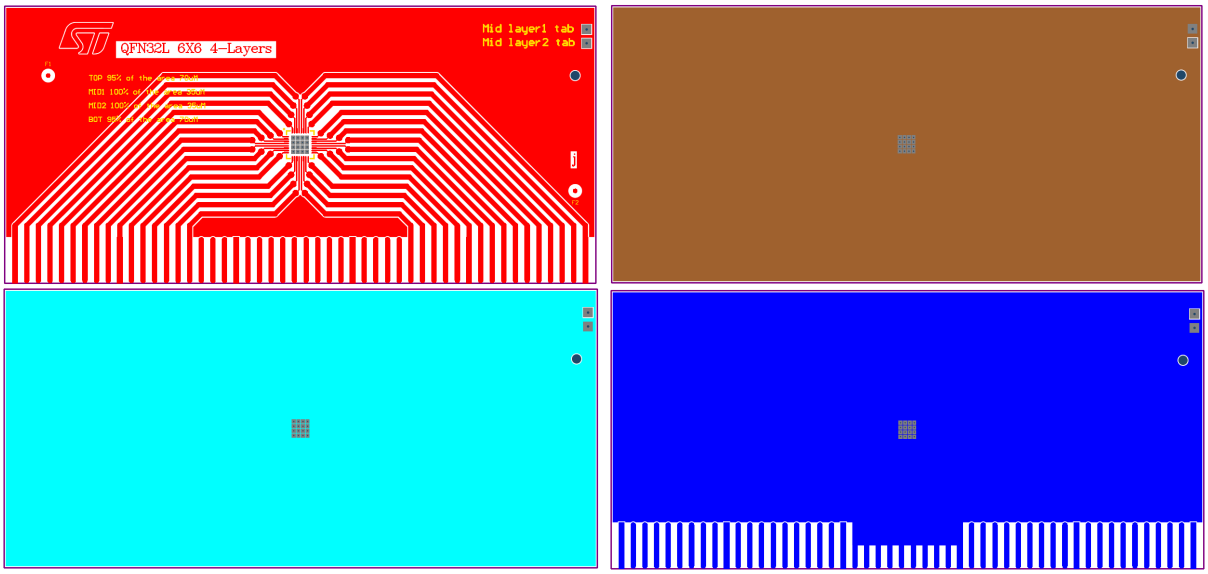
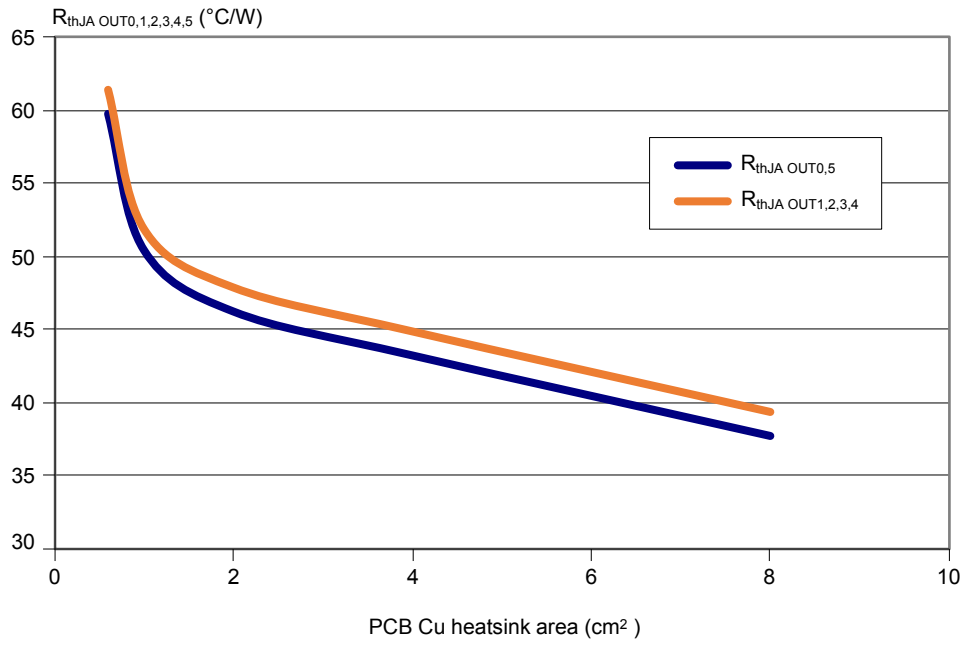


Table 66. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	129 mm x 60 mm
Board material	FR4
Cu thickness (top and bottom layers)	0.070 mm
Cu thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal vias diameter	0.3 mm +/- 0.08 mm
Cu thickness on vias	0.025 mm
Footprint dimension (top layer)	6 mm x 6 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 43. **R_{thJA} vs PCB copper area in open box free air conditions**



OUT 0-5 R_{thJA} on 4Layers PCB: 22.9 °C/W

OUT 1-2-3-4 R_{thJA} on 4Layers PCB: 24.6 °C/W

Figure 44. **QFN 6x6 thermal impedance junction ambient for channels 0 and 5**

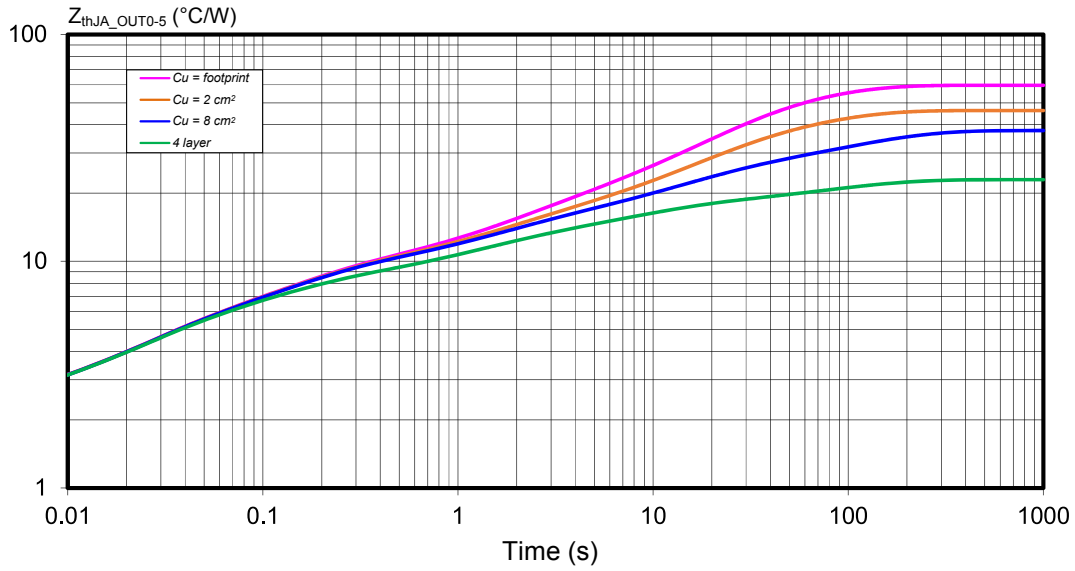
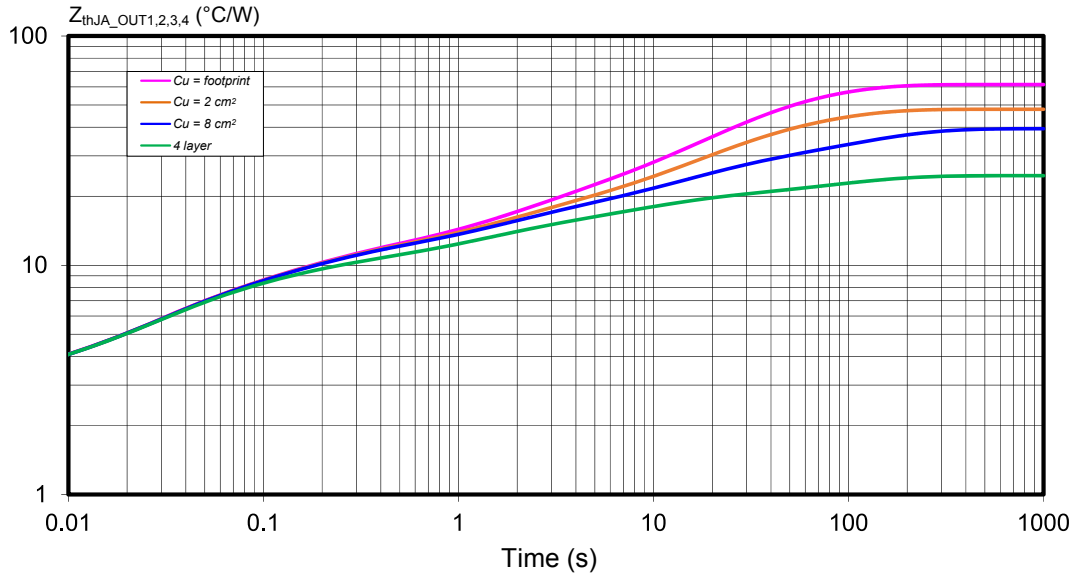


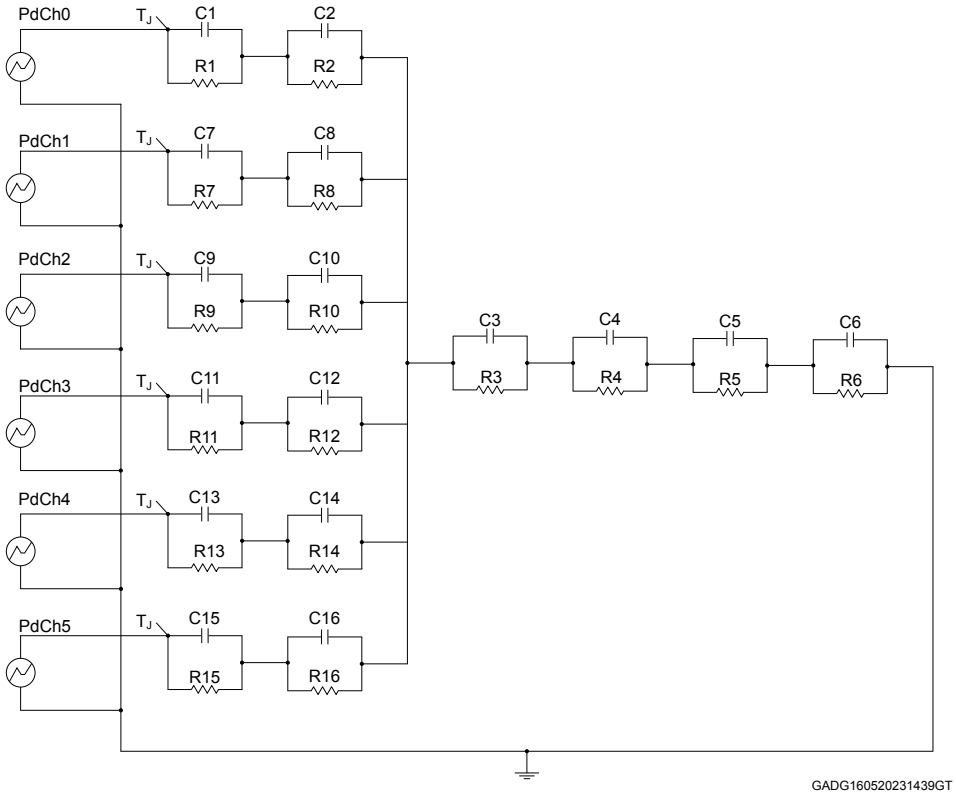
Figure 45. **QFN 6x6 thermal impedance junction ambient for channels 1,2,3,4**



$Z_{th\delta} = R_{th} \cdot \delta + Z_{tht_p} (1 - \delta)$

where $\delta = t_P/T$

Figure 46. **Thermal fitting model**



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 67. **Thermal parameters**

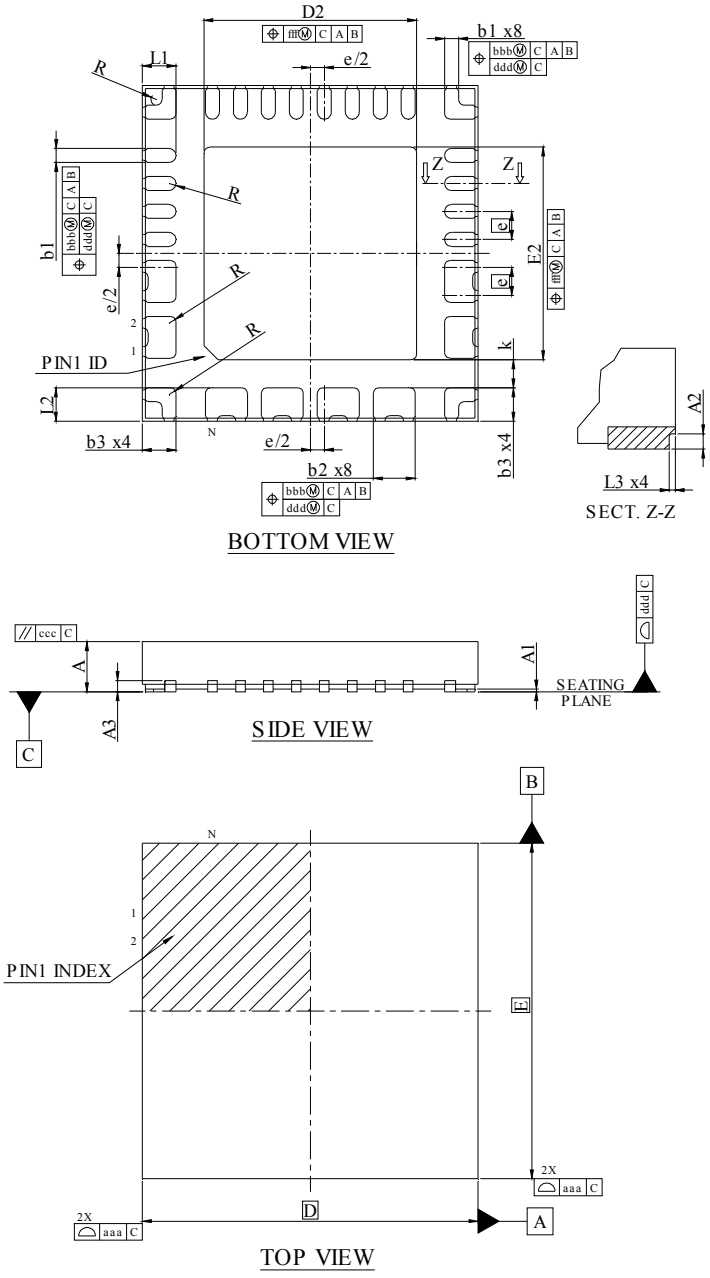
Area/island (cm²)	FP	2	8	4L
R1 = R15 (°C/W)	2			
R2 = R16 (°C/W)	2.2			
R3 (°C/W)	4.5	4.5	4.5	3.5
R4 (°C/W)	6	5	5	4
R5 (°C/W)	21	15	10	5.5
R6 (°C/W)	24	17.5	14	5.7
R7 = R9 = R11 = R13 (°C/W)	2.8			
R8 = R10 = R12 = R14 (°C/W)	3.1			
C1 = C15 (W·s/°C)	0.0005			
C2 = C16 (W·s/°C)	0.01			
C3 (W·s/°C)	0.03			
C4 (W·s/°C)	0.3			
C5 (W·s/°C)	1	1.2	1.4	1.4
C6 (W·s/°C)	2.4	3.5	8	15
C7 = C9 = C11 = C13 (W·s/°C)	0.0004			
C8 = C10 = C12 = C14 (W·s/°C)	0.01			

12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

12.1 QFN 6x6 package information

Figure 47. QFN 6x6 package outline



DM00346180_2

Table 68. **QFN 6x6 mechanical data**

Dim.	Millimeters		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	-	0.05
A2	0.10		
A3		0.20 REF.	
b1	0.20	0.25	0.30
b2	0.70	0.75	0.80
b3	0.50	0.60	0.70
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
L1	0.50	0.60	0.70
L2	0.50	0.60	0.70
L3			0.05
k	0.45		
R			0.10
N		32+4	

Table 69. **QFN 6x6 tolerance of form and position**

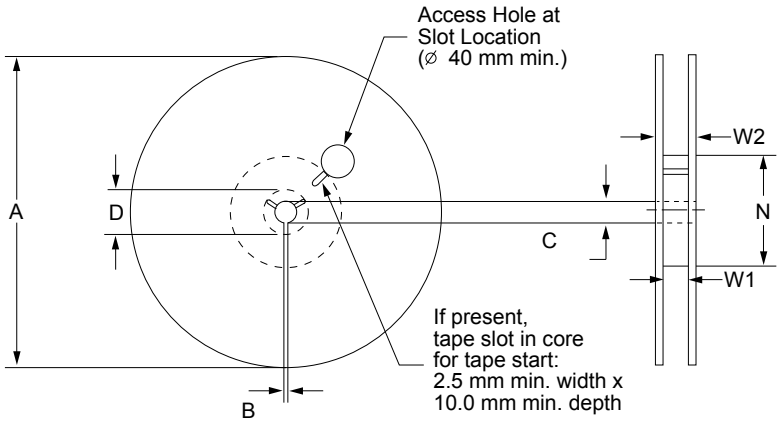
Dim.	Millimeters
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Table 70. **QFN 6x6 variations**

Dim.	Millimeters			OPT.
	Min.	Typ.	Max.	
D2	3.70	3.80	3.90	A
E2	3.70	3.80	3.90	

12.2 QFN 6x6 packing information

Figure 48. **QFN 6x6 reel 13"**



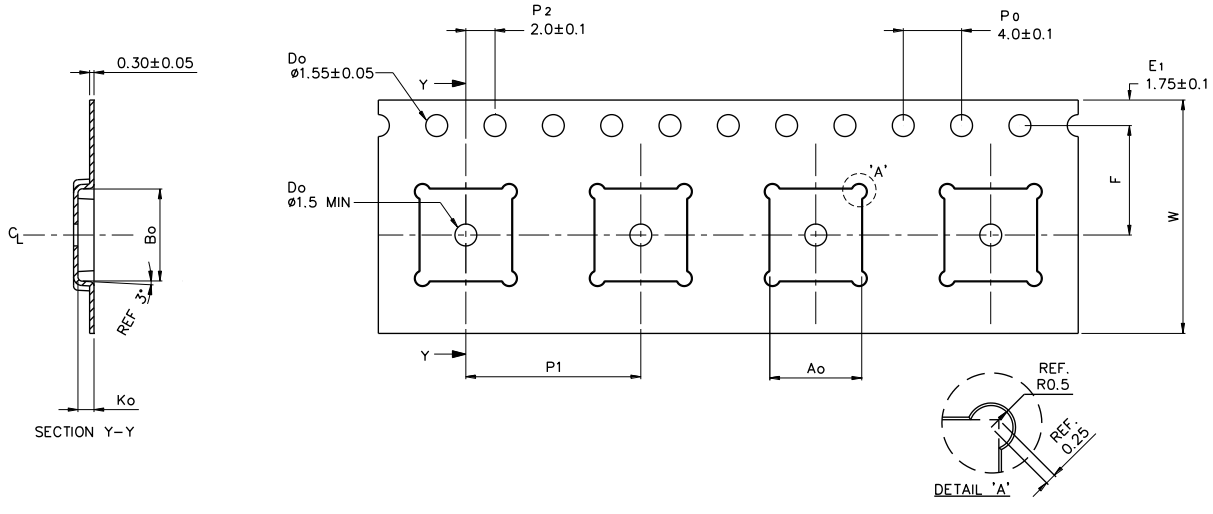
TAPG2004151655CFT

Table 71. **Reel dimensions**

Description	Value(1)
Base quantity	3000
Bulk quantity	3000
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	178
W1	146.4
W2	22.4

1. *All dimensions are in mm.*

Figure 49. **QFN 6x6 carrier tape**



GADG140420211629GT

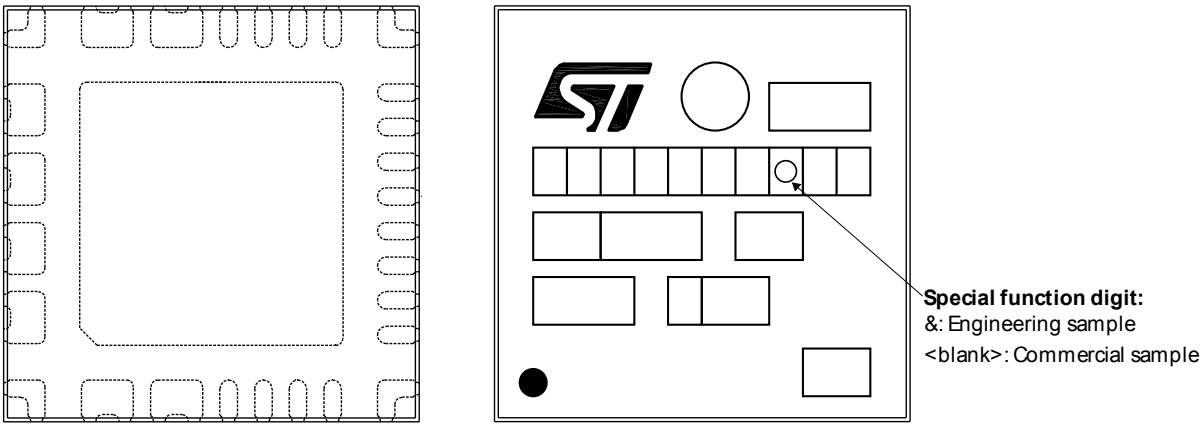
Table 72. **QFN 6x6 carrier tape dimensions**

Description	Value[1]
A_0	6.30 ± 0.1
B_0	6.30 ± 0.1
K_0	1.10 ± 0.1
F	7.50 ± 0.1
P_1	12.00 ± 0.1
W	16.00 ± 0.3

1. *All dimensions are in mm.*

12.3 QFN 6x6 marking information

Figure 50. **QFN 6x6 marking information**



Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 73. **Document revision history**

Date	Version	Changes
07-Feb-2020	1	Initial release.
14-Feb-2020	2	Updated *Pin functionality description*.
22-Dec-2020	3	Added: • Product summary table in Cover Page; • *Section 11.1 QFN 6x6 thermal data.*. Updated: • *Table 23. RAM memory map*; • *Table 37. OTP memory map (reserved)*; • *Section 5.1.2 ADC operating principle*; • *Table 38. Status registers*; • *Section 5.1.4.3 Asynchronous mode*; • *Section 5.2 Integrated LP (Progressive Average) Filter*; • *Table 44. Absolute maximum ratings*; • *Table 45. Thermal data*; • Tables in *Section 7.3 SPI electrical characteristics*; • *Table 49. Power section*; • *Table 51. Protection*; • Tables in *Section 7.6 BULB mode*; • Tables and Figure in *Section 7.7 LED mode*; • Table and Figure in *Section 9 Application schematics*. Minor text changes in: • *Section 4.6.7 OUTSRx*; • *Section 8 ISO Pulse*. Deleted "Reserved" registers in *Section 4.6 Control registers*.
21-May-2021	4	Updated *VN9D30Q100F package silhouette*. Updated note in *Figure 2. Connection diagram (top view)*. Updated *Table 44. Absolute maximum ratings*. Updated *Table 55. BULB - switching (V_{CC} = 13 V; Normal switch mode)*, *Table 57. BULB - Digital current sense (7 V < V_{CC} < 18 V, channel 0,5; T_J = -40 °C to 150 °C)* and *Table 58. BULB - Digital current sense (7 V < V_{CC} < 18 V, channel 1,2,3,4; T_J = -40 °C to 150 °C)*. Updated *Table 60. LED - switching (V_{CC} = 13 V; Normal switch mode)*, *Table 62. LED - Digital current sense (7 V < V_{CC} < 18 V, channel 0,5; T_J = -40 °C to 150 °C)* and *Table 63. LED - Digital current sense (7 V < V_{CC} < 18 V, channel 1,2,3,4; T_J = -40 °C to 150 °C)*. Added *Section 10 Maximum demagnetization energy (V_{CC} = 16 V)*. Added *Section 11.2 QFN 6x6 packing information* and *Section 11.3 QFN 6x6 marking information*. Minor text changes.
20-Jun-2023	5	Updated *Section 2.2 Operating modes and Section 2.2.2 Reset mode*. Updated Section 3.2 Junction overtemperature (OT) and Section 3.3 Power limitation (PL). Updated *Table 24, Section 4.4.1 Procedure to turn on the outputs in PWM operations and Table 33.* Updated *OUTCTRCRx, OUTCFGRx, CHLOFFTCR0, CHLOFFTCR1, SOCR, OUTSRx and ADCxSR*. Updated *Figure 18, Section 5.4 Overload (VDS high voltage, overload (OVL)), Section 5.6 Open-load OFF-state detection, Section 5.9 Open-load in OFF-State / Stuck to VCC status bit "STKFLTR" in OUTSRx register and removed "Figure 24. Diagnostic registers".* Updated *Table 44, Table 46, Table 49, Table 51, Section 7.5 PWM unit, Table 57, Table 58,Table 62 and Table 63.* Updated *Section 8 ISO Pulse*.

Date	Version	Changes
		Swap places "*Section 11 Package information*" with "*Section 12 Package and PCB thermal data*". Updated *Figure 43* and split "*Figure 49*" in the two *Figure 44* and *Figure 45*. Minor text changes.
25-Aug-2023	6	Updated *Table 44. Absolute maximum ratings*.
06-May-2024	7	Updated Figure 2. Connection diagram (top through view), Section 4.2.2: Operating code definition, Table 29. Write SOCR 0x13 and Figure 46. Thermal fitting model.

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