



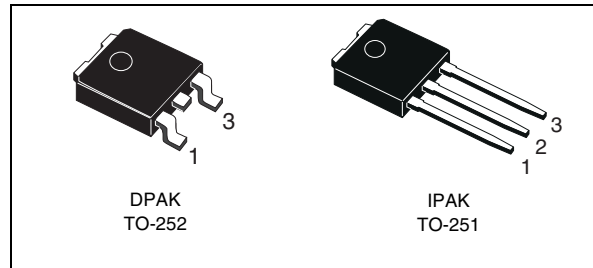
# VND10N06 VND10N06-1

"OMNIFET"  
fully autoprotected Power MOSFET

## Features

|                                   |              |              |
|-----------------------------------|--------------|--------------|
| Max on-state resistance (per ch.) | $R_{DS(on)}$ | 0.3 $\Omega$ |
| Current limitation (typ)          | $I_{lim}$    | 10A          |
| Drain-Source clamp voltage        | $V_{CLAMP}$  | 60V          |

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Logic level input threshold
- ESD protection
- Schmitt trigger on input
- High noise immunity



## Description

The VND10N06 and VND10N06-1 are monolithic devices designed in STMicroelectronics VIPower M0-2 technology, intended for replacement of standard Power MOSFETs in DC to 50KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Table 1. Device summary

| Package | Order codes |               |
|---------|-------------|---------------|
|         | Tube        | Tape and reel |
| DPAK    | VND10N06    | VND10N06TR    |
| IPAK    | VND10N06-1  |               |

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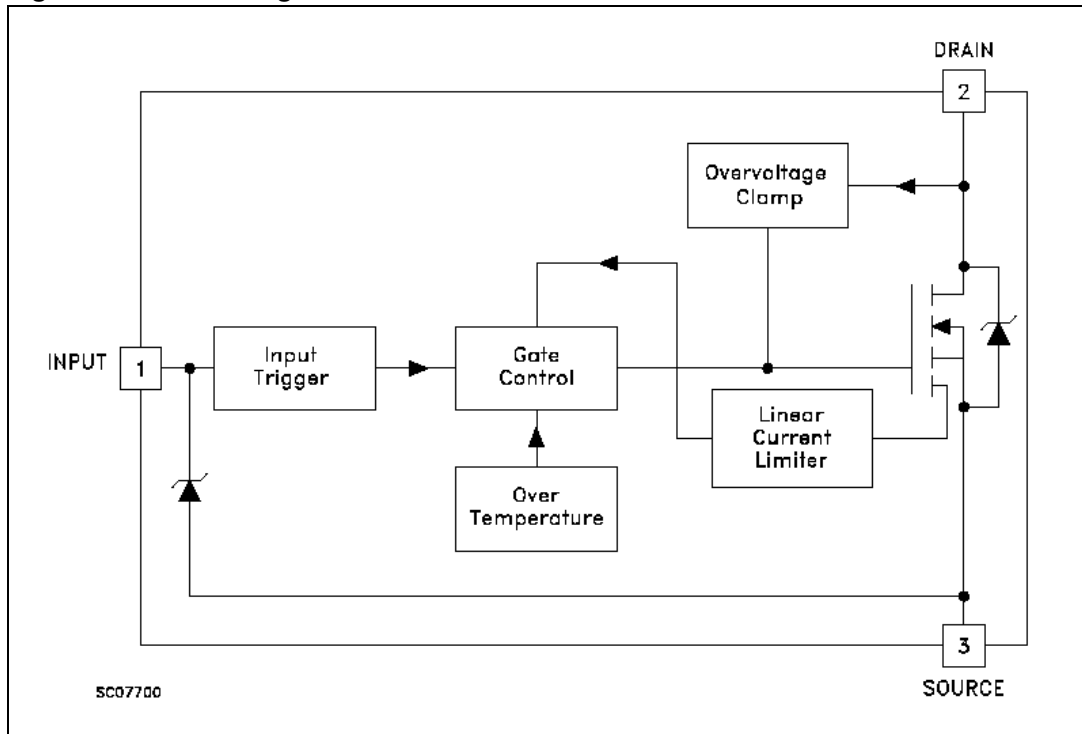
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# 1 Block diagram and pin description

Figure 1. Block diagram



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

**Table 2. Absolute maximum ratings**

| Symbol    | Parameter   | Value              | Unit       |
|-----------|---|--------------------|------------|
| $V_{DSn}$ | Drain-Source voltage ( $V_{in} = 0V$ )                        | Internally clamped | V          |
| $V_{INn}$ | Input voltage   | Internally clamped | V          |
| $I_{in}$  | Input current   | $\pm 20$           | mA         |
| $I_{Dn}$  | Drain current   | Internally limited | A          |
| $I_{Rn}$  | Reverse DC output current                                     | - 15               | A          |
| $V_{ESD}$ | Electrostatic discharge<br>( $R = 1.5K\Omega$ , $C = 100pF$ ) | 4000               | V          |
| $P_{tot}$ | Total dissipation at $T_c = 25^\circ C$                       | 35                 | W          |
| $T_j$     | Operating junction temperature                                | Internally limited | $^\circ C$ |
| $T_c$     | Case operating temperature                                    | Internally limited | $^\circ C$ |
| $T_{stg}$ | Storage temperature   | - 55 to 150        | $^\circ C$ |

### 2.2 Thermal data

**Table 3. Thermal data**

| Symbol         | Parameter                           | Max. value | Unit         |
|----------------|-------------------------------------|------------|--------------|
| $R_{thj-case}$ | Thermal resistance junction-case    | 3.5        | $^\circ C/W$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient | 100        | $^\circ C/W$ |

## 2.3 Electrical characteristics

T<sub>case</sub> = 25 °C unless otherwise stated.

**Table 4. Off**

| Symbol             | Parameter   | Test conditions  | Min.    | Typ. | Max.       | Unit     |
|--------------------|---|--|---------|------|------------|----------|
| V <sub>CLAMP</sub> | Drain-Source clamp voltage                              | V <sub>IN</sub> = 0V; I <sub>D</sub> = 200mA   | 50      | 60   | 70         | V        |
| V <sub>IL</sub>    | Input low level voltage                                 | I <sub>D</sub> = 100 μA; V <sub>DS</sub> = 16 V  |         |      | 1.5        | V        |
| V <sub>IH</sub>    | Input high Level voltage                                | R <sub>L</sub> = 27Ω; V <sub>DD</sub> = 16 V<br>V <sub>DS</sub> = 0.5 V  | 3.2     |      |            | V        |
| I <sub>ISS</sub>   | Supply current from input pin                           | V <sub>DS</sub> = 0V; V <sub>IN</sub> = 5V   |         | 150  | 300        | μA       |
| V <sub>INCL</sub>  | Input-Source reverse clamp voltage                      | I <sub>IN</sub> = -1mA<br>I <sub>IN</sub> = 1mA  | -1<br>8 |      | -0.3<br>11 | V<br>V   |
| I <sub>DSS</sub>   | Zero input voltage drain current (V <sub>IN</sub> = 0V) | V <sub>DS</sub> = 50V; V <sub>IN</sub> = V <sub>IL</sub> ;<br>V <sub>DS</sub> < 35V; V <sub>IN</sub> = V <sub>IL</sub> |         |      | 250<br>100 | μA<br>μA |

**Table 5. Switching<sup>(1)</sup>**

| Symbol                | Parameter             | Test conditions  | Min. | Typ. | Max. | Unit |
|-----------------------|-----------------------|--|------|------|------|------|
| t <sub>d(on)</sub>    | Turn-on delay time    | V <sub>DD</sub> = 16V; I <sub>D</sub> = 1A<br>V <sub>gen</sub> = 7V; R <sub>gen</sub> = 10Ω<br>(see <a href="#">Figure 2</a> )   |      | 1100 | 1600 | ns   |
| t <sub>r</sub>        | Rise time             |  |      | 550  | 900  | ns   |
| t <sub>d(off)</sub>   | Turn-off delay time   |  |      | 200  | 400  | ns   |
| t <sub>f</sub>        | Fall time             |  |      | 100  | 200  | ns   |
| t <sub>d(on)</sub>    | Turn-on delay time    | V <sub>DD</sub> = 16V; I <sub>D</sub> = 1A<br>V <sub>gen</sub> = 7V; R <sub>gen</sub> = 1000Ω<br>(see <a href="#">Figure 2</a> ) |      | 1.2  | 1.8  | μs   |
| t <sub>r</sub>        | Rise time             |  |      | 1    | 1.5  | μs   |
| t <sub>d(off)</sub>   | Turn-off delay time   |  |      | 1.6  | 2.3  | μs   |
| t <sub>f</sub>        | Fall time             |  |      | 1.2  | 1.8  | μs   |
| (di/dt) <sub>on</sub> | Turn-on current slope | V <sub>DD</sub> = 16V; I <sub>D</sub> = 1A<br>V <sub>in</sub> = 7V; R <sub>gen</sub> = 10Ω                                       |      | 1.5  |      | A/μs |
| Q <sub>i</sub>        | Total input charge    | V <sub>DD</sub> = 12V; I <sub>D</sub> = 1A; V <sub>IN</sub> = 7V   |      | 13   |      | nC   |

1. Parameters guaranteed by design / characterization.

**Table 6. On<sup>(1)</sup>**

| Symbol              | Parameter                         | Test conditions   | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------|---|------|------|------|------|
| R <sub>DS(on)</sub> | Static Drain-Source on resistance | V <sub>IN</sub> = 7V; I <sub>D</sub> = 1 A; T <sub>j</sub> < 125 °C |      | 0.15 | 0.3  | Ω    |

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%.

**Table 7. Dynamic**

| Symbol           | Parameter          | Test conditions                                       | Min. | Typ. | Max. | Unit |
|------------------|--------------------|---|------|------|------|------|
| C <sub>OSS</sub> | Output capacitance | V <sub>DS</sub> = 13V; f = 1MHz; V <sub>IN</sub> = 0V |      | 350  | 500  | pF   |

**Table 8. Source Drain diode**

| Symbol                          | Parameter                | Test conditions   | Min. | Typ. | Max. | Unit |
|---------------------------------|--------------------------|---|------|------|------|------|
| V <sub>SD</sub> <sup>(1)</sup>  | Forward on voltage       | I <sub>SD</sub> = 1 A; V <sub>IN</sub> = V <sub>IL</sub>  |      | 0.8  | 1.6  | V    |
| t <sub>rr</sub> <sup>(2)</sup>  | Reverse recovery time    | I <sub>SD</sub> = 1A; di/dt = 100 A/μs<br>V <sub>DD</sub> = 30V; T <sub>j</sub> = 25°C<br>(see <a href="#">Figure 4</a> ) |      | 125  |      | ns   |
| Q <sub>rr</sub> <sup>(2)</sup>  | Reverse recovery charge  |   |      | 0.22 |      | μC   |
| I <sub>RRM</sub> <sup>(2)</sup> | Reverse recovery current |   |      | 3.5  |      | A    |

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%.
2. Parameters guaranteed by design / characterization.

**Table 9. Protections (-40°C < T<sub>j</sub> < 150°C, unless otherwise specified)**

| Symbol                           | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit |
|----------------------------------|-------------------------------|--|------|------|------|------|
| I <sub>lim</sub>                 | Drain current limit           | V <sub>IN</sub> = 7V; V <sub>DS</sub> =13V   | 6    | 10   | 15   | A    |
| t <sub>dlim</sub> <sup>(1)</sup> | Step response current limit   | V <sub>IN</sub> = 7 V; V <sub>DS</sub> step from 0 to 13V  |      | 12   | 20   | μs   |
| T <sub>jsh</sub> <sup>(1)</sup>  | Overtemperature shutdown      |  | 150  |      |      | °C   |
| T <sub>jrs</sub> <sup>(1)</sup>  | Overtemperature reset         |  | 135  |      |      | °C   |
| E <sub>as</sub> <sup>(1)</sup>   | Single pulse avalanche energy | Starting T <sub>j</sub> = 25°C; V <sub>DD</sub> = 24V<br>V <sub>IN</sub> = 7V R <sub>gen</sub> = 1kΩ; L = 10mH | 250  |      |      | mJ   |

1. Parameters guaranteed by design / characterization.

**Figure 2. Switching waveforms**

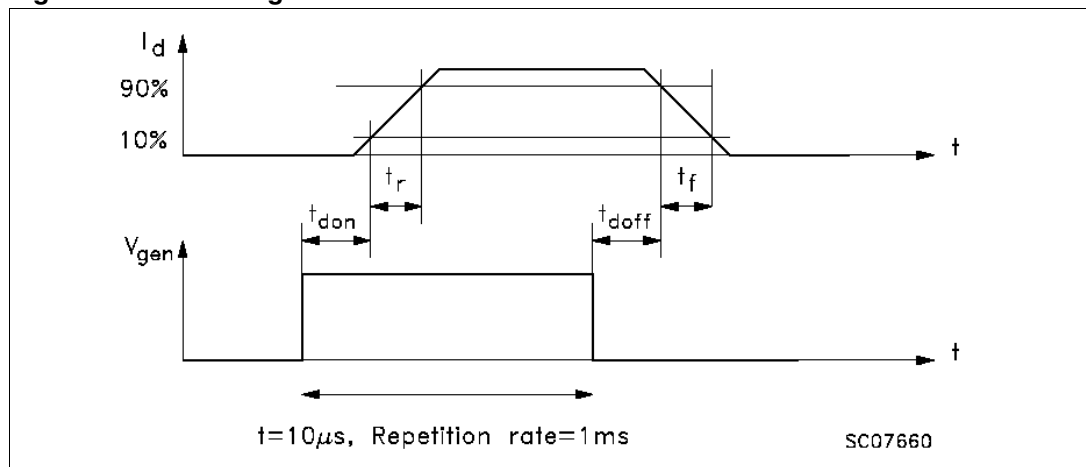




Figure 3. Switching time test circuit for resistive load

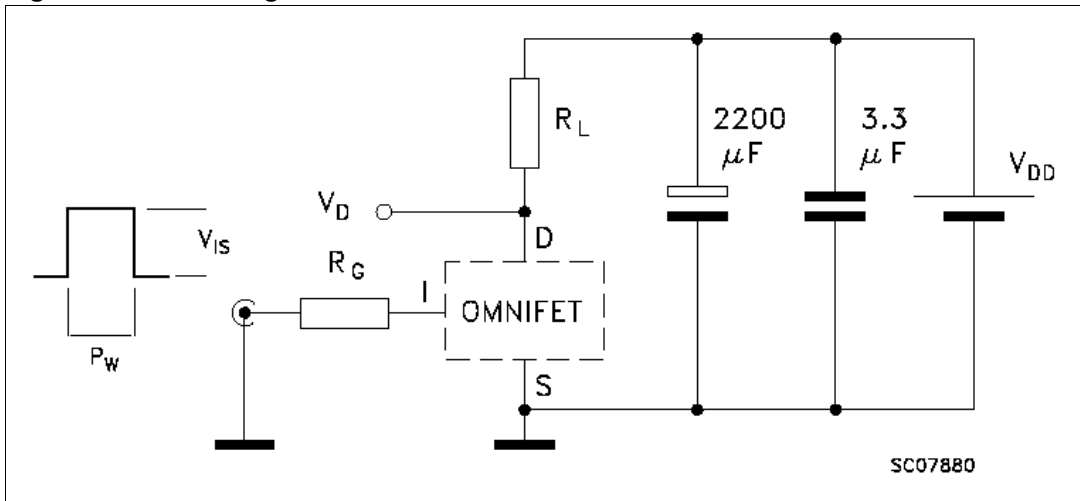


Figure 4. Test circuit for inductive load switching and diode recovery time

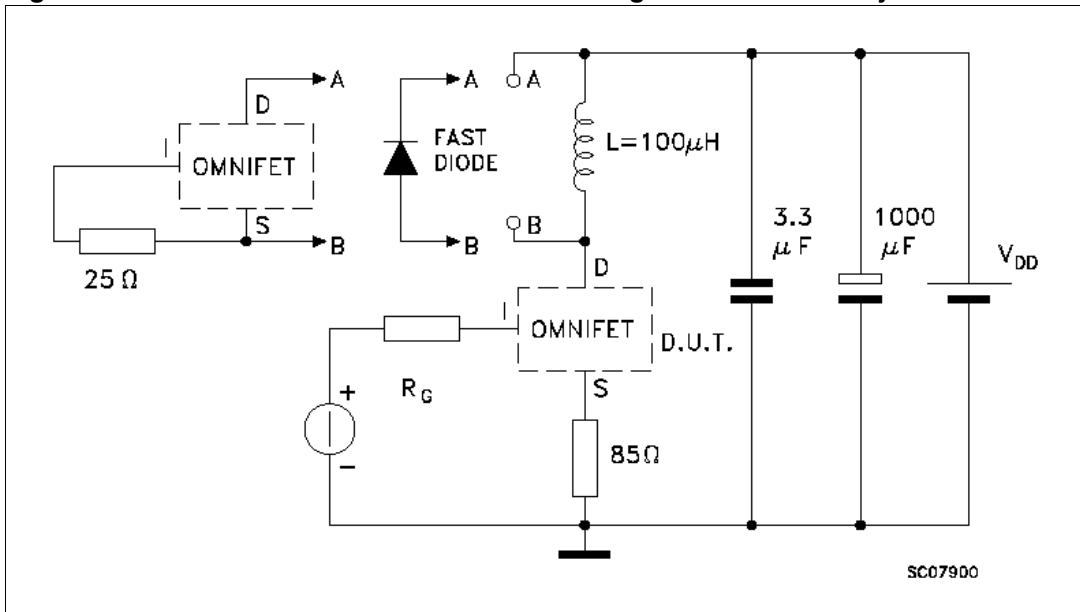


Figure 5. Unclamped inductive load test circuits

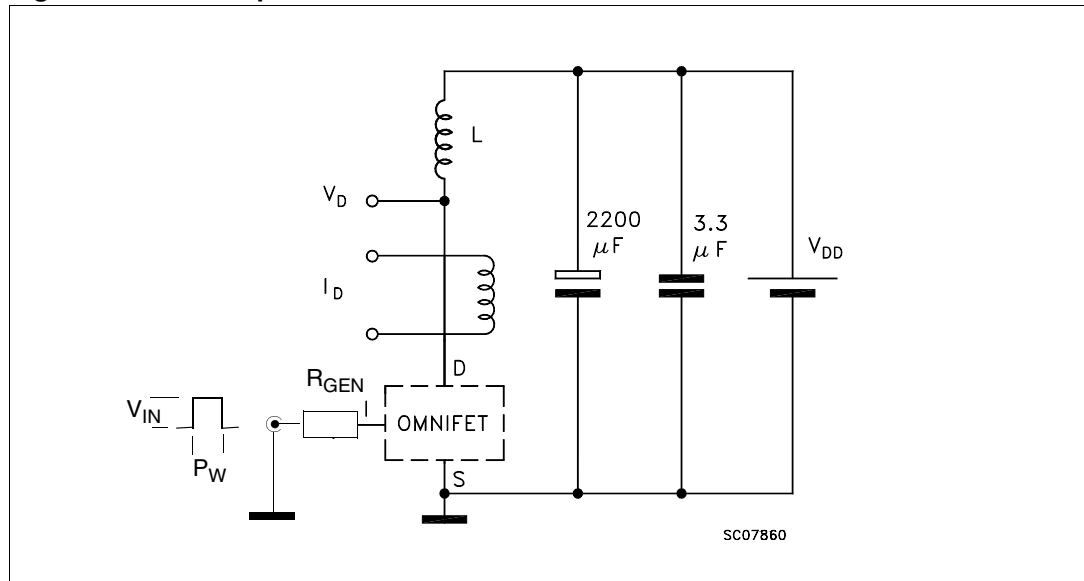


Figure 6. Input charge test circuit

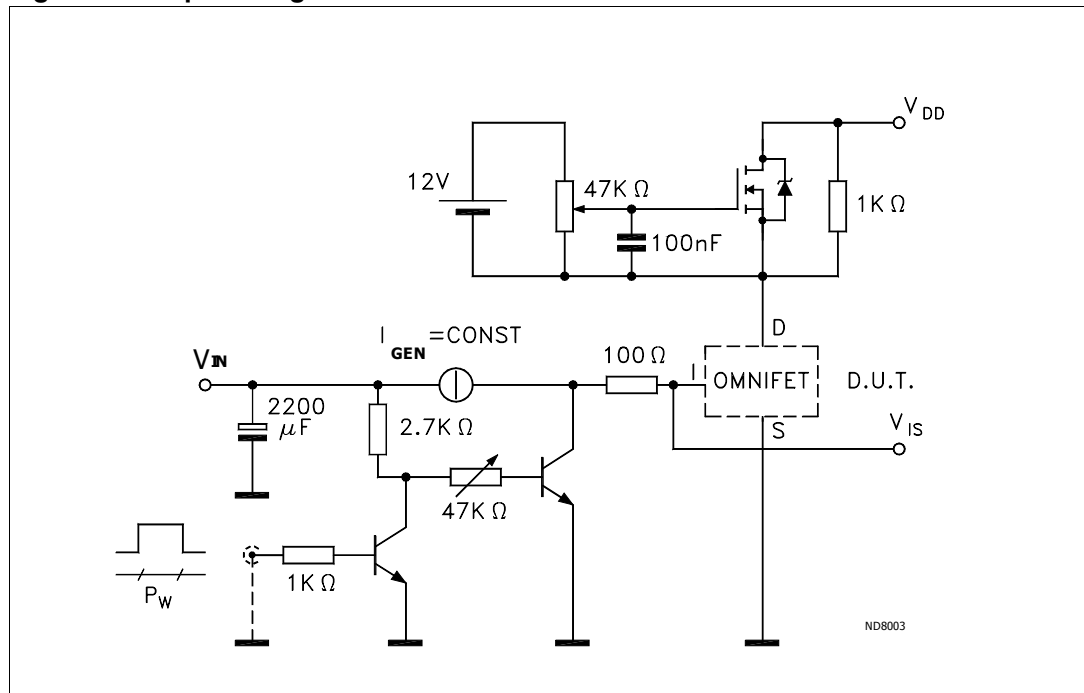
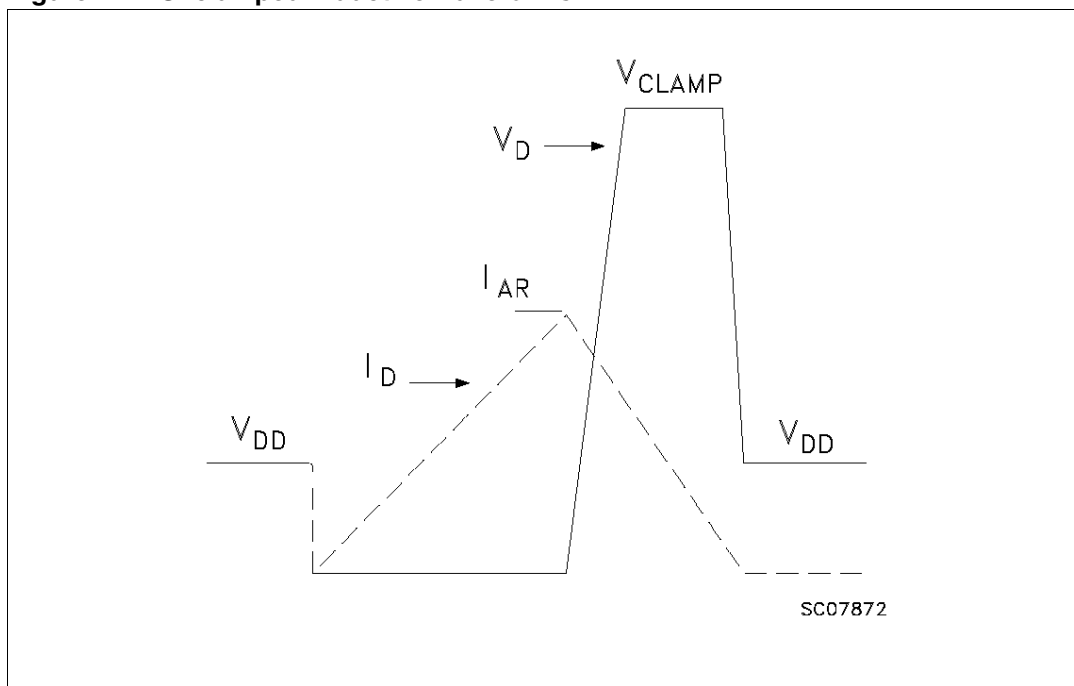
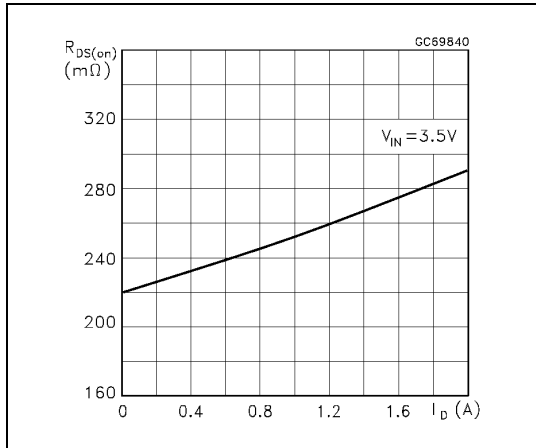


Figure 7. Unclamped inductive waveforms

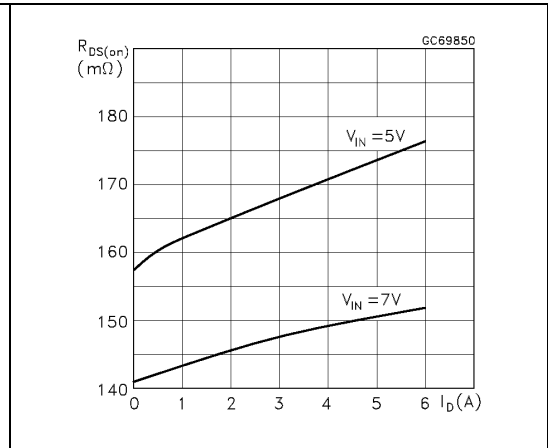


## 2.4 Electrical characteristics curves

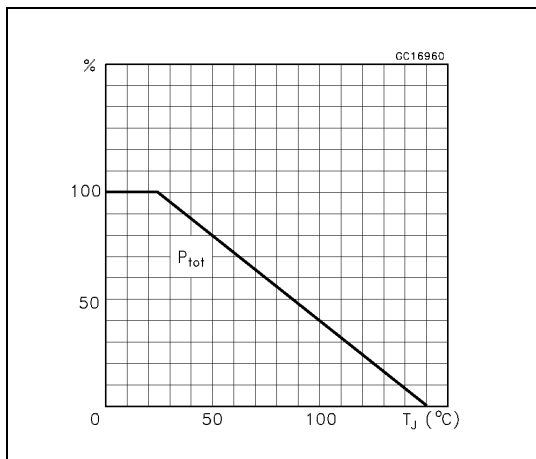
**Figure 8. Static Drain-Source on resistance ( $V_{IN} = 3.5V$ )**



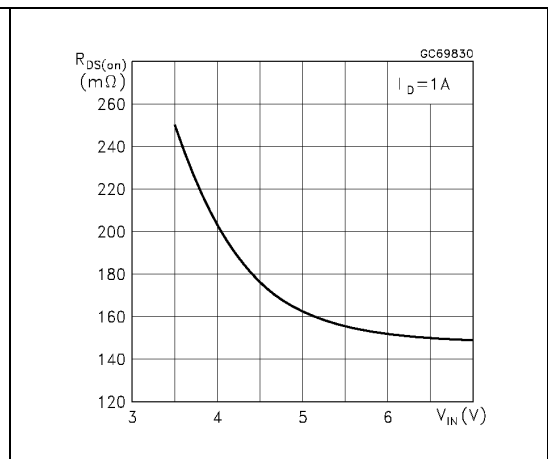
**Figure 9. Static Drain-Source on resistance ( $V_{IN} = 5V$ )**



**Figure 10. Derating curve**



**Figure 11. Static Drain-Source on resistance vs. input voltage**



**Figure 12. Current limit Vs. junction temperature**

**Figure 13. Source-Drain diode voltage Vs. junction temperature**

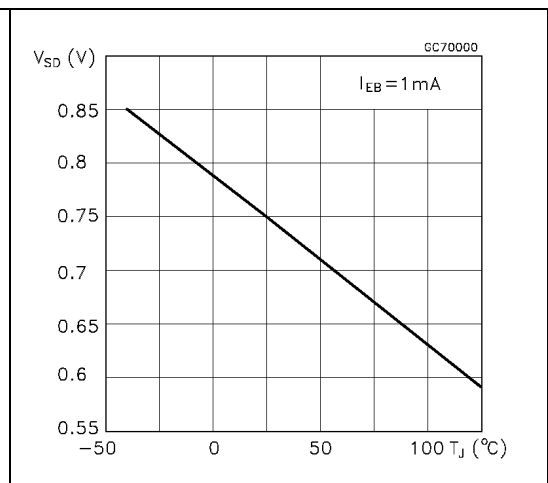
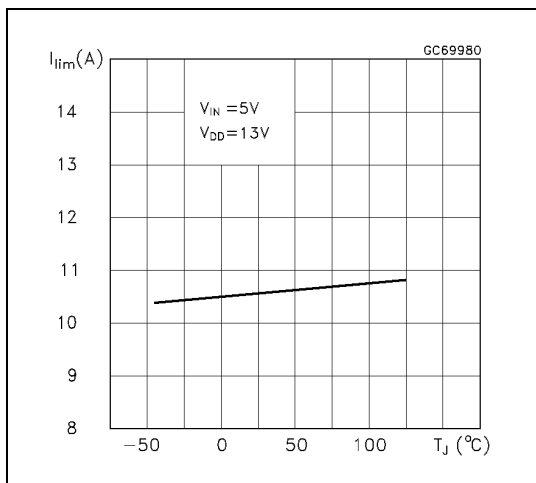


Figure 14. Step response current limit

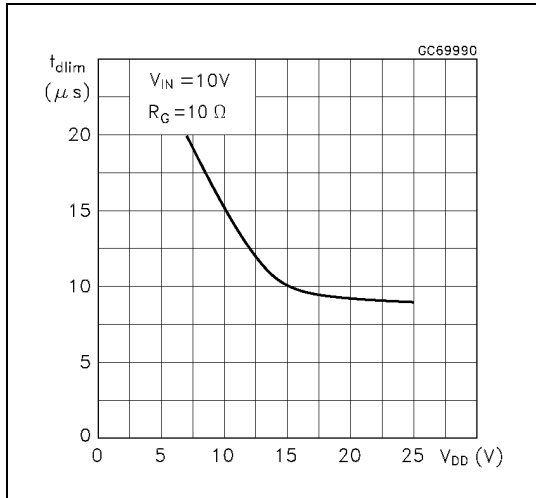


Figure 15. Switching time resistive load

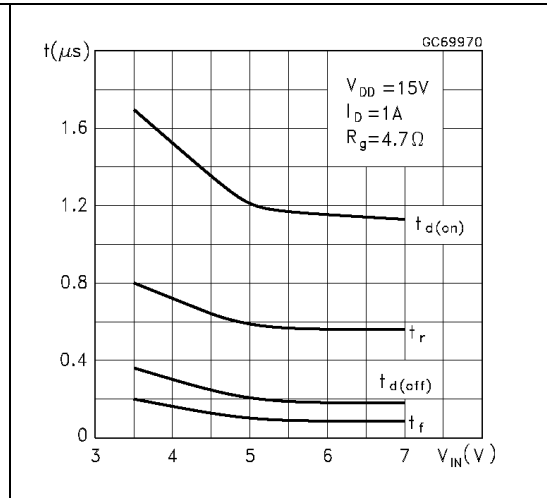


Figure 16. Turn-on current slope ( $V_{IN} = 3.5V$ )

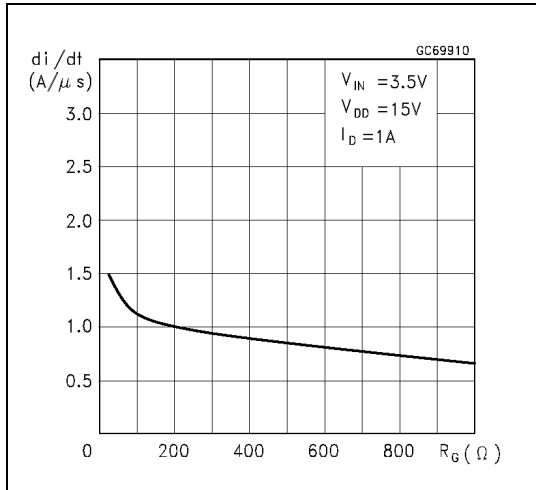


Figure 17. Turn-on current slope ( $V_{IN} = 7V$ )

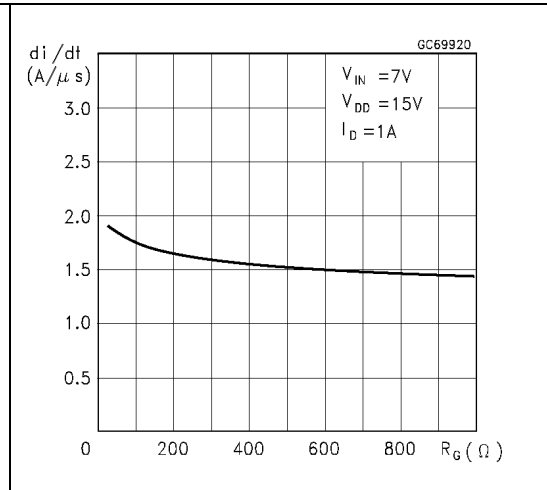


Figure 18. Input voltage Vs. input charge

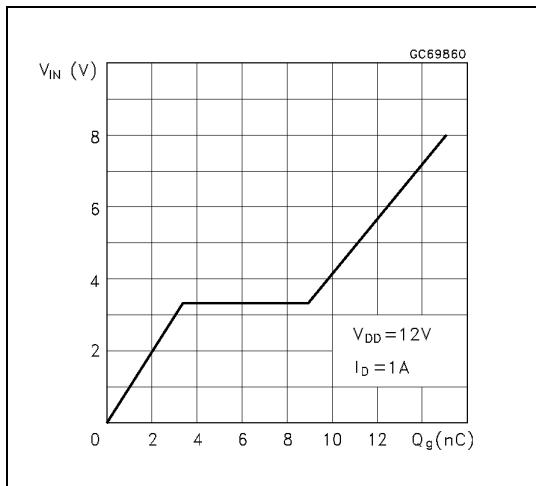
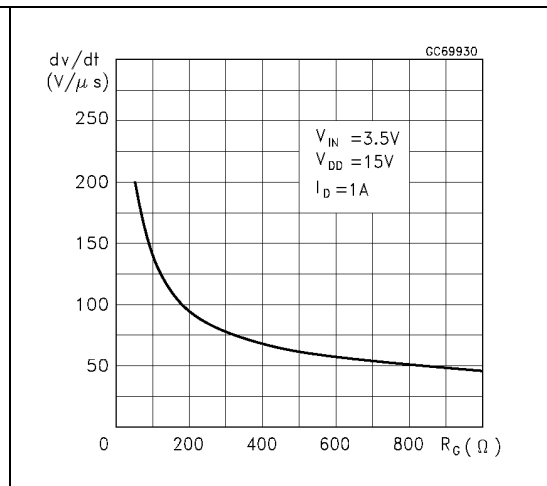
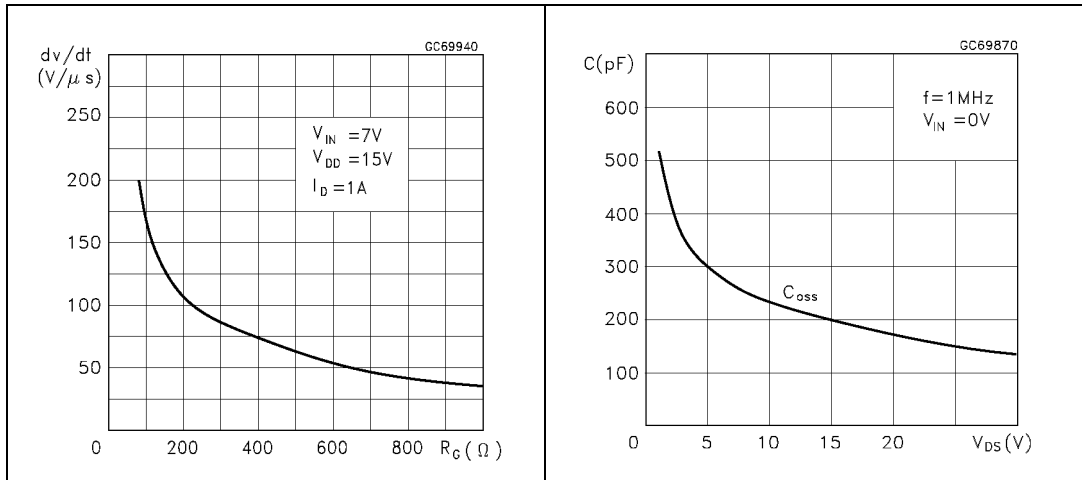


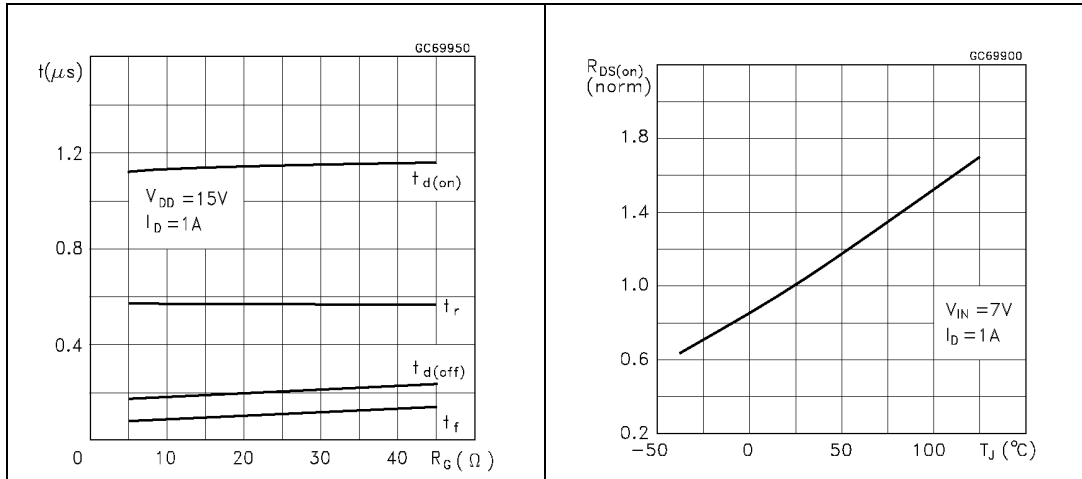
Figure 19. Turn-off Drain-Source voltage slope



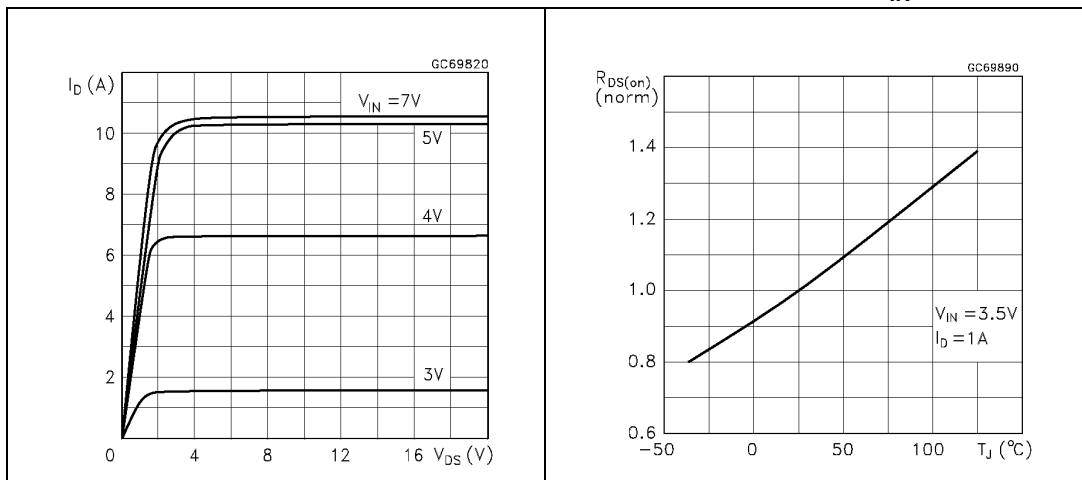
**Figure 20. Turn-off Drain-Source voltage slope** **Figure 21. Capacitance variations**



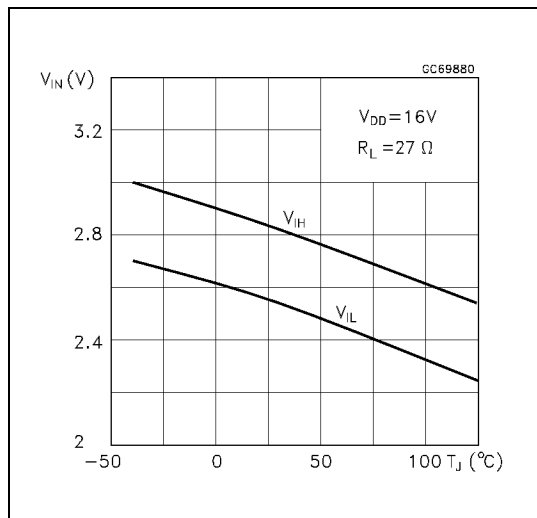
**Figure 22. Switching time resistive load** **Figure 23. Normalized on resistance Vs. temperature ( $V_{IN} = 7V$ )**



**Figure 24. Output characteristics** **Figure 25. Normalized on resistance Vs. temperature ( $V_{IN} = 3.5V$ )**



**Figure 26. Normalized input threshold voltage Vs. temperature**



### 3 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path as soon as  $V_{IN} > V_{IH}$ .

The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50KHz. The only difference from the user's standpoint is that a small DC current  $I_{ISS}$  flows into the INPUT pin in order to supply the internal circuitry.

During turn-off of an unclamped inductive load the output voltage is clamped to a safe level by an integrated Zener clamp between DRAIN pin and the gate of the internal Power MOSFET.

In this condition, the Power MOSFET gate is set to a voltage high enough to sustain the inductive load current even if the INPUT pin is driven to 0V. The device integrates an active current limiter circuit which limits the drain current  $I_D$  to  $I_{lim}$  whatever the INPUT pin Voltage.

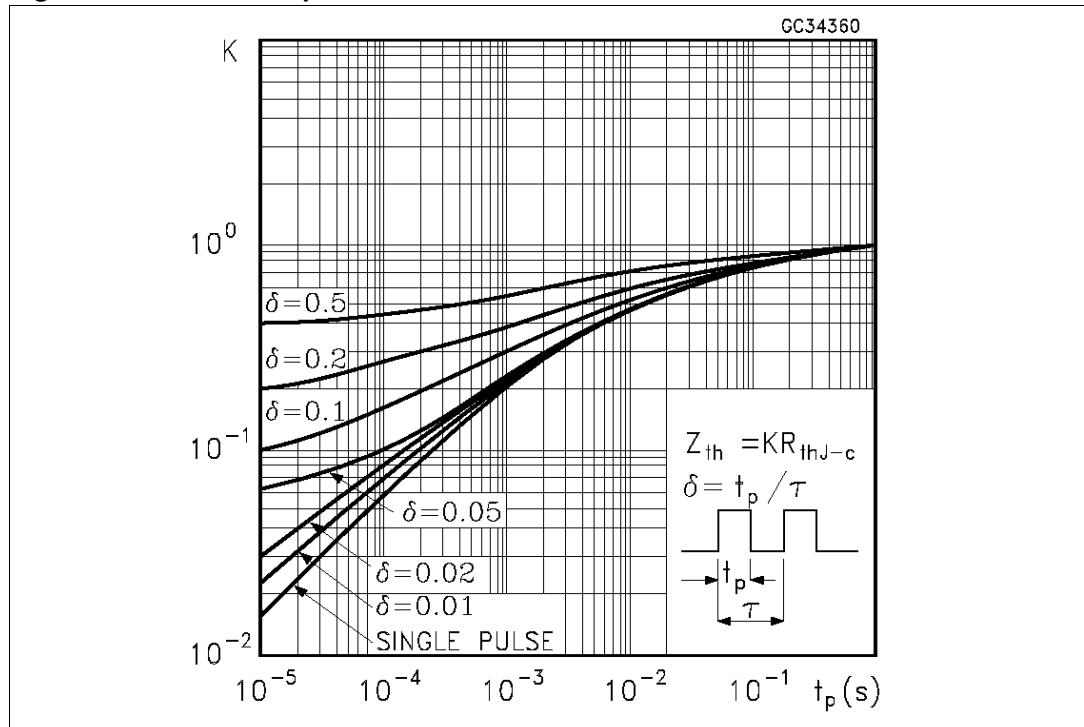
When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the heatsinking capability. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold  $T_{jsh}$ .

If  $T_j$  reaches  $T_{jsh}$ , the device shuts down whatever the INPUT pin voltage. The device will restart automatically when  $T_j$  has cooled down to  $T_{jrs}$ .



## 4 Thermal data

Figure 27. Thermal impedance for DPAK / IPAK



## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 5.2 DPAK mechanical data

Figure 28. DPAK package dimensions

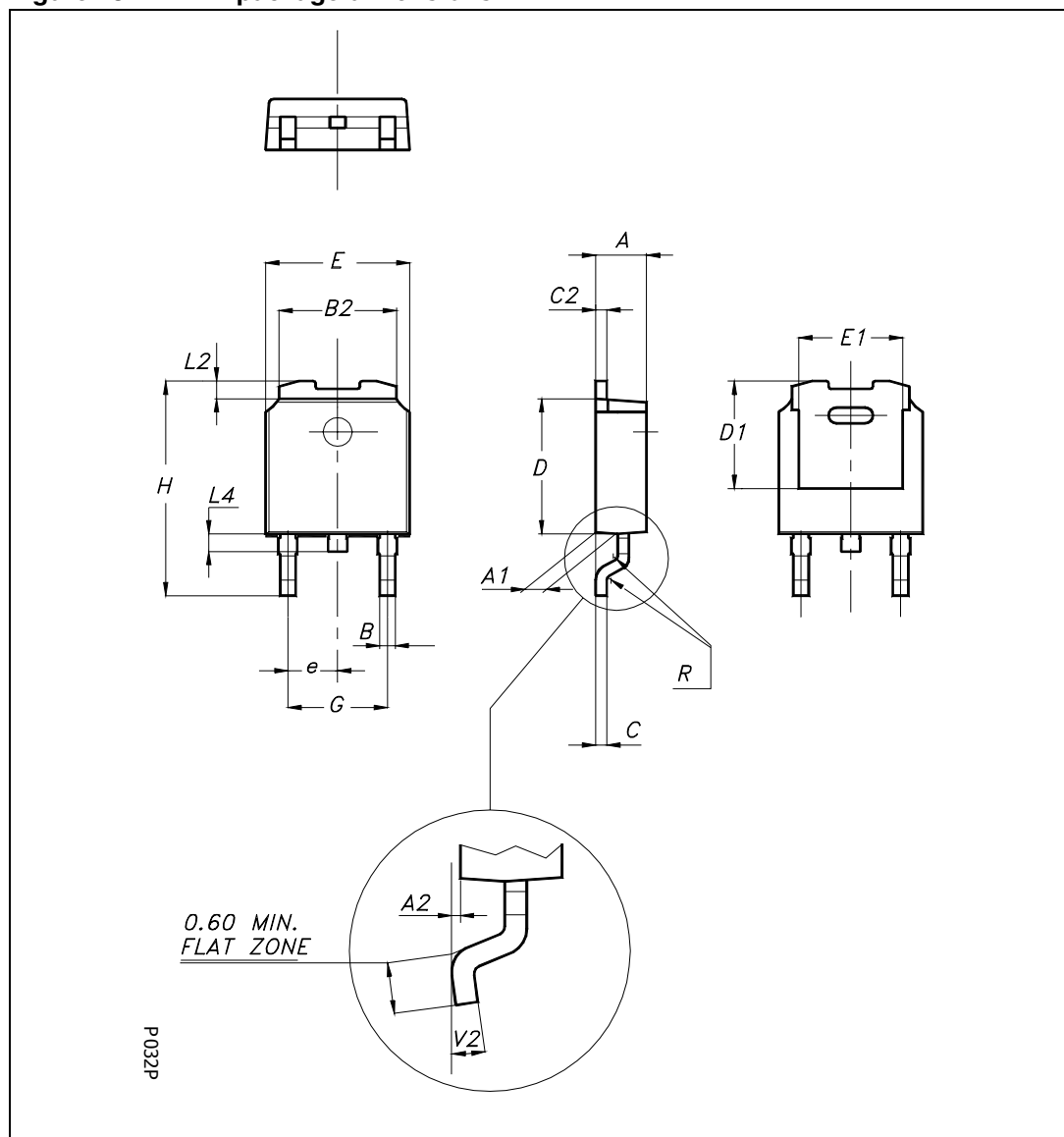


Table 10. DPAK mechanical data

| Dim.           | Millimeters |      |       |
|----------------|-------------|------|-------|
|                | Min.        | Typ. | Max.  |
| A              | 2.20        |      | 2.40  |
| A1             | 0.90        |      | 1.10  |
| A2             | 0.03        |      | 0.23  |
| B              | 0.64        |      | 0.90  |
| B2             | 5.20        |      | 5.40  |
| C              | 0.45        |      | 0.60  |
| C2             | 0.48        |      | 0.60  |
| D              | 6.00        |      | 6.20  |
| D1             |             | 5.1  |       |
| E              | 6.40        |      | 6.60  |
| E1             |             | 4.7  |       |
| e              |             | 2.28 |       |
| G              | 4.40        |      | 4.60  |
| H              | 9.35        |      | 10.10 |
| L2             |             | 0.8  |       |
| L4             | 0.60        |      | 1.00  |
| R              |             | 0.2  |       |
| V2             | 0°          | 8°   |       |
| Package weight | Gr. 0.29    |      |       |

### 5.3 IPAK mechanical data

Figure 29. IPAK mechanical data and package outline

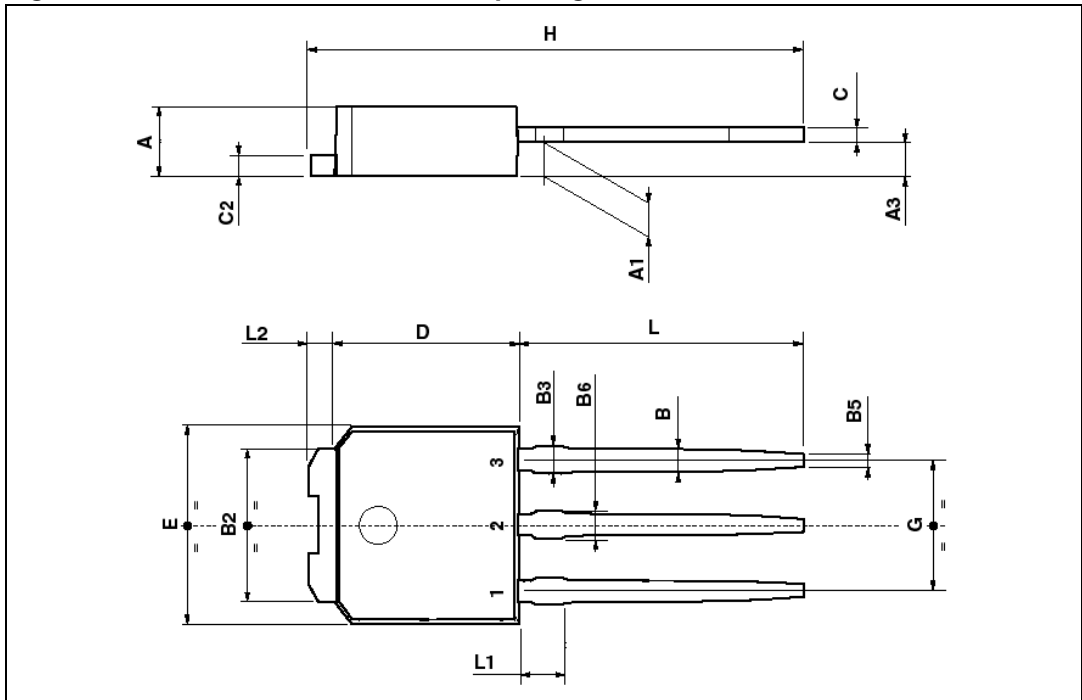


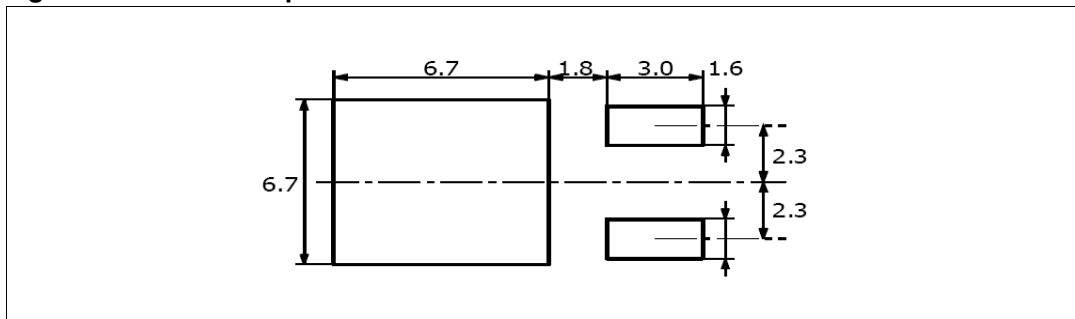
Table 11. IPAK mechanical data

| Symbol | Millimeters |      |      |
|--------|-------------|------|------|
|        | Min.        | Typ. | Max. |
| A      | 2.2         |      | 2.4  |
| A1     | 0.9         |      | 1.1  |
| A3     | 0.7         |      | 1.3  |
| B      | 0.64        |      | 0.9  |
| B2     | 5.2         |      | 5.4  |
| B3     |             |      | 0.85 |
| B5     |             | 0.3  |      |
| B6     |             |      | 0.95 |
| C      | 0.45        |      | 0.6  |
| C2     | 0.48        |      | 0.6  |
| D      | 6           |      | 6.2  |
| E      | 6.4         |      | 6.6  |
| G      | 4.4         |      | 4.6  |
| H      | 15.9        |      | 16.3 |
| L      | 9           |      | 9.4  |
| L1     | 0.8         |      | 1.2  |
| L2     |             | 0.8  | 1    |

## 5.4 DPAK packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

**Figure 30. DPAK footprint**



**Figure 31. DPAK tube shipment (no suffix)**

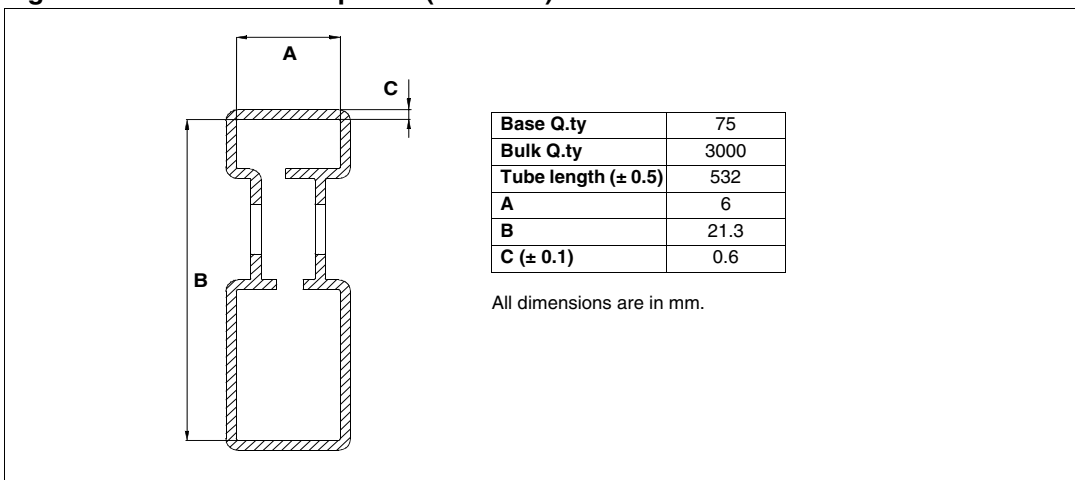
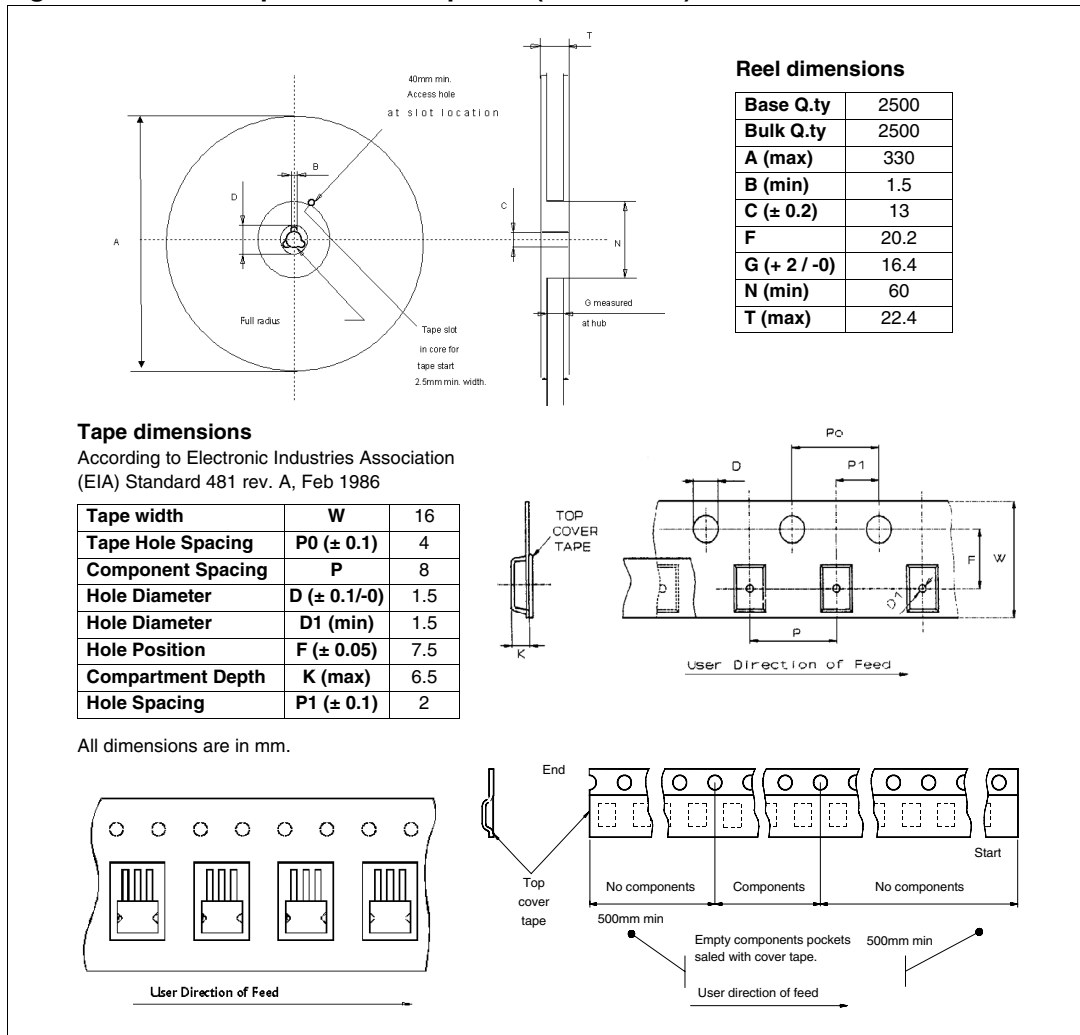
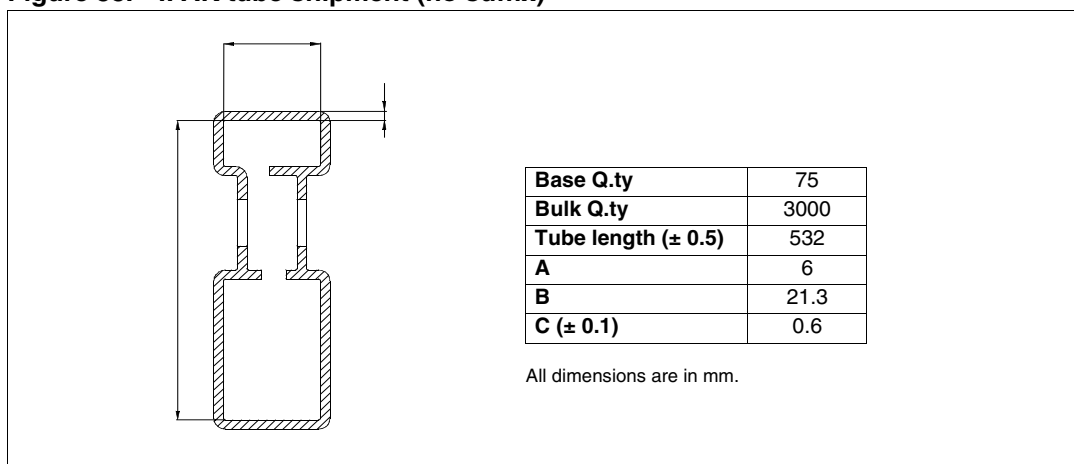


Figure 32. DPAK tape and reel shipment (suffix "TR")



## 5.5 IPAK packing information

Figure 33. IPAK tube shipment (no suffix)



## 6 Revision history

**Table 12. Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| Oct-1997    | 1        | Initial release.  |
| 22-Aug-2006 | 2        | Document restructured.  |
| 12-Dec-2008 | 3        | Document restructured and reformatted.<br>Added <i>ECOPACK® packages</i> information. |
| 25-Sep-2013 | 4        | Updated disclaimer.   |



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