



## VND5E025AK-E

### Double channel high side driver with analog current sense for automotive applications

#### Features

Max transient supply voltage	$V_{CC}$	41V
Operating voltage range	$V_{CC}$	4.5 to 28V
Max On-state resistance (per ch.)	$R_{ON}$	25m $\Omega$
Current limitation (typ)	$I_{LIMH}$	60A
Off state supply current	$I_S$	2 $\mu$ A <sup>(1)</sup>

1. Typical value with all loads connected.

#### ■ General

- Inrush current active management by power limitation
- Very low stand-by current
- 3.0V CMOS compatible inputs
- Optimized electromagnetic emissions
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC european directive
- Very low current sense leakage

#### ■ Diagnostic functions

- Proportional load current sense
- High current sense precision for wide currents range
- Current sense disable
- Off state open load detection
- Output short to  $V_{CC}$  detection
- Overload and short to ground (power limitation) indication
- Thermal shutdown indication

#### ■ Protections

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of  $V_{CC}$
- Over-temperature shutdown with autorestart (thermal shut down)



PowerSSO-24

- Reverse battery protected (see [Figure 32.](#))
- Electrostatic discharge protection

#### Application

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

#### Description

The VND5E025AK-E is a double channel high-side drivers manufactured in the ST proprietary VIPower M0-5 technology and housed in the tiny PowerSSO-24 package. The VND5E025AK-E is designed to drive 12V automotive grounded loads delivering protection, diagnostics and easy 3V and 5V CMOS compatible interface with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, over-temperature shut-off with auto-restart and over-voltage active clamp. A dedicated analog current sense pin is associated with every output channel in order to provide *Enhanced* diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, over-temperature indication, short-circuit to  $V_{CC}$  diagnosis and ON & OFF state open load detection. The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS\_DIS pin high to allow sharing of the external sense resistor with other similar devices.

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# 1 Block diagram and pin description

Figure 1. Block diagram

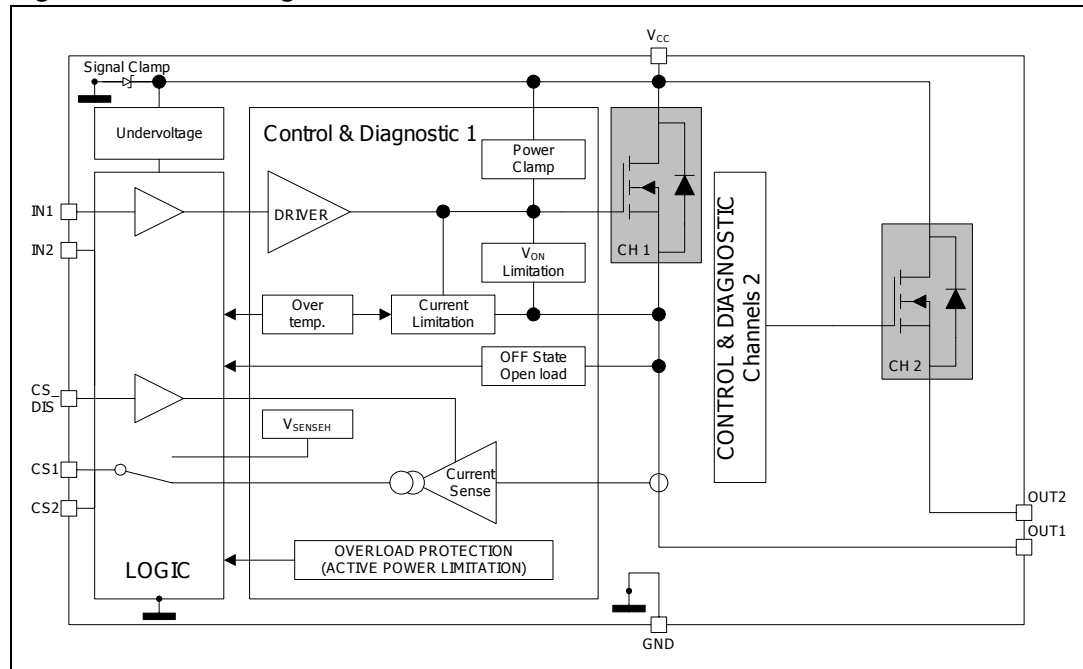


Table 1. Pin functions

Name	Function
$V_{CC}$	Battery connection.
OUTPUT <sub>1,2</sub>	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT <sub>1,2</sub>	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE <sub>1,2</sub>	Analog current sense pin; delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin to disable the current sense pin.

Figure 2. Configuration diagram (top view)

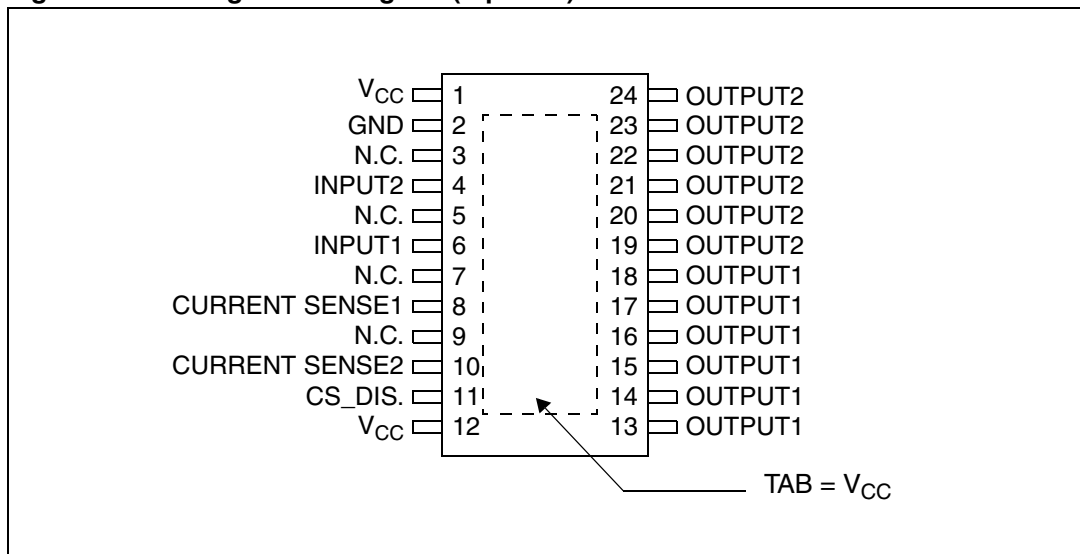
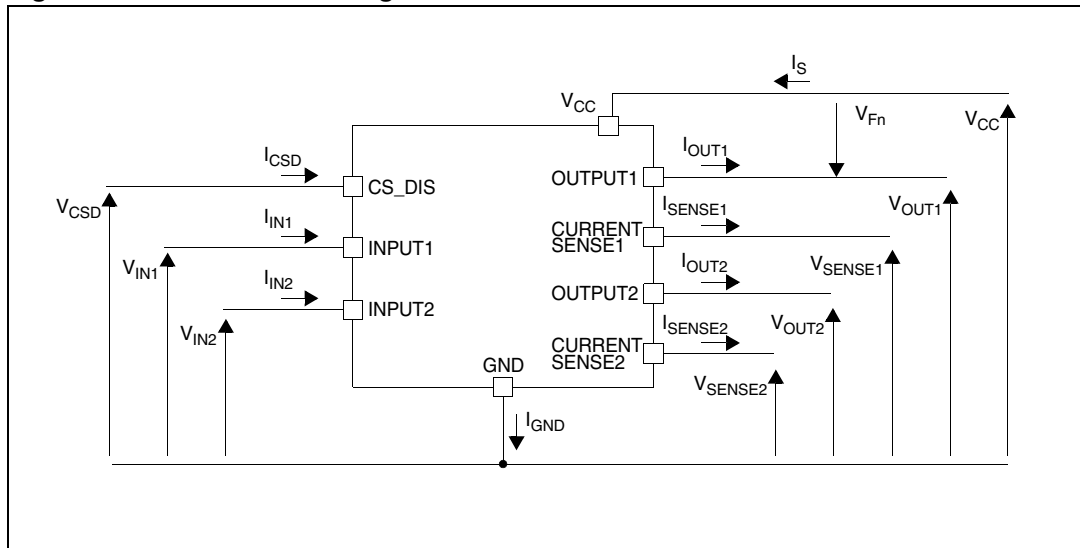


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1k $\Omega$ resistor	X	Through 22k $\Omega$ resistor	Through 10k $\Omega$ resistor	Through 10k $\Omega$ resistor

## 2 Electrical specification

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

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Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	24	
$I_{IN}$	DC input current	-1 to 10	mA
$I_{CSD}$	DC current sense disable input current		
$-I_{CSENSE}$	DC reverse CS pin current		
$V_{CSENSE}$	Current sense maximum voltage	$V_{CC} - 41$ to $+V_{CC}$	V

**Table 3. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
$E_{MAX}$	Maximum switching energy (single pulse) ( $L = 0.8 \text{ mH}$ ; $R_L = 0\Omega$ ; $V_{bat} = 13.5\text{V}$ ; $T_{jstart} = 150^\circ\text{C}$ ; $I_{OUT} = I_{limL}(Typ.)$ )	140	mJ
$V_{ESD}$	Electrostatic discharge (Human Body Model: $R = 1.5\text{k}\Omega$ ; $C = 100\text{pF}$ )		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- CS_DIS	4000	V
	- OUTPUT	5000	V
	- $V_{CC}$	5000	V
$V_{ESD}$	Charge device model (CDM-AEC-Q100-011)	750	V
$T_j$	Junction operating temperature	- 40 to 150	°C
$T_{stg}$	Storage temperature	- 55 to 150	

## 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	1.35	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See <a href="#">Figure 36</a>	



## 2.3 Electrical characteristics

Values specified in this section are for  $8V < V_{CC} < 28V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$ , unless otherwise stated.

**Table 5. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		4.5	13	28	V
$V_{USD}$	Undervoltage shutdown			3.5	4.5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		
$R_{ON}$	On state resistance <sup>(1)</sup>	$I_{OUT} = 3A$ ; $T_j = 25^{\circ}C$			25	m $\Omega$
		$I_{OUT} = 3A$ ; $T_j = 150^{\circ}C$			50	
		$I_{OUT} = 3A$ ; $V_{CC} = 5V$ ; $T_j = 25^{\circ}C$			35	
$V_{clamp}$	Clamp voltage	$I_S = 20$ mA	41	46	52	V
$I_S$	Supply current	Off State; $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$ ; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0V$		2 <sup>(2)</sup>	5 <sup>(2)</sup>	$\mu A$
		On State; $V_{CC} = 13V$ ; $V_{IN} = 5V$ ; $I_{OUT} = 0A$		3	6	mA
$I_{L(off1)}$	Off state output current <sup>(1)</sup>	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$	0	0.01	3	$\mu A$
		$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 125^{\circ}C$	0		5	
$V_F$	Output - $V_{CC}$ diode voltage <sup>(1)</sup>	$-I_{OUT} = 4$ A; $T_j = 150^{\circ}C$			0.7	V

1. For each channel.
2. PowerMOS leakage included.

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**Table 6. Switching ( $V_{CC} = 13V$ ;  $T_j = 25^{\circ}C$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On delay time	$R_L = 4.3 \Omega$ (see <a href="#">Figure 6</a> )		20		$\mu s$
$t_{d(off)}$	Turn-Off delay time			40		
$(dV_{OUT}/dt)_{on}$	Turn-On voltage slope	$R_L = 4.3 \Omega$		See <a href="#">Figure 27</a>		V/ $\mu s$
$(dV_{OUT}/dt)_{off}$	Turn-Off voltage slope			See <a href="#">Figure 28</a>		
$W_{ON}$	Switching energy losses during $t_{WON}$	$R_L = 4.3 \Omega$ (see <a href="#">Figure 6</a> )		0.6		mJ
$W_{OFF}$	Switching energy losses during $t_{WOFF}$			0.35		

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Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.9	V
$I_{IL}$	Low level input current	$V_{IN} = 0.9V$	1			$\mu A$
$V_{IH}$	Input high level voltage		2.1			V
$I_{IH}$	High level input current	$V_{IN} = 2.1V$			10	$\mu A$
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1mA$	5.5		7	
		$I_{IN} = -1mA$		-0.7		
$V_{CSDL}$	CS_DIS low level voltage				0.9	
$I_{CSDL}$	Low level CS_DIS current	$V_{CSD} = 0.9V$	1			$\mu A$
$V_{CSDH}$	CS_DIS high level voltage		2.1			V
$I_{CSDH}$	High level CS_DIS current	$V_{CSD} = 2.1V$			10	$\mu A$
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
$V_{CSCL}$	CS_DIS clamp voltage	$I_{CSD} = 1mA$	5.5		7	
		$I_{CSD} = -1mA$		-0.7		

Table 8. Protections and diagnostics (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{LIMH}$	DC short circuit current	$V_{CC} = 13V$	43	60	85	A
		$5V < V_{CC} < 28V$				
$I_{LIML}$	Short circuit current during thermal cycling	$V_{CC} = 13V$ ; $T_R < T_j < T_{TSD}$		15		
$T_{TSD}$	Shutdown temperature		150	175	200	°C
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		
$T_{RS}$	Thermal reset of STATUS		135			
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		
$V_{DEMAG}$	Turn-Off output voltage clamp	$I_{OUT} = 2A$ ; $V_{IN} = 0$ ; $L = 6 mH$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 0.1A$ ; $T_j = -40^\circ C$ to $+150^\circ C$ (see <a href="#">Figure 8</a> )		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense ( $8V < V_{CC} < 18V$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$K_{LED}$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 0.05A; V_{SENSE} = 0.5V; V_{CSD} = 0V;$ $T_j = -40^{\circ}C \text{ to } 150^{\circ}C$	1240	3350	4960	
$K_0$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 0.5A; V_{SENSE} = 0.5V; V_{CSD} = 0V;$ $T_j = -40^{\circ}C \text{ to } 150^{\circ}C$	1860	3150	4600	
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 2 A; V_{SENSE} = 4 V;$ $V_{CSD} = 0V;$ $T_j = -40^{\circ}C \text{ to } 150^{\circ}C$ $T_j = 25^{\circ}C \text{ to } 150^{\circ}C$	2100 2250	3100 3100	4400 3850	
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT} = 2 A; V_{SENSE} = 4 V;$ $V_{CSD} = 0V;$ $T_j = -40^{\circ}C \text{ to } 150^{\circ}C$	-13		13	%
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 3 A; V_{SENSE} = 4V;$ $V_{CSD} = 0V;$ $T_j = -40^{\circ}C \text{ to } 150^{\circ}C$ $T_j = 25^{\circ}C \text{ to } 150^{\circ}C$	2200 2450	3000 3000	4100 3550	
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT} = 3 A; V_{SENSE} = 4V; V_{CSD} = 0V;$ $T_j = -40^{\circ}C \text{ to } 150^{\circ}C$	-12		12	%
$K_3$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 10 A; V_{SENSE} = 4V;$ $V_{CSD} = 0V;$ $T_j = -40^{\circ}C \text{ to } 150^{\circ}C$ $T_j = 25^{\circ}C \text{ to } 150^{\circ}C$	2550 2650	2850 2850	3280 3180	
$dK_3/K_3^{(1)}$	Current sense ratio drift	$I_{OUT} = 10 A; V_{SENSE} = 4V; V_{CSD} = 0V;$ $T_j = -40^{\circ}C \text{ to } 150^{\circ}C$	-6		+6	%
$I_{SENSE0}$	Analog sense leakage current	$I_{OUT} = 0A; V_{SENSE} = 0V;$ $V_{CSD} = 5V; V_{IN} = 0V; T_j = -40^{\circ}C \text{ to } 150^{\circ}C$ $V_{CSD} = 0V; V_{IN} = 5V; T_j = -40^{\circ}C \text{ to } 150^{\circ}C$ $I_{OUT} = 2A; V_{SENSE} = 0V;$ $V_{CSD} = 5V; V_{IN} = 5V; T_j = -40^{\circ}C \text{ to } 150^{\circ}C$	0 0 0		1 2 1	$\mu A$ $\mu A$ $\mu A$
$I_{OL}$	Openload ON state current detection threshold	$V_{IN} = 5V, 8V < V_{CC} < 18V$ $I_{SENSE} = 5 \mu A$	5		30	mA
$V_{SENSE}$	Max analog sense output voltage	$I_{OUT} = 3 A; V_{CSD} = 0V$	5			V
$V_{SENSEH}$	Analog sense output voltage in fault condition <sup>(1)</sup>	$V_{CC} = 13V; R_{SENSE} = 3.9k\Omega$		8		
$I_{SENSEH}$	Analog sense output current in fault condition <sup>(2)</sup>	$V_{CC} = 13V; V_{SENSE} = 5V$		9		mA

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Table 9. Current sense (8V < V<sub>CC</sub> < 18V) (continued)

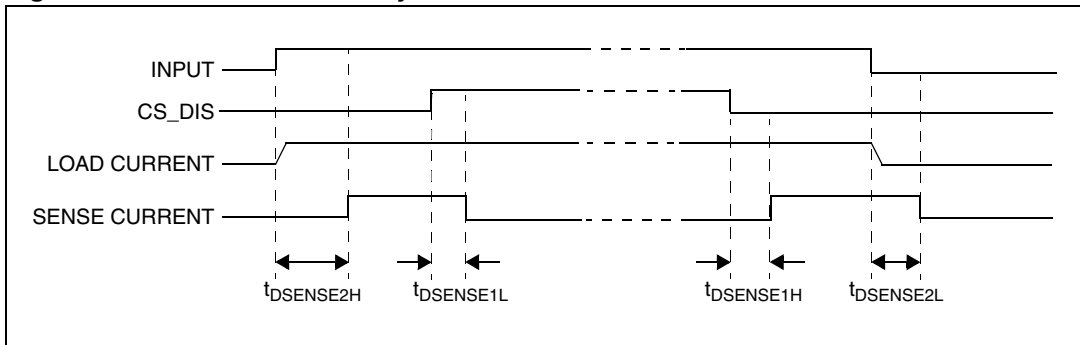
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>DSENSE1H</sub>	Delay response time from falling edge of CS_DIS pin	V <sub>SENSE</sub> < 4V, 0.5 < I <sub>OUT</sub> < 10A I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> (see Figure 4)		30	100	μs
t <sub>DSENSE1L</sub>	Delay response time from rising edge of CS_DIS pin	V <sub>SENSE</sub> < 4V, 0.5 < I <sub>OUT</sub> < 10A I <sub>SENSE</sub> = 10% of I <sub>SENSEMAX</sub> (see Figure 4)		5	20	
t <sub>DSENSE2H</sub>	Delay response time from rising edge of INPUT pin	V <sub>SENSE</sub> < 4V, 0.5 < I <sub>OUT</sub> < 10A I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> (see Figure 4)		80	300	
Δt <sub>DSENSE2H</sub>	Delay response time between rising edge of output current and rising edge of current sense	V <sub>SENSE</sub> < 4V, I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> , I <sub>OUT</sub> = 90% of I <sub>OUTMAX</sub> , I <sub>OUTMAX</sub> = 3A (see Figure 7)			110	
t <sub>DSENSE2L</sub>	Delay response time from falling edge of INPUT pin	V <sub>SENSE</sub> < 4V, 0.5 < I <sub>OUT</sub> < 10A I <sub>SENSE</sub> = 10% of I <sub>SENSEMAX</sub> (see Figure 4)		70	250	

1. Fault condition includes: power limitation, overtemperature and open load OFF state detection.

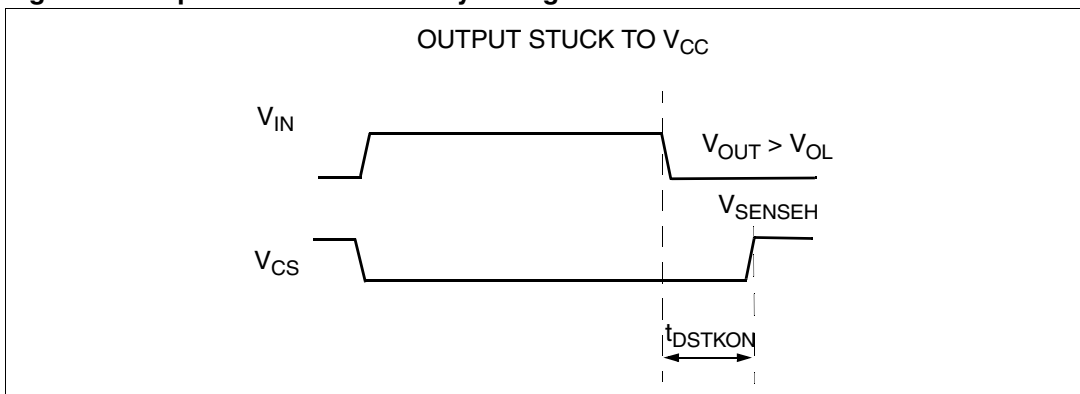
Table 10. Openload detection (8V < V<sub>CC</sub> < 18V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V <sub>OL</sub>	Openload Off State voltage detection threshold	V <sub>IN</sub> = 0V	2	See Figure 5	4	V
t <sub>DSTKON</sub>	Output short circuit to V <sub>CC</sub> detection delay at turn Off	See Figure 5	180		1200	μs
I <sub>L(off2)r</sub>	Off state output current at V <sub>OUT</sub> = 4V	V <sub>IN</sub> =0V; V <sub>SENSE</sub> =0V V <sub>OUT</sub> rising from 0V to 4V	-120		0	μA
I <sub>L(off2)f</sub>	Off state output current at V <sub>OUT</sub> = 2V	V <sub>IN</sub> =0V; V <sub>SENSE</sub> =V <sub>SENSEH</sub> V <sub>OUT</sub> falling from V <sub>CC</sub> to 2V	-50		90	μA
td_vol	Delay response from output rising edge to V <sub>SENSE</sub> rising edge in openload	V <sub>OUT</sub> = 4 V; V <sub>IN</sub> = 0V V <sub>SENSE</sub> = 90% of V <sub>SENSEH</sub>			20	μs

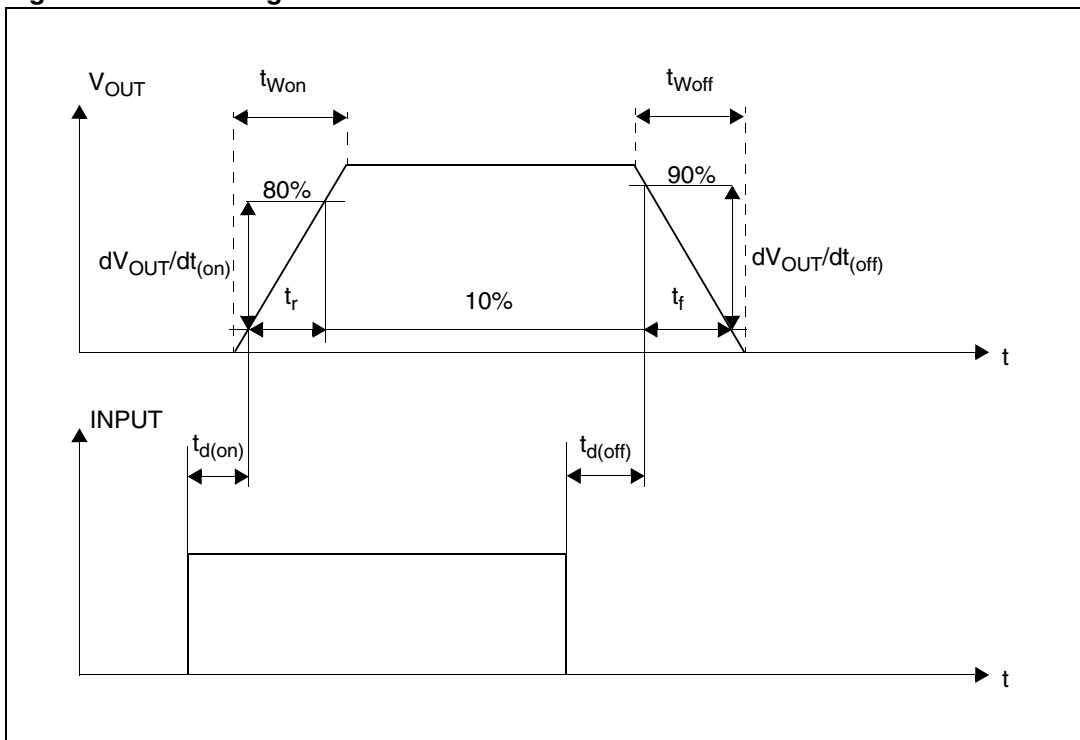
**Figure 4. Current sense delay characteristics**



**Figure 5. Openload Off-state delay timing**

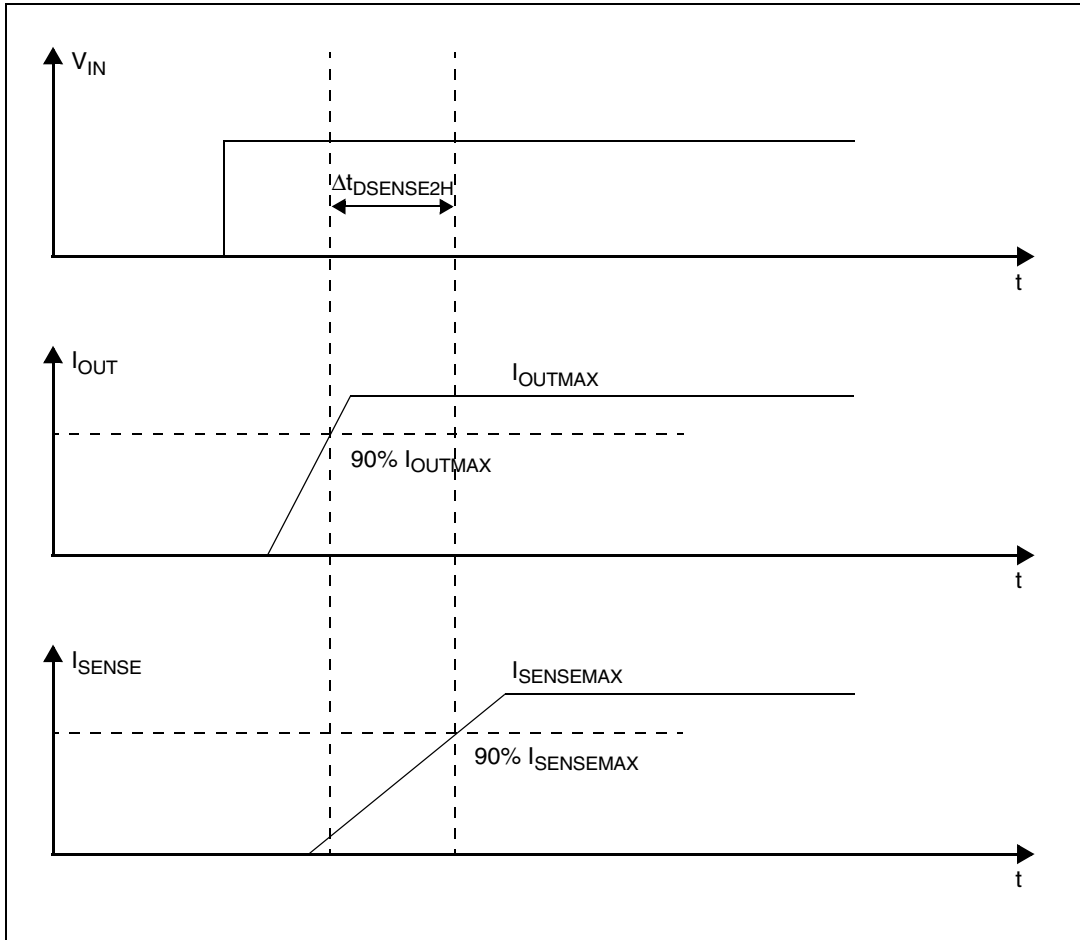


**Figure 6. Switching characteristics**



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**Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)**



**Figure 8. Output voltage drop limitation**

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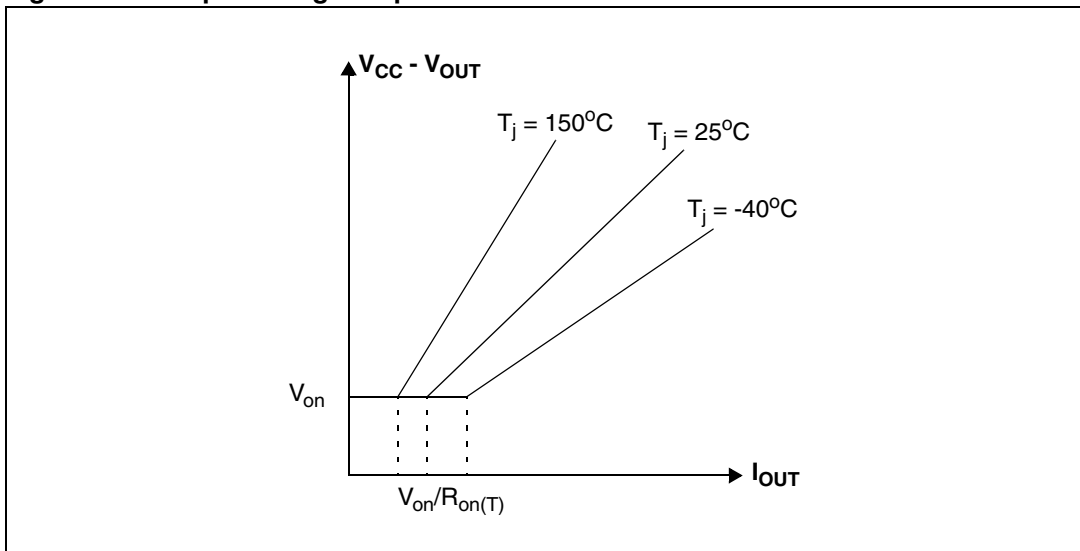


Figure 9.  $I_{OUT}/I_{SENSE}$  vs.  $I_{OUT}$

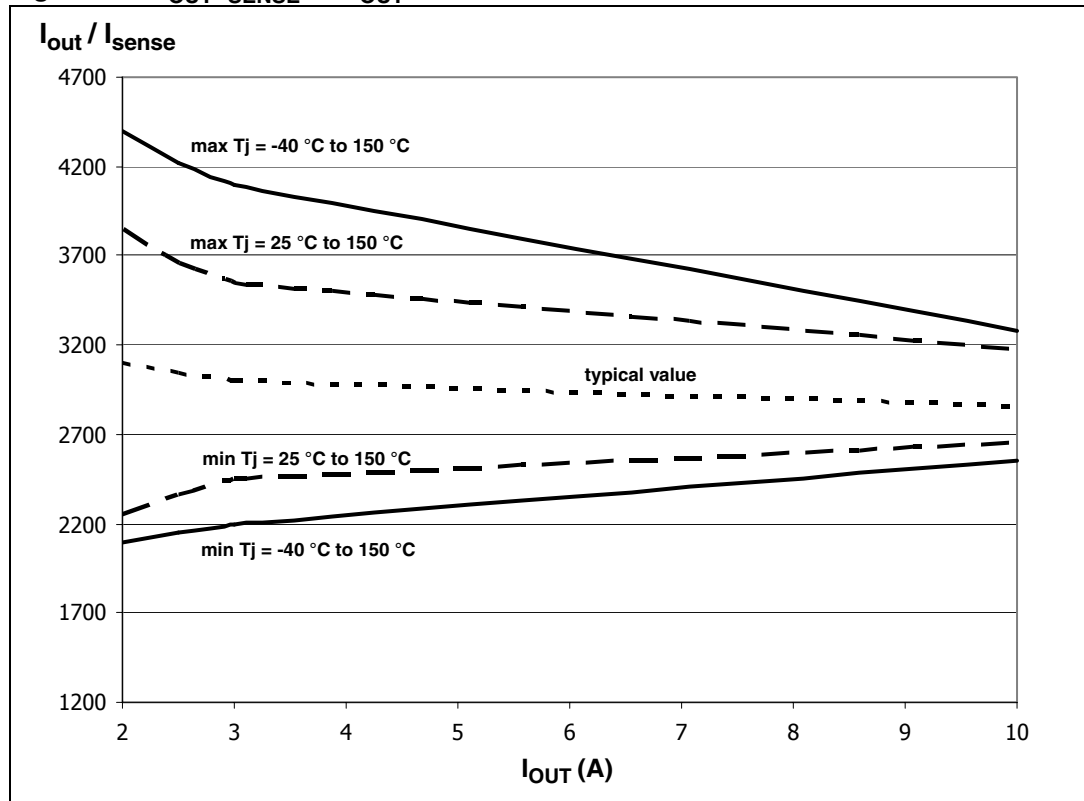
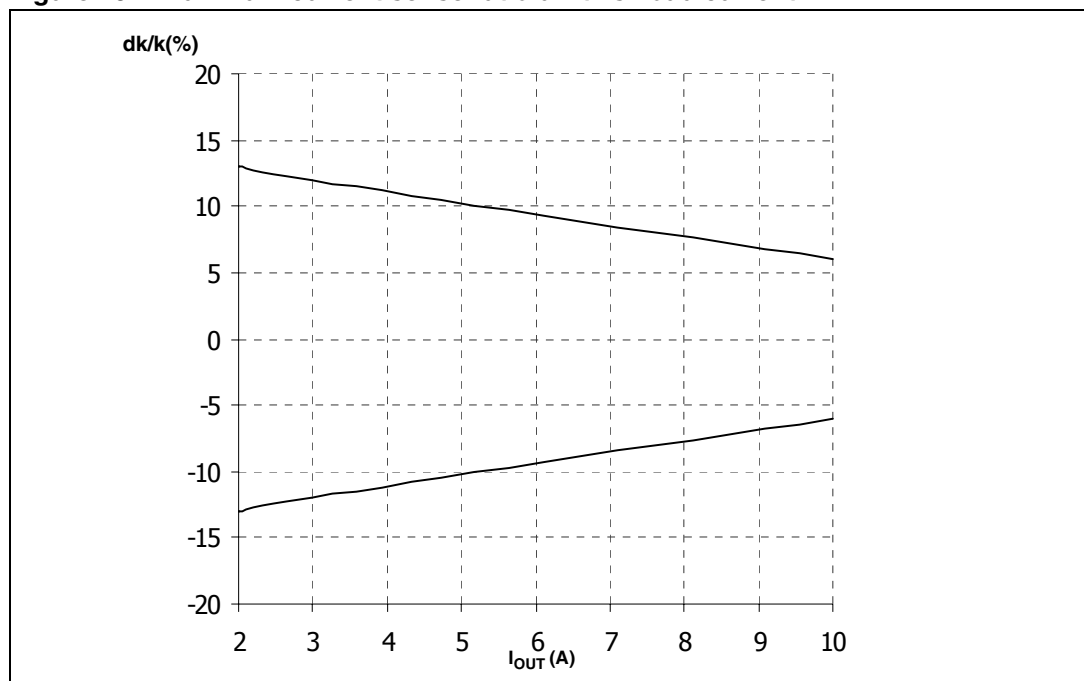


Figure 10. Maximum current sense ratio drift vs. load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense ( $V_{CSD}=0V$ ) <sup>(1)</sup>
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Overload	H	X (no power limitation)	Nominal
	H	Cycling (power limitation)	$V_{SENSEH}$
Short circuit to GND (Power limitation)	L	L	0
	H	L	$V_{SENSEH}$
Open load OFF state (with external pul up)	L	H	$V_{SENSEH}$
Short circuit to $V_{CC}$ (external pull up disconnected)	L	H	$V_{SENSEH}$
	H	H	$V_{SENSEH}$ < Nominal
Negative output voltage clamp	L	L	0

1. If the  $V_{CSD}$  is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.



Table 12. Electrical transient requirements

ISO 7637-2: 2004(E) Test pulse	Test levels <sup>(1)</sup>		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1μs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1μs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b <sup>(2)</sup>	+65V	+87V	1 pulse			400ms, 2Ω

ISO 7637-2: 2004E Test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b <sup>(2)</sup>	C	C

Class	Contents
C	All functions of the device <b>performed</b> as designed after exposure to disturbance.
E	One or more functions of the device <b>did not</b> perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

1. The above test levels must be considered referred to  $V_{CC} = 13.5V$  except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

## 2.4 Waveforms

Figure 11. Normal operation

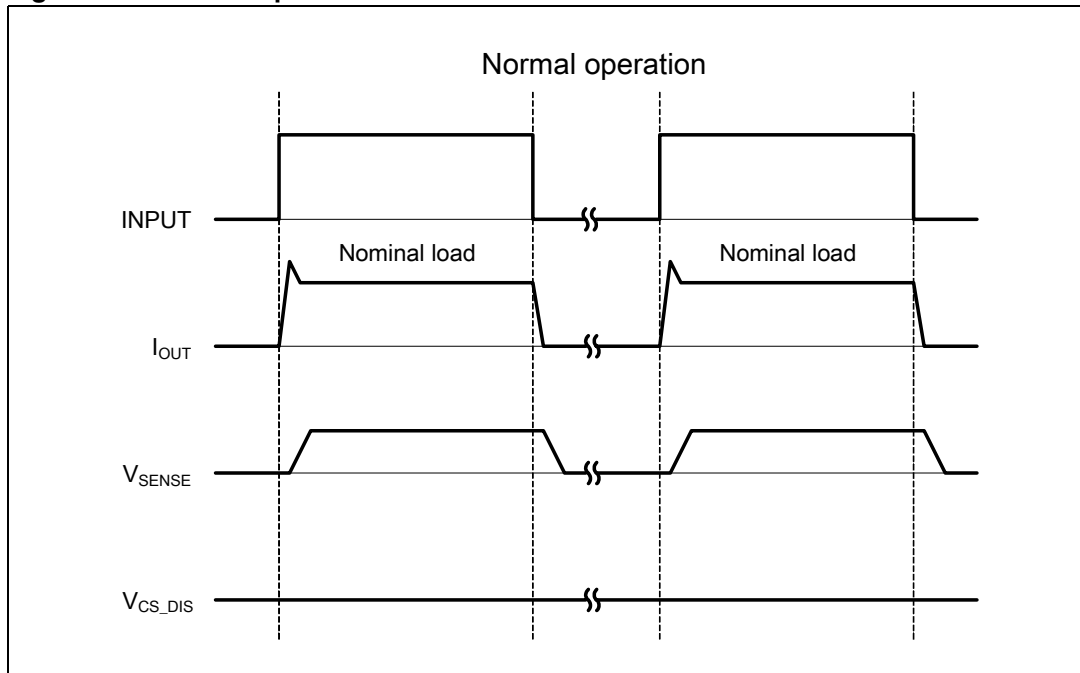


Figure 12. Overload or Short to GND

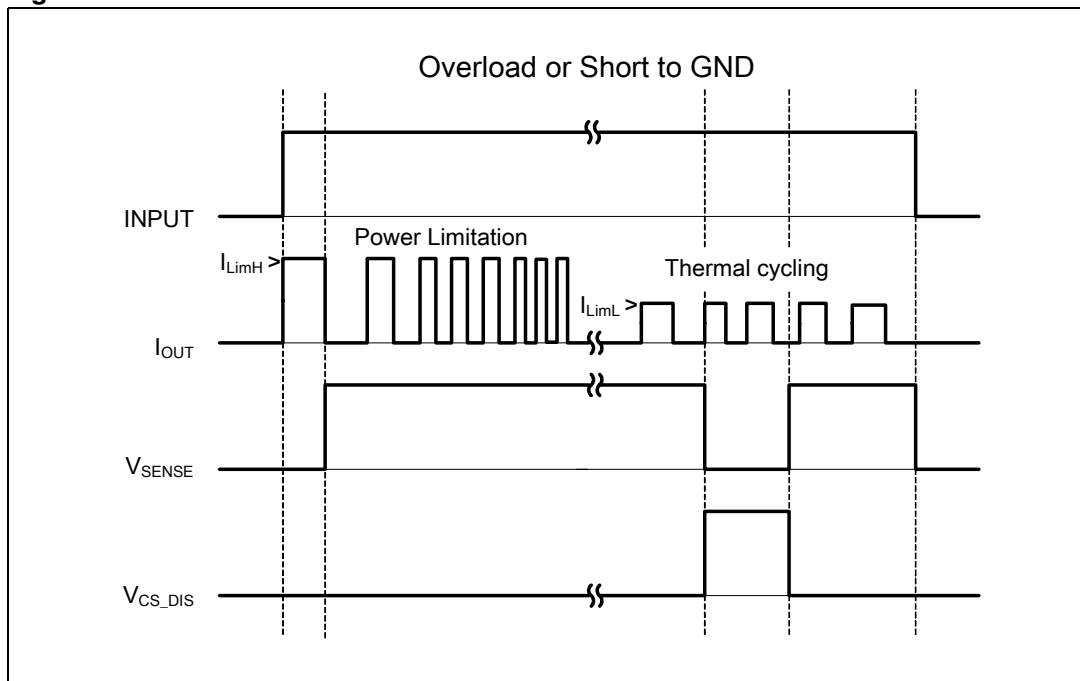


Figure 13. Intermittent Overload

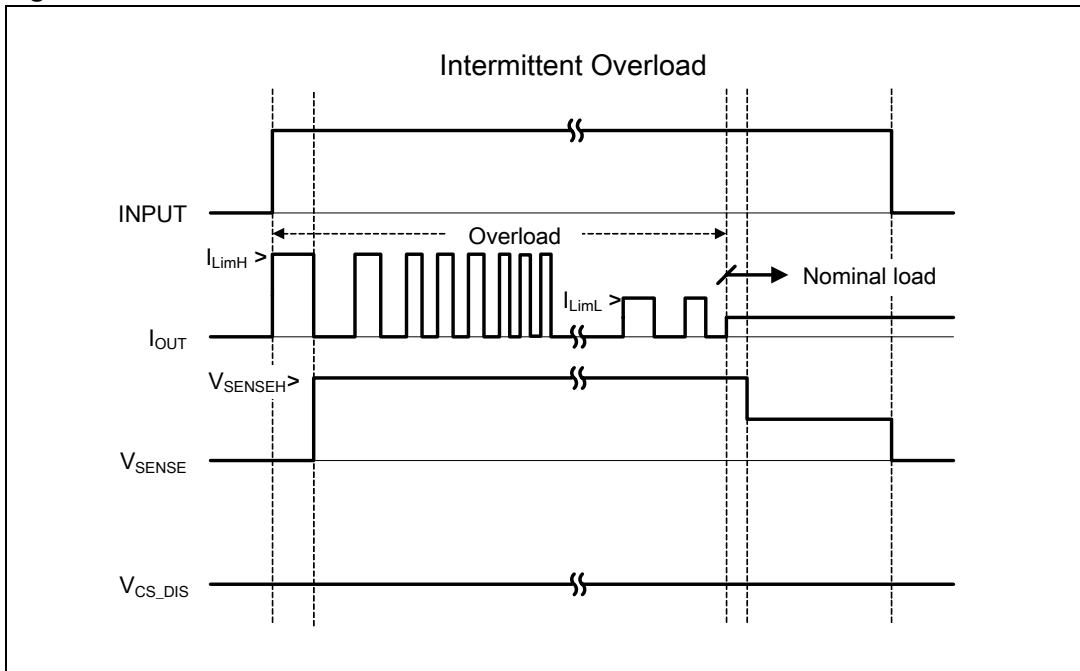
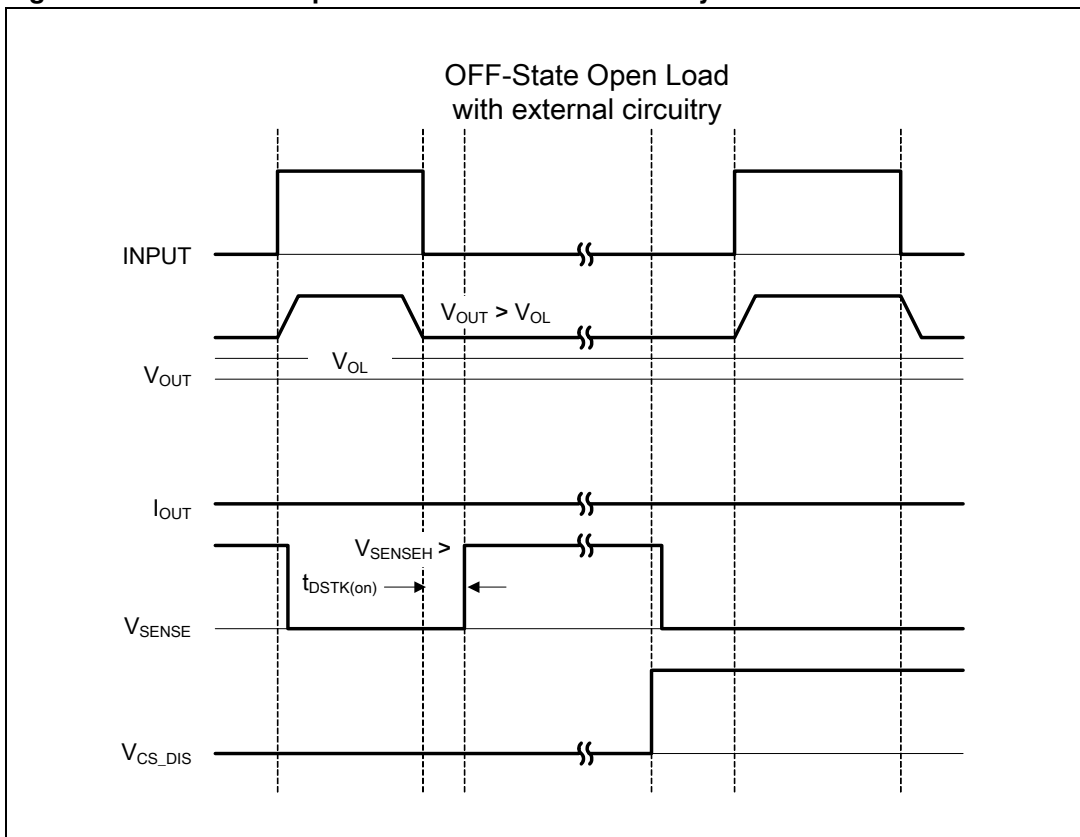


Figure 14. OFF-State Open Load with external circuitry



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Figure 15. Short to  $V_{CC}$

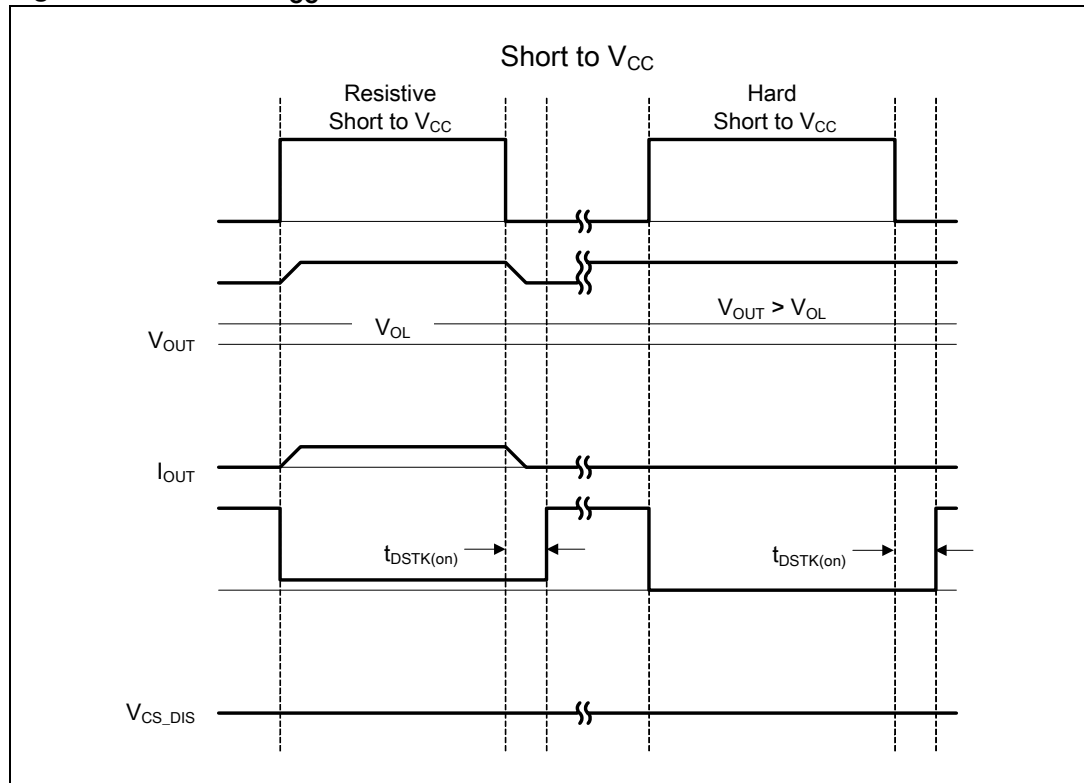
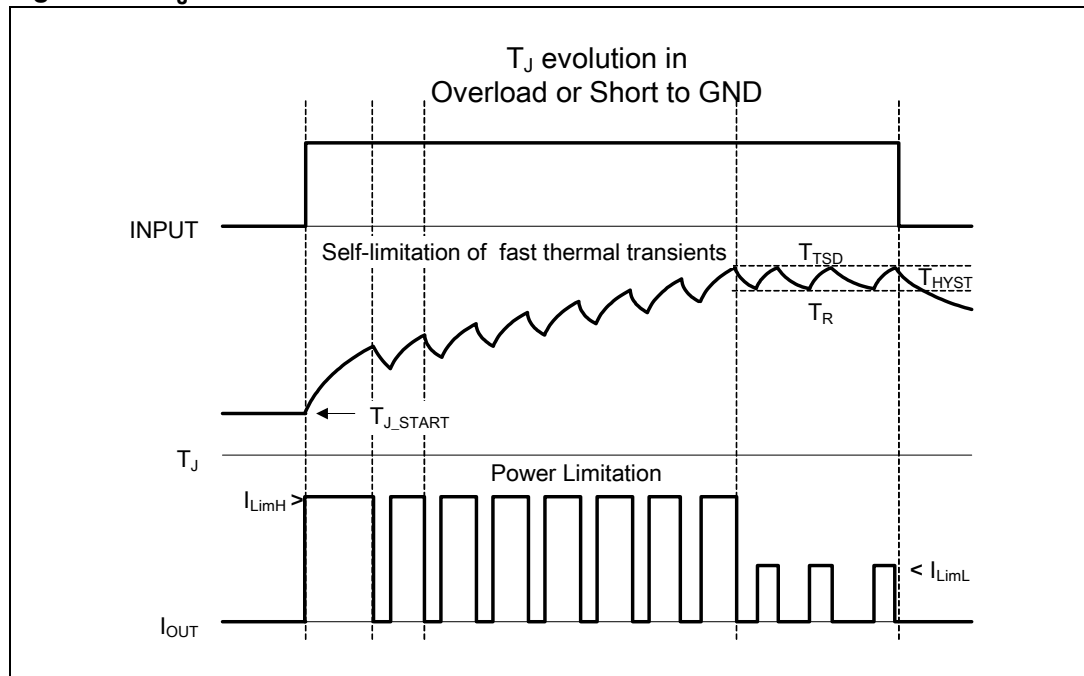


Figure 16.  $T_J$  evolution in Overload or Short to GND



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## 2.5 Electrical characteristics curves

Figure 17. Off state output current

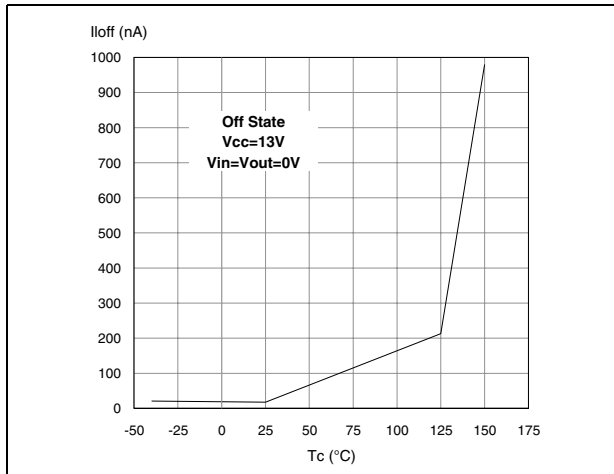


Figure 18. High level input current

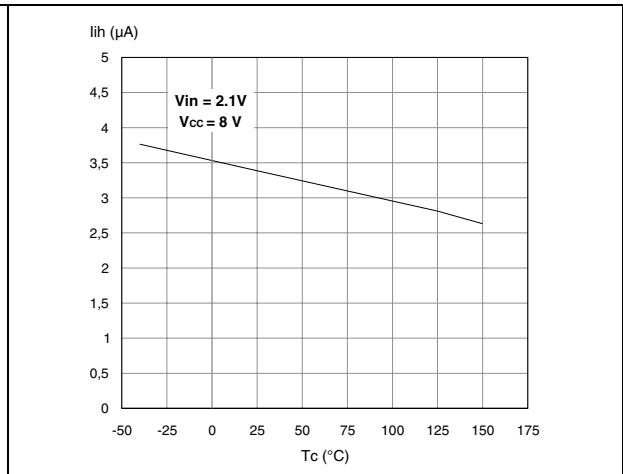


Figure 19. Input clamp voltage

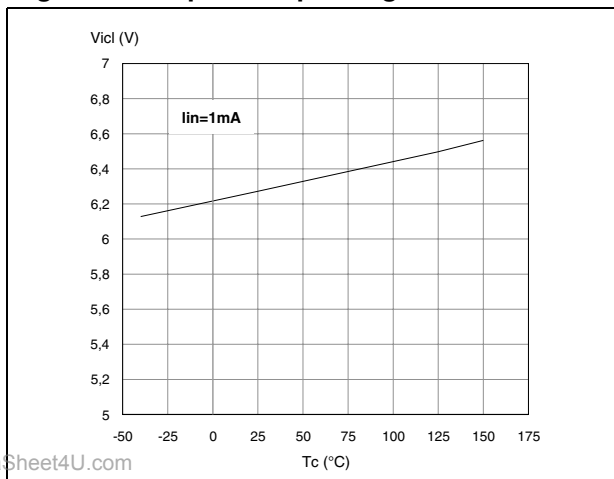


Figure 20. Input high level

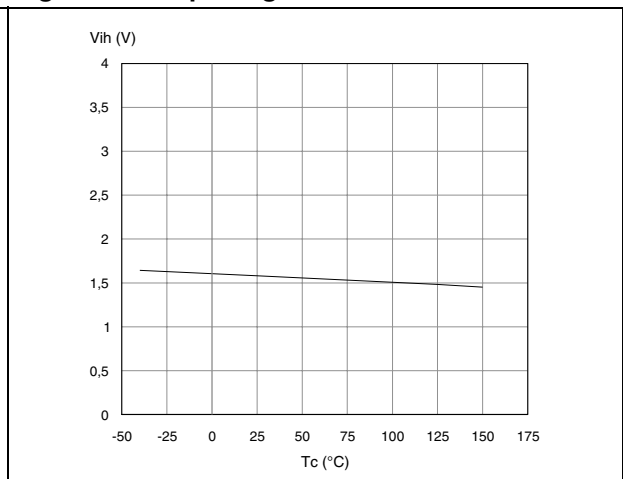


Figure 21. Input low level

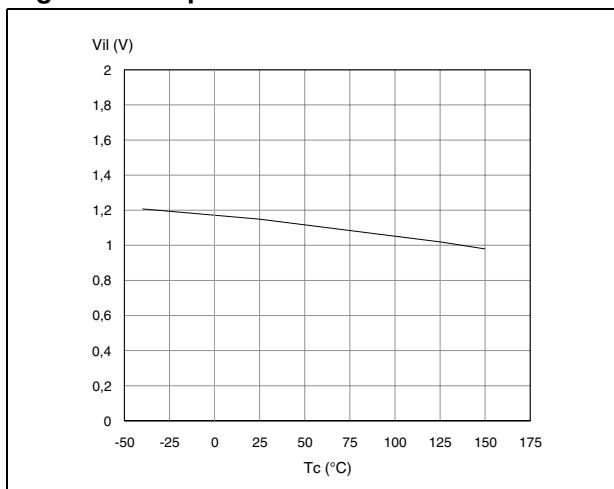
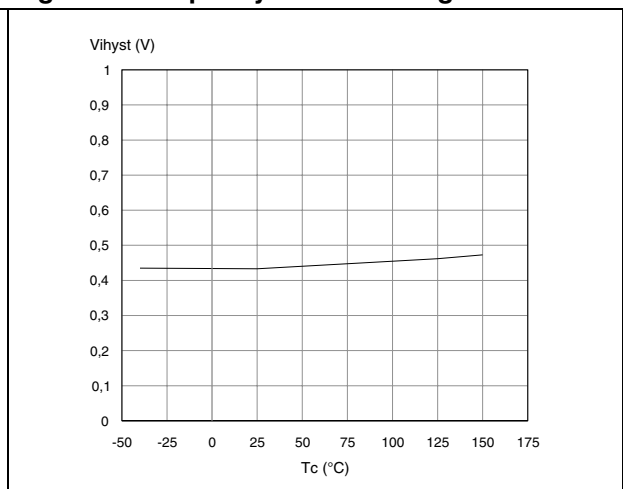


Figure 22. Input hysteresis voltage



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Electrical specification

VND5E025AK-E

Figure 23. On state resistance vs  $T_{case}$

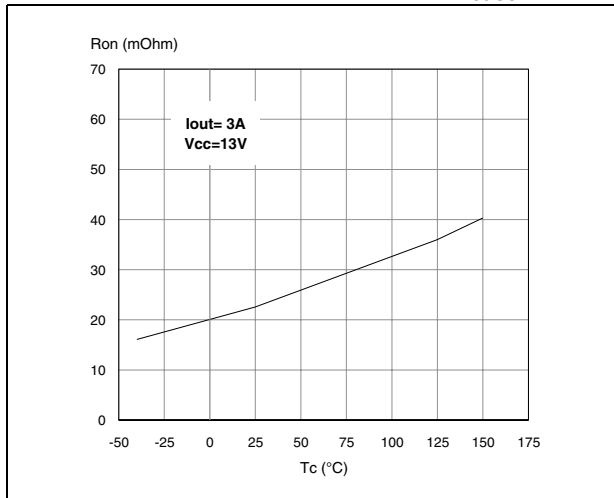


Figure 24. On state resistance vs  $V_{CC}$

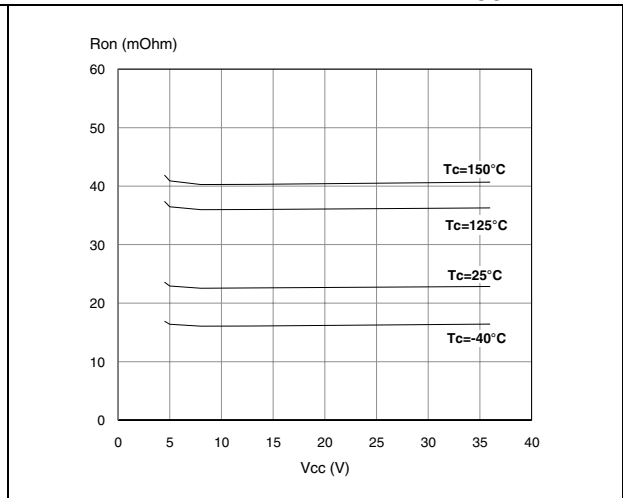


Figure 25. Undervoltage shutdown

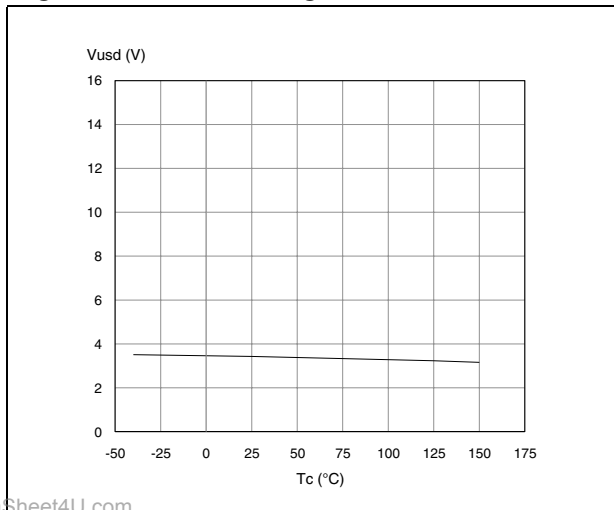
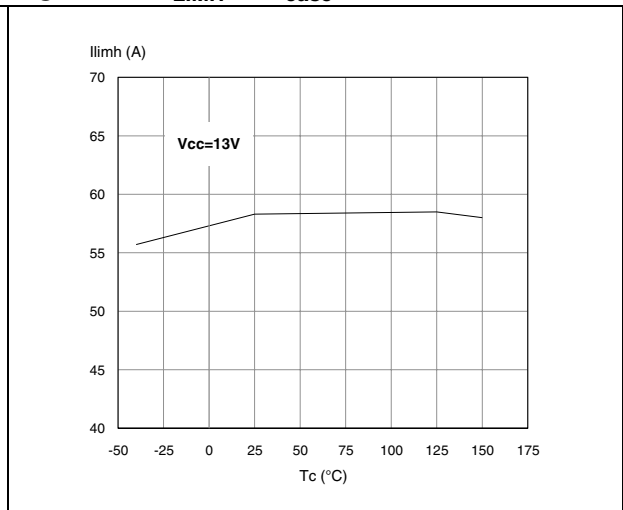


Figure 26.  $I_{LIMH}$  vs  $T_{case}$



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Figure 27. Turn-On voltage slope

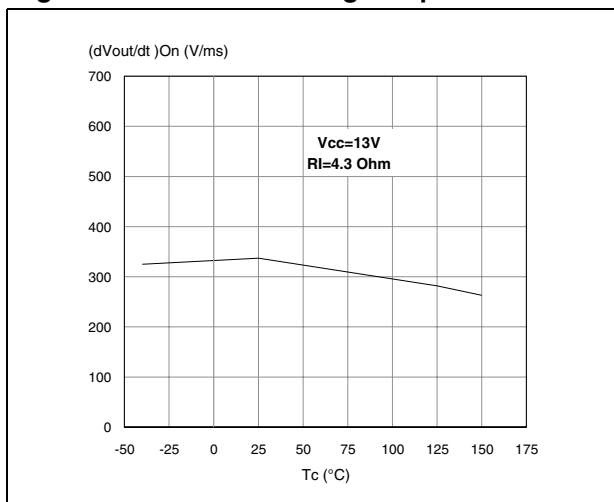


Figure 28. Turn-Off voltage slope

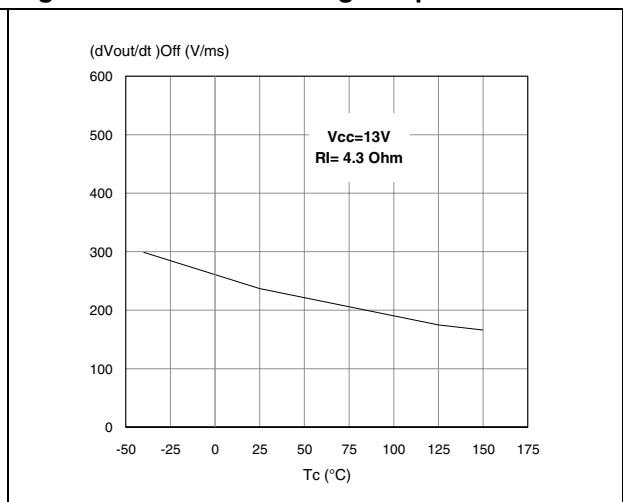


Figure 29. CS\_DIS high level voltage

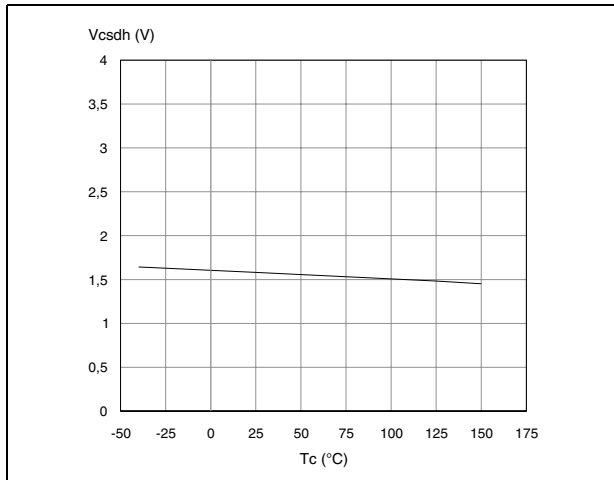


Figure 30. CS\_DIS low level voltage

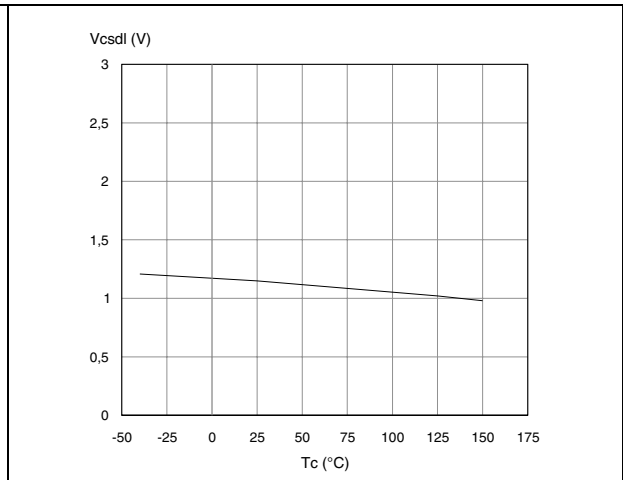
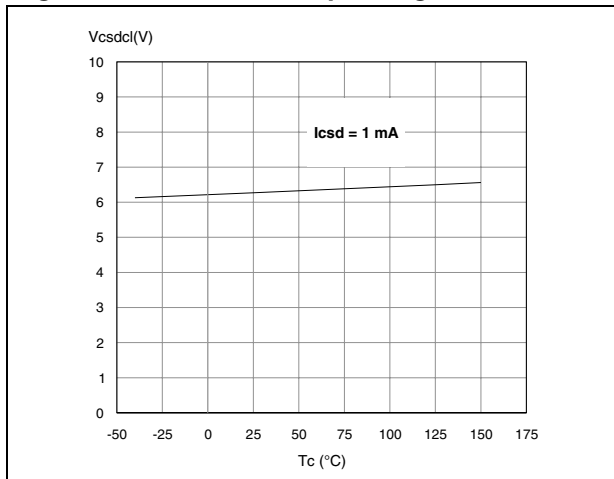
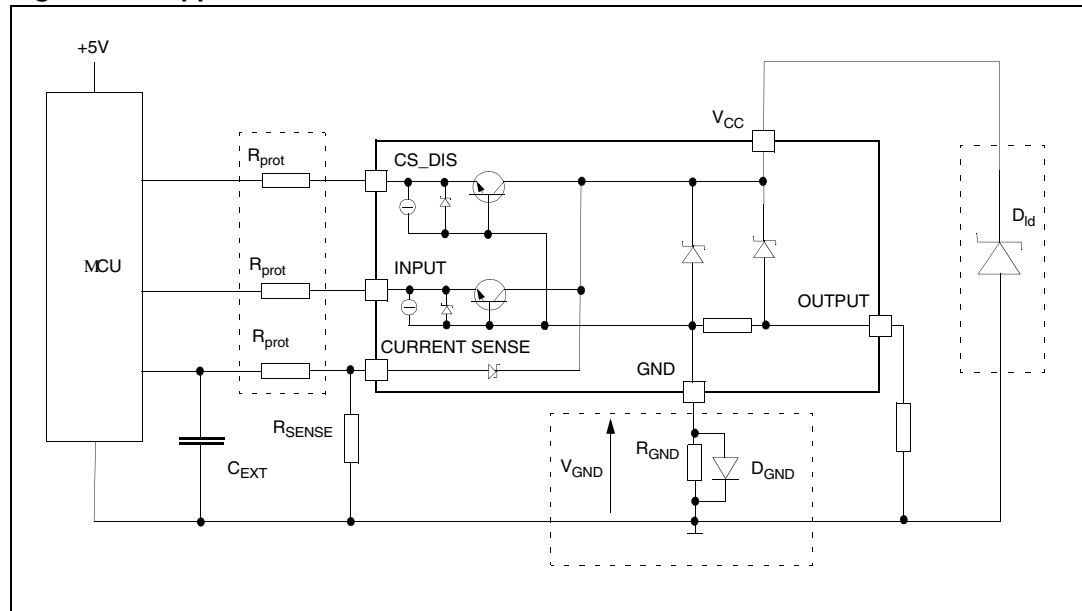


Figure 31. CS\_DIS clamp voltage



### 3 Application information

Figure 32. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

#### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

##### 3.1.1 Solution 1 : resistor in the ground line ( $R_{GND}$ only)

www.DataSheet4U.com This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

1.  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum On-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are On in the case of several high side drivers sharing the same  $R_{GND}$ .



If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

### 3.1.2 Solution 2 : diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND}=1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ( $\approx 600mV$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

## 3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values:  $R_{prot} = 10k\Omega$ ,  $C_{EXT} = 10nF$ .



### 3.4.1 Short to $V_{CC}$ and OFF state open load detection

#### Short to $V_{CC}$

A short circuit between  $V_{CC}$  and output is indicated by the relevant current sense pin set to  $V_{SENSEH}$  during the device off state. Small or no current is delivered by the current sense during the on state depending on the nature of the short circuit.

#### OFF state open load with external circuitry

Detection of an open load in off mode requires an external pull-up resistor  $R_{PU}$  connecting the output to a positive supply voltage  $V_{PU}$ .

It is preferable  $V_{PU}$  to be switched off during the module stand-by mode in order to avoid the overall stand-by current consumption to increase in normal conditions, i.e. when load is connected.

An external pull down resistor  $R_{PD}$  connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off state (see [Figure 33: Current sense and diagnostic](#)).

$R_{PD}$  must be selected in order to ensure  $V_{OUT} < V_{OLmin}$  unless pulled up by the external circuitry:

$$V_{OUT}|_{Pull-up\_OFF} = R_{PD} \cdot I_{L(off)2f} < V_{OLmin} = 2V$$

$R_{PD} \leq 22 \text{ K}\Omega$  is recommended.

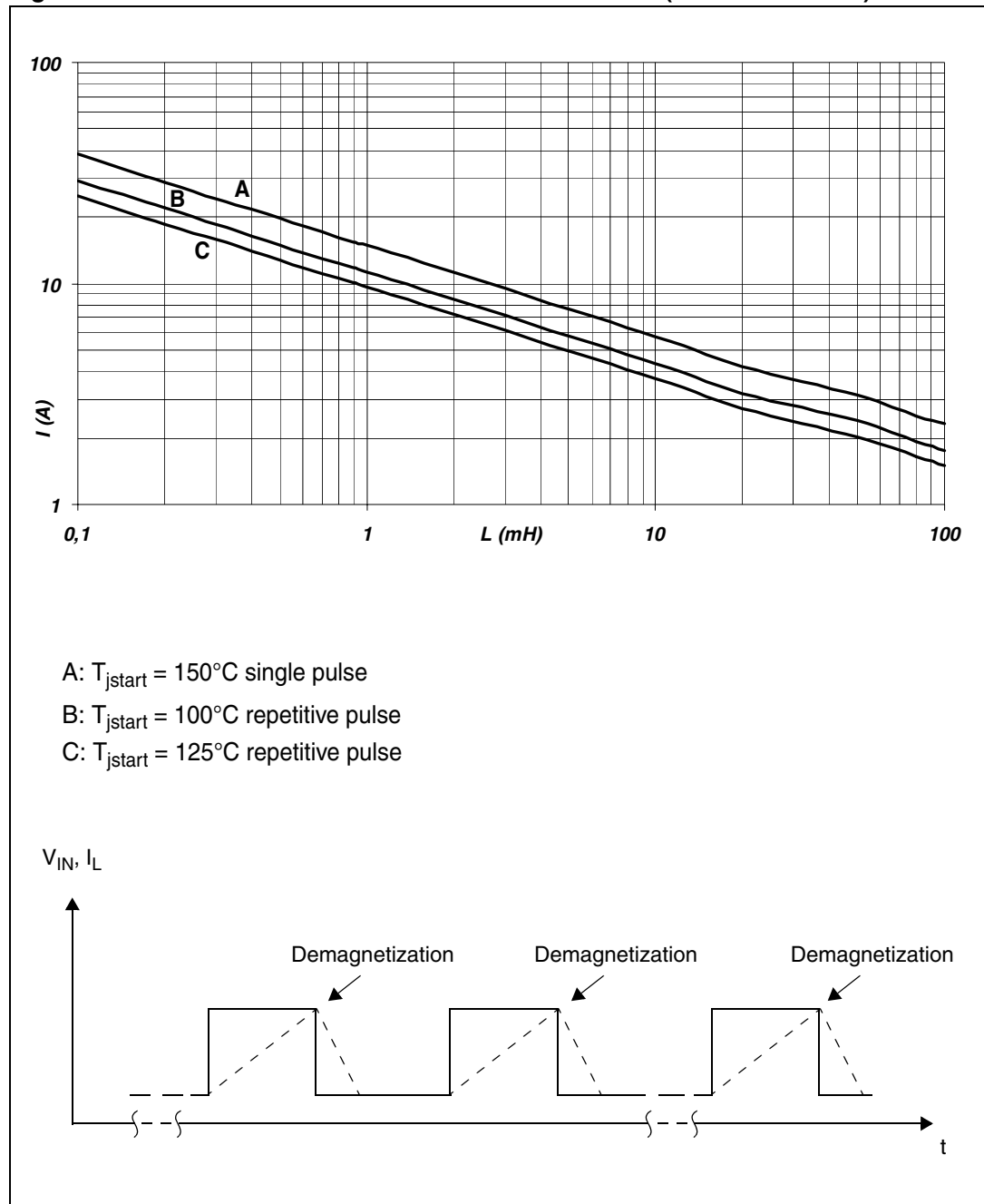
For proper open load detection in off state, the external pull-up resistor must be selected according to the following formula:

$$V_{OUT}|_{Pull-up\_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off)2r}}{R_{PU} + R_{PD}} > V_{OLmax} = 4V$$

For the values of  $V_{OLmin}$ ,  $V_{OLmax}$ ,  $I_{L(off)2r}$  and  $I_{L(off)2f}$  see [Table 10: Openload detection \(8V < VCC < 18V\)](#).

### 3.5 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 34. Maximum turn off current versus inductance (for each channel)



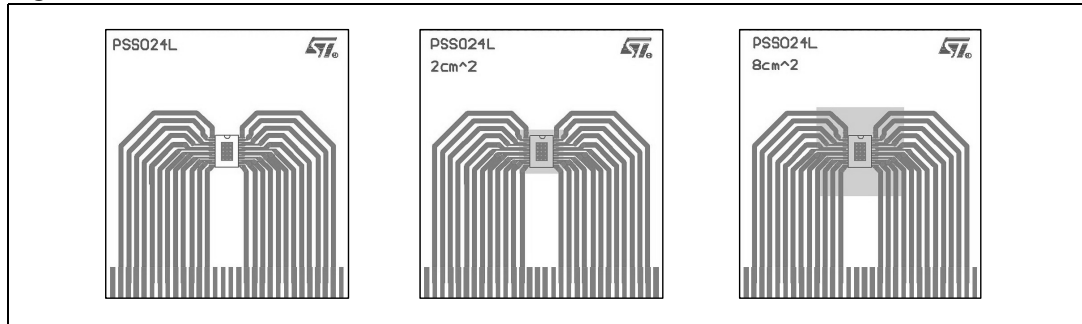
Note: Values are generated with  $R_L = 0 \Omega$

In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and thermal data

### 4.1 PowerSSO-24 thermal data

Figure 35. PowerSSO-24 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area = 77mm x 86mm, PCB thickness = 1.6mm, Cu thickness = 70 $\mu$ m (front and back side), Copper areas: from minimum pad layout to 8cm<sup>2</sup>).

Figure 36.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel ON)

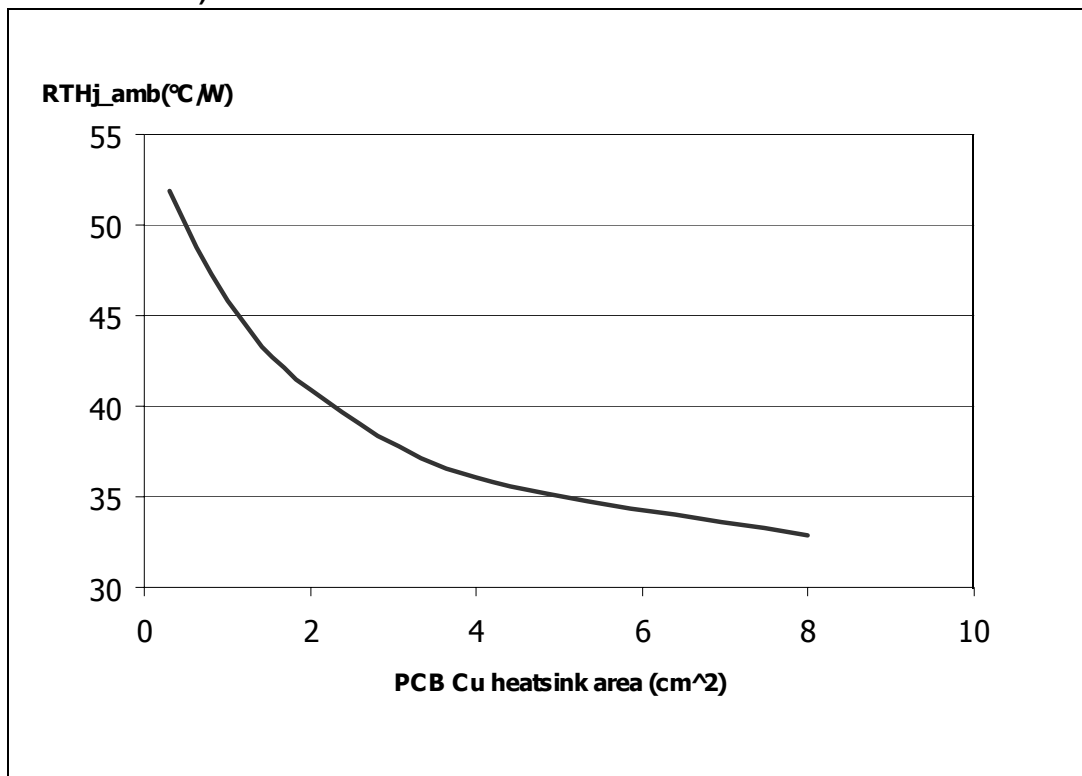
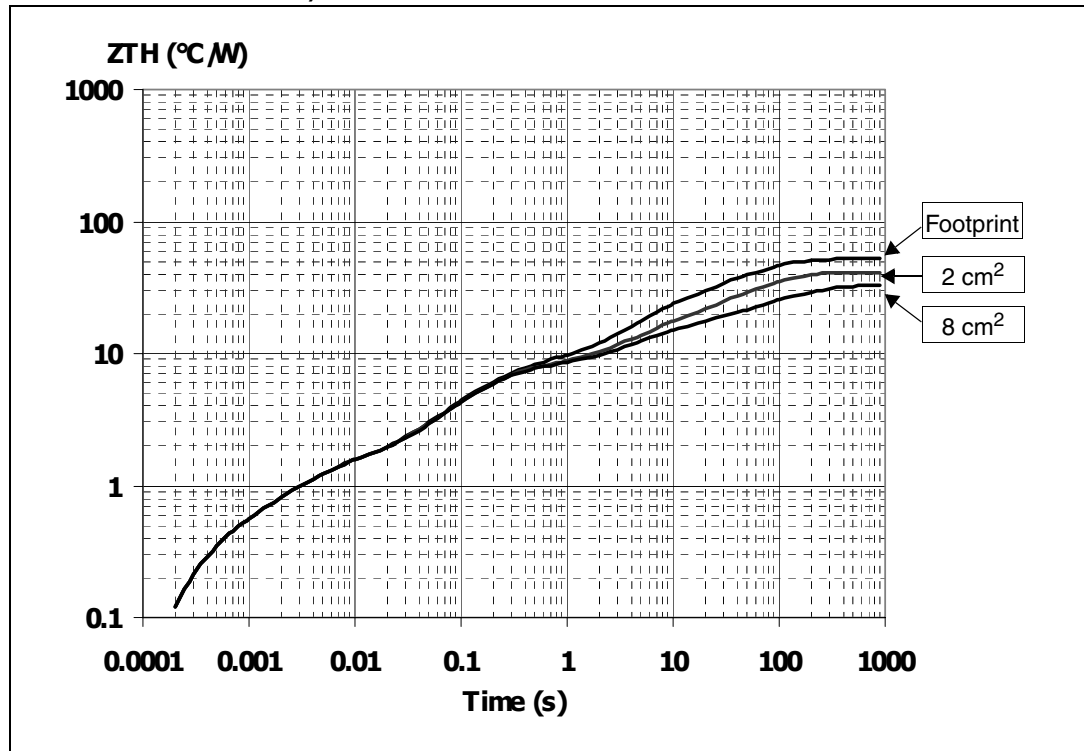


Figure 37. PowerSSO-24 thermal impedance junction to ambient single pulse (one channel ON)

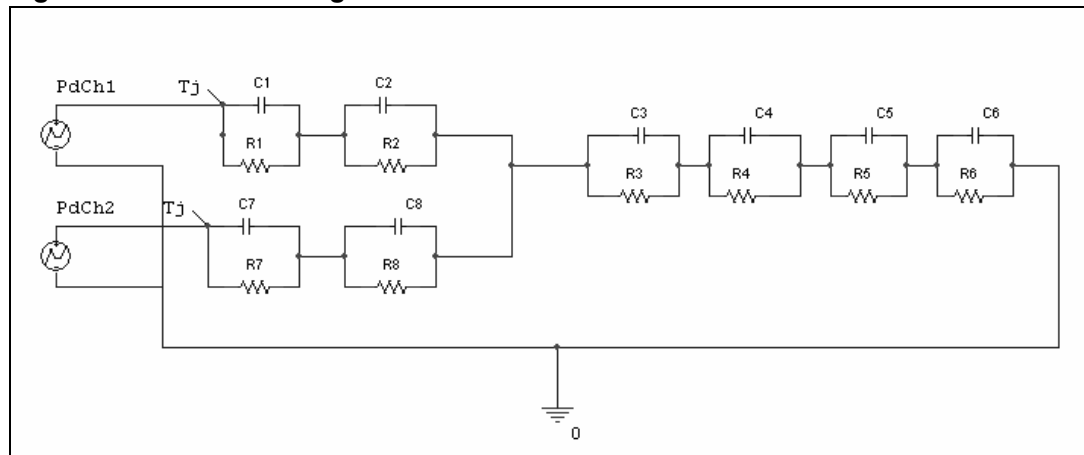


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-24 (a)



- a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 13. Thermal parameters

Area/Island (cm <sup>2</sup> )	Footprint	2	8
R1 (°C/W)	0.28		
R2 (°C/W)	0.9		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
R7 (°C/W)	0.28		
R8 (°C/W)	0.9		
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.003		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17
C7 (W.s/°C)	0.001		
C8 (W.s/°C)	0.003		

## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. ECOPACK<sup>®</sup> packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at [www.st.com](http://www.st.com).

### 5.2 Package mechanical data

Figure 39. PowerSSO-24 package dimensions

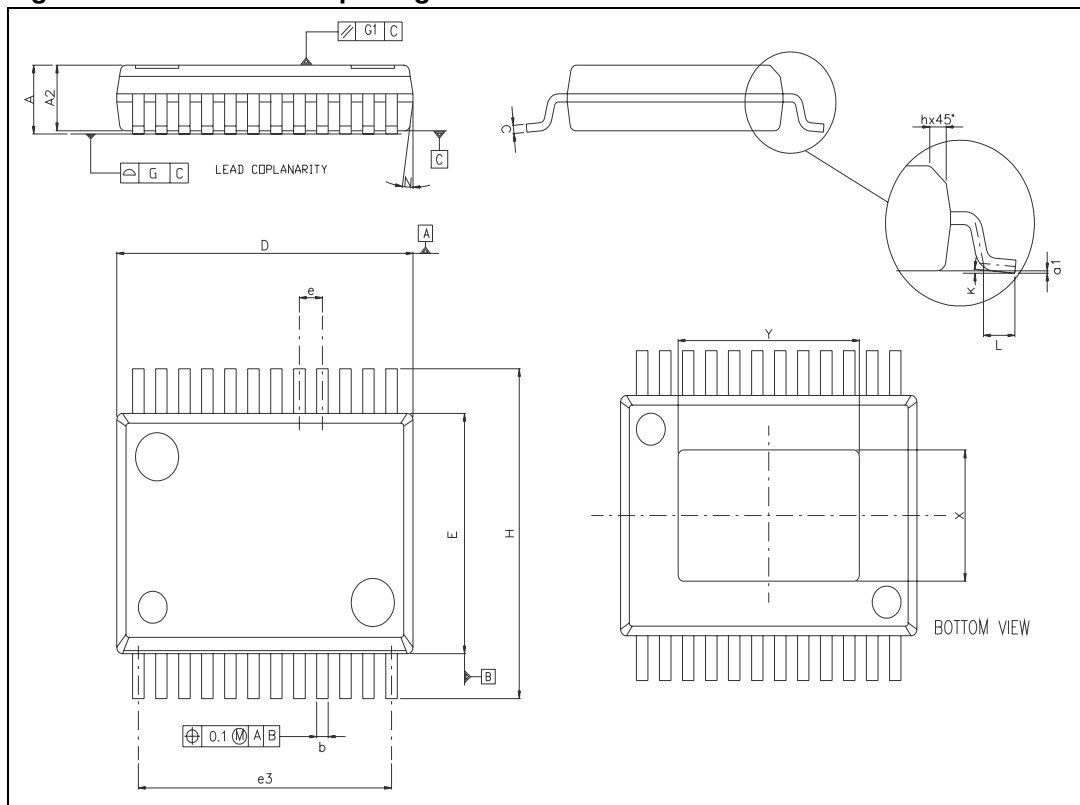




Table 14. PowerSSO-24 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k		5°	
L	0.55		0.85
N			10°
X	4.1		4.7
Y	6.5		7.1

### 5.3 Packing information

Figure 40. PowerSSO-24 tube shipment (no suffix)

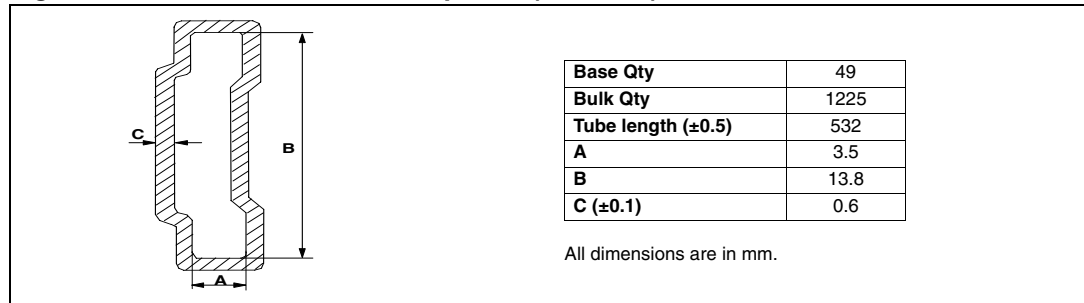
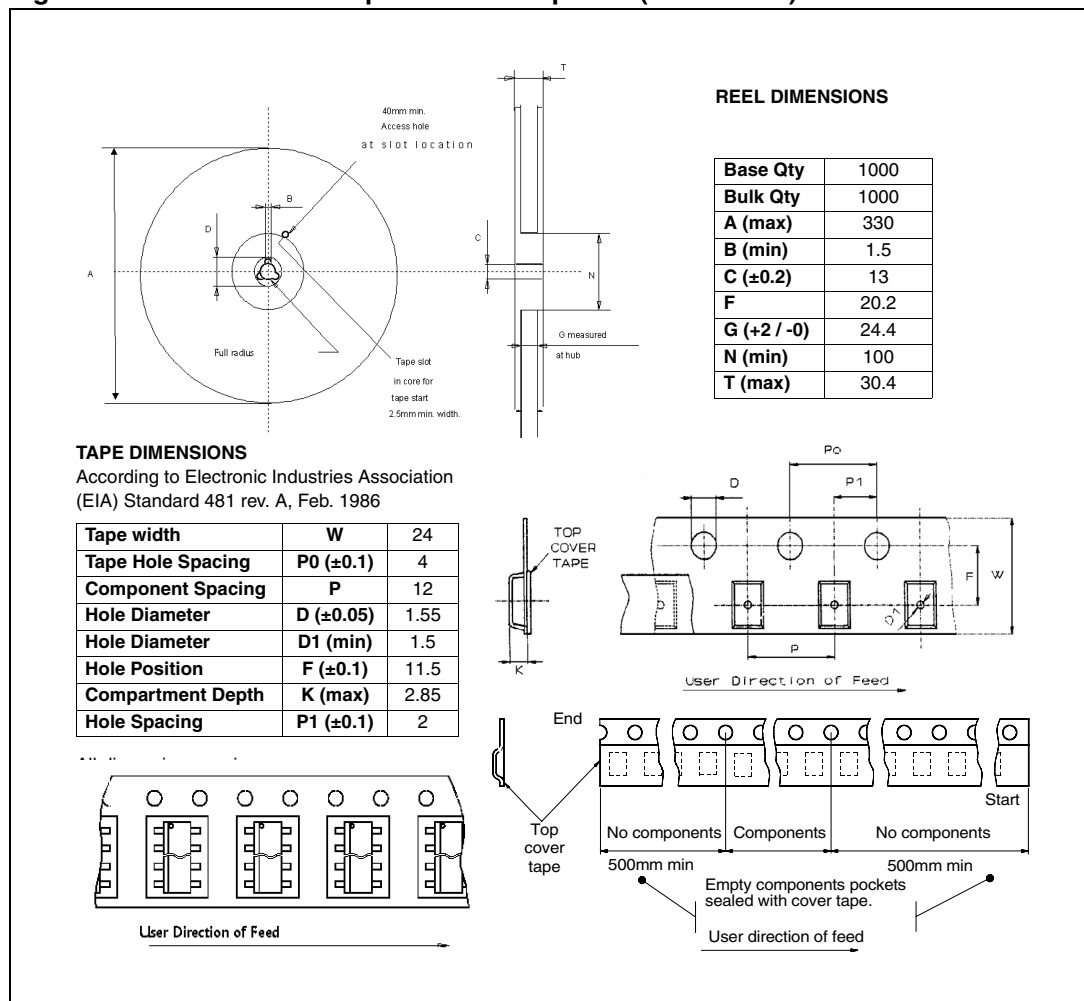


Figure 41. PowerSSO-24 tape and reel shipment (suffix "TR")



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## 6 Order codes

Table 15. Device summary

Package	Order codes	
	Part number (tube)	Part number (tape & reel)
PowerSSO-24	VND5E025AK-E	VND5E025AKTR-E

## 7 Revision history

**Table 16. Document revision history**

Date	Revision	Changes
01-Apr-2008	1	Initial release

**VND5E025AK-E**

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