VNH7100AS-E

Automotive fully integrated H-bridge motor driver

Datasheet - preliminary data

SO-16N

Features

Type	$R_{DS(on)}$	I_{out}	V_{CCmax}
VNH7100AS-E	100 mΩ typ (per leg)	12 A	41 V

- Automotive qualified
- Output current: 15 A
- 3 V CMOS-compatible inputs
- Undervoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- Protection against loss of ground and loss of V_{CC}
- PWM operation up to 20 KHz
- Multisense diagnostic functions
  - Analog motor current feedback
  - Output short to ground detection
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
- Output protected against short to ground and short to V_{CC}
- Standby Mode
- Half Bridge Operation
- Package: ECOPACK®

Description

The VNH7100AS-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver and two low-side switches.

Both switches are designed using STMicroelectronics' well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The three dies are assembled in SO-16N package on electrically isolated leadframes.

Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals IN_A and IN_B can directly interface to the microcontroller to select the motor direction and the brake condition. A SEL0 pin is available to address to the microcontroller the information available on the Multisense. The Multisense pin allows to monitor the motor current by delivering a current proportional to the motor current value. The normal operating condition is explained in the truth table.

The PWM, up to 20 KHz, allows to control the speed of the motor in all possible conditions. In all cases, a low level state on the PWM pin turns off both the LS_A and LS_B switches.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-16N	VNH7100AS-E	VNH7100ASTR-E

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Block diagram and pin description

Figure 1. Block diagram

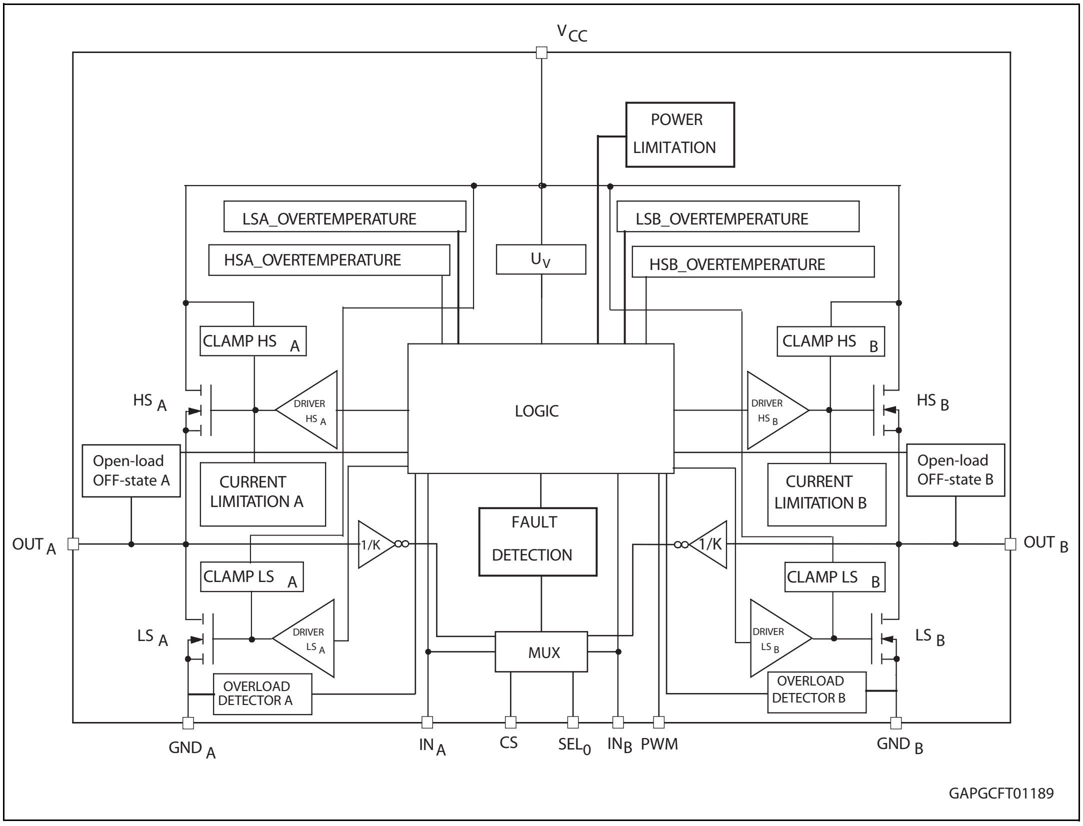

Table 2. Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table.
Undervoltage	Shuts down the device for battery voltage lower than 4 V.
High-side and low-side clamp voltage	Protect the high-side and the low-side switches from the high voltage on the battery line.
High-side and low-side driver	Drive the gate of the concerned switch to allow a proper R_{on} for the leg of the bridge.
Current limitation	Limits the motor current in case of short circuit.
High-side and low-side overtemperature protection	In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die.
Low-side overload detector	Detects when low side current exceeds shutdown current and latches off the concerned Low side.

Table 2. Block description (continued)

Name	Description
Fault detection	Signalizes the abnormal behavior of the switch through Multisense pin.
Power limitation	Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition.

Figure 2. Configuration diagram (top view)

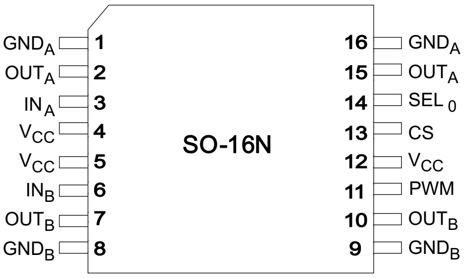

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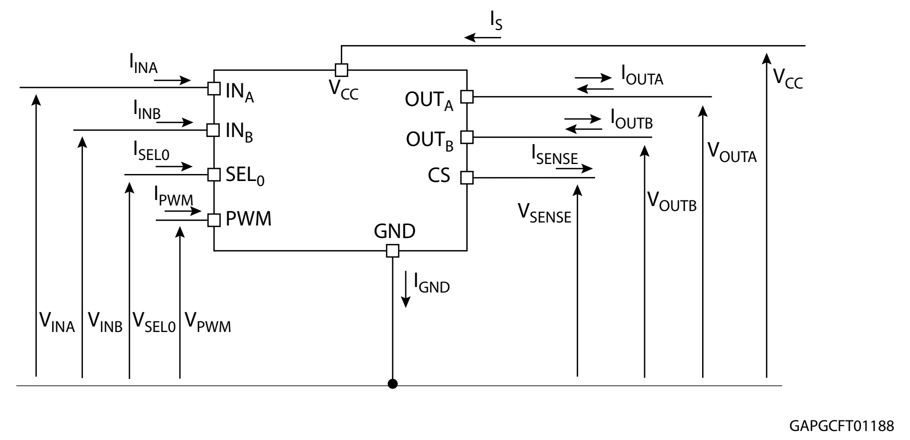
Table 3. Pin definitions and functions

Pin N°	Symbol	Function
1, 16	GND_A	Source of low-side switch A
2, 15	OUT_A	Source of high-side switch A / drain of low-side switch A
3	IN_A	Clockwise input
4, 5, 12	V_{CC}	Power supply voltage
6	IN_B	Counter clockwise input
7, 10	OUT_B	Source of high-side switch B / drain of low-side switch B
8, 9	GND_B	Source of low-side switch B
11	PWM	Voltage controlled input pin with hysteresis, CMOS compatible. Gates of low-side FETS get modulated by the PWM signal during their on phase allowing speed control of the motor
13	CS	Multiplexed analog sense output pin; it delivers a current proportional to the motor current.
14	SEL_0	Active high compatible with 3 V and 5 V CMOS outputs pin; n combination with IN_A, IN_B, it addresses the Multisense information delivered to the micro.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	38	V
$-V_{CC}$	Reverse DC Supply Voltage	0.3	V
I_{max}	Maximum output current (continuous)	Internally limited	A
I_R	Reverse output current (continuous)	TBD	A
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; RL = 4 Ω)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
I_{IN}	Input current (IN_A and IN_B pins)	-1 to 10	mA
I_{SEL0}	SEL_0 DC input current	-1 to 10	mA
I_{PWM}	PWM input current	-1 to 10	mA
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{SENSE}	CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	CS pin DC output current in reverse ($V_{CC} < 0$ V)	-20	

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human body model: R = 1.5 kΩ C = 100 pF) – IN_A,IN_B, PWM – SEL_0 – CS – V_{CC} – Output	 2 2 2 4 4	kV
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_c	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}pin}$	Thermal resistance junction-case (per leg) (JEDEC JESD 51-5)(1)	TBD	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(2)	TBD	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)	TBD	°C/W

1. Device mounted on four-layers 2s2p PCB.
2. Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace.

2.3 Electrical characteristics

Values specified in this section are for V_{CC} = 7 V up to 28 V; -40°C < T_j < 150°C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4		28	V
I_S	Supply current	Off-state (standby) $IN_A = IN_B = 0$; $SEL_0 = 0$; PWM = 0; T_j = 25 °C; V_{CC} = 13 V;			1	µA
		Off-state (standby) $IN_A = IN_B = 0$; $SEL_0 = 0$; PWM = 0; V_{CC} = 13 V; T_j = 85°C			1	µA
		Off-state (standby) $IN_A = IN_B = 0$; $SEL_0 = 0$; PWM = 0; V_{CC} = 13 V; T_j = 125 °C			3	µA
		Off-state (no standby) $IN_A = IN_B = 0$; SEL_0 = 5 V; PWM= 0		2	4	mA
		On-state: IN_A or IN_B = 5 V; PWM = 0 or PWM = 5; SEL_0 = X		3	6	mA
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; $IN_A = IN_B$ = PMW = 0 V; V_{SEL0} from 5 V to 0 V	0.2	1	1.8	ms
R_{ONHS}	Static high-side resistance	I_{OUT} = 2.5 A; T_j = 25°C		60		mΩ
		I_{OUT} = 2.5 A; T_j = -40 to 150°C			120	mΩ
R_{ONLS}	Static low-side resistance	I_{OUT} = 2.5 A; T_j = 25°C		40		mΩ
		I_{OUT} = 2.5 A; T_j = -40°C to 150°C			80	mΩ
V_f	High-side free-wheeling diode forward voltage	I_{OUT} = -2.5 A; T_j = 150°C		0.7	0.9	V
$I_{L(off)}$	Off-state output current of one leg	$IN_A = IN_B = 0$; PWM = 0; V_{CC} = 13 V; T_j = 25 °C	0		0.5	µA
		$IN_A = IN_B = 0$; PWM = 0; V_{CC} = 13 V; T_j = 125 °C	0		3	µA
$I_{L(off\_h)}$	Off-state output current of one leg with other HSD on	$IN_A = 0$; IN_B = 5 V; PWM = 0; V_{CC} = 13 V		20	60	µA

Table 7. Logic inputs (IN_A, IN_B, PWM) (V_{CC} = 7 V up to 28 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
V_{IH}	Input high level voltage		2.1			V
V_{IHYST}	Input hysteresis voltage		0.2			V

Table 7. Logic inputs (IN_A, IN_B, PWM) (V_{CC} = 7 V up to 28 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		V
I_{INL}	Input current	V_{IN} = 0.9 V	1			µA
I_{INH}	Input current	V_{IN} = 2.1 V			10	µA
SEL_0 (V_{CC} = 7 V up to 18 V; -40°C < T_j < 150°C)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{SEL} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{SEL} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{SEL} = 1 mA	5.3		7.5	V
		I_{SEL} = -1 mA		-0.7		V
PWM (V_{CC}= 7 V up to 28 V; -40°C < T_j < 150°C)						
V_{PWM}	Input low level voltage				0.9	V
I_{PWM}	Low level input current	V_{PWM} = 0.9 V	1			µA
V_{PWM}	Input high level voltage		2.1			V
I_{PWMH}	High level input current	V_{PWM} = 2.1 V			10	µA
$V_{PWM(hyst)}$	Input hysteresis voltage		0.2			V
V_{PMWCL}	Input clamp voltage	I_{PWM} = 1 mA	5.3		7.2	V
		I_{PWM} = -1 mA		-0.7		V

Table 8. Switching (V_{CC} = 13 V; R_{LOAD} = 5.2 Ω)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	PWM frequency		0		20	kHz
$t_{d(on)}$	Turn-on delay time	Input rise time < 1µs (see *Figure 6*)		17		µs
$t_{d(off)}$	Turn-off delay time	Input rise time < 1µs (see *Figure 6*)		10		µs
t_r	Rise time	See *Figure 5*		1	2	µs
t_f	Fall time	See *Figure 5*		1	2	µs
t_{cross}	Low-side turn-on delay time	Input rise time < 1 µs (see *Figure 7*)	40	140	240	µs

Table 9. Protections and diagnostics (V_{CC} = 7 V up to 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{USD}	Undervoltage shutdown				4	V
$V_{USDreset}$	Undervoltage shutdown reset				5	V
$V_{USDHyst}$	Undervolatge shutdown Hysteresis			0.3		V
I_{LIM_H}	High-side current limitation		12	18	24	A
I_{SD_LS}	Shutdown LS current		15	22	30	A
t_{SD_LS}	Time to shutdown for the low-side	V_{INA} = V_{INB} = 0 V; PWM = 5 V (see *Figure 8*)		5		µs
V_{CL_HSD}	High-side clamp voltage (V_{CC} to OUT_A = 0 or OUT_B = 0)	I_{OUT} = 2.5 A; L = 6 mH; T_j = -40 °C	38			V
		I_{OUT} = 2.5 A; L = 6 mH; T_j = 25 °C to 150 °C	41	46		V
V_{CL_LSD}	Low-side clamp voltage (OUT_A = V_{CC} or OUT_B = V_{CC} to GND)	I_{OUT} = 2.5 A; L = 6 mH	38	46		V
T_{TSD_HS}	High-side thermal shutdown temperature	IN_x = 2.1 V	150	175	200	°C
T_{TR_HS}	High-side thermal reset temperature		135			°C
T_{HYST_HS}	High-side thermal hysteresis (T_{SD_HS} - T_{R_HS})			7		°C
T_{TSD_LS}	Low-side thermal shutdown temperature	IN_x = 0 V	150	175	200	°C
V_{CL}	Total clamp voltage (V_{CC} to GND)	I_{OUT} = 2.5 A; L = 6 mH	38	46	52	V
V_{OL}	OFF-state open-load voltage detection threshold	IN_A = IN_B = 0; PWM = 0; V_{SEL0} = 5 V for CHA; V_{SEL0} = 0 V and within t_{D_STBY} for CHB	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	IN_A = IN_B = 0; V_{OUTx} = V_{OL}; PWM = 0 V; V_{SEL0} = 5 V for CHA; V_{SEL0} = 0 V and within t_{D_STBY} for CHB	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 4*)	IN_A = 5 V to 0 V; IN_B = 0 V; V_{SEL0} = 5 V; I_{OUT} = 0 A; V_{OUTA} = 4 V; PWM = 0 V	40	140	240	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	IN_A = IN_B = 0 V; PWM = 0 V; V_{OUTx} = 0 V to 4 V; V_{SEL0} = 5 V for CHA; V_{SEL0} = 0 V and within t_{D_STBY} for CHB		5	30	µs

Table 9. Protections and diagnostics (V_{CC} = 7 V up to 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{Latch\_RST\_HD}$(1)	Input reset time for high-side fault unlatch	V_{INx} = 5 V to 0 V; HSDx faulting	3	10	20	µs
$t_{Latch\_RST\_LS}$(1)	Input reset time for low-side fault unlatch	V_{INx} = 0 V to 5 V; LSDx faulting	3	10	20	µs

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 10. CS (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = -1 mA		TBD		V
		V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	TBD		TBD	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	TBD		TBD	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 2.5 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	TBD		TBD	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 5 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	TBD		TBD	%
dK_0/K_0(1)	Analog sense current drift	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	TBD		TBD	%
dK_1/K_1(1)	Analog sense current drift	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	TBD		TBD	%
dK_2/K_2(1)	Analog sense current drift	I_{OUT} = 2.5 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	TBD		TBD	%
dK_3/K_3(1)	Analog sense current drift	I_{OUT} = 5 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	-4		4	%
V_{SENSE_SAT}	Max analog sense output voltage	V_{CC} = 7 V; R_{SENSE} = 10 kΩ; V_{SEL0} = 5 V; I_{OUTA} = 5 A; V_{INA} = 5 V; PWM = 0; T_j = 150 °C	5			V
I_{SENSE0}	Multisense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; IN_x = 0 V; SEL_0 = 0; T_j = -40°C to 150°C (Standby)	0		0.5	µA
		I_{OUT} = 0 A; V_{SENSE} = 0 V; IN_x = 0 V; SEL_0 = 5 V; Tj = -40°C to 150°C (No Standby)	0		0.5	µA
		IN_x = 5 V; PWM = 5 V: T_j = -40°C to 150°C; I_{OUT} = 0 A	0		5	µA
V_{SENSEH}	Multisense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ – E.g: OUT_A in open-load IN_A = 0 V; I_{OUTA} = 0 A; V_{OUTA} = 4 V; V_{SEL0} = 5 V	5		7	V

Table 10. CS (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OUT_MSD}(2)	Output Voltage for MultiSense shutdown	V_{INA} = 5 V; V_{INB} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; R_{SENSE} = 2.7 kΩ I_{OUT} = 2.5 A		5		V
I_{SENSE_SAT}	MultiSense saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{INA} = 5 V; V_{INB} = 0 V; V_{SEL0} = 5 V; T_j = 150 °C	4			mA
I_{OUT_SAT}(2)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{INA} = 5 V; V_{INB} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; T_j = 150°C	5			A
I_{SENSEH}	Multisense output voltage in fault condition	V_{CC} = 13 V; V_{SENSE} = V_{SENSEH}	7	20	30	mA

1. Analog sense current drift is deviation of factor K for a given device over (-40 °C to 150 °C and 9 V < V_{CC} < 18 V) with respect to its value measured at T_j = 25 °C, V_{CC} = 13 V.
2. Parameter guaranteed by design and characterization; not subject to production test.

Figure 4. T_{DSTKON}

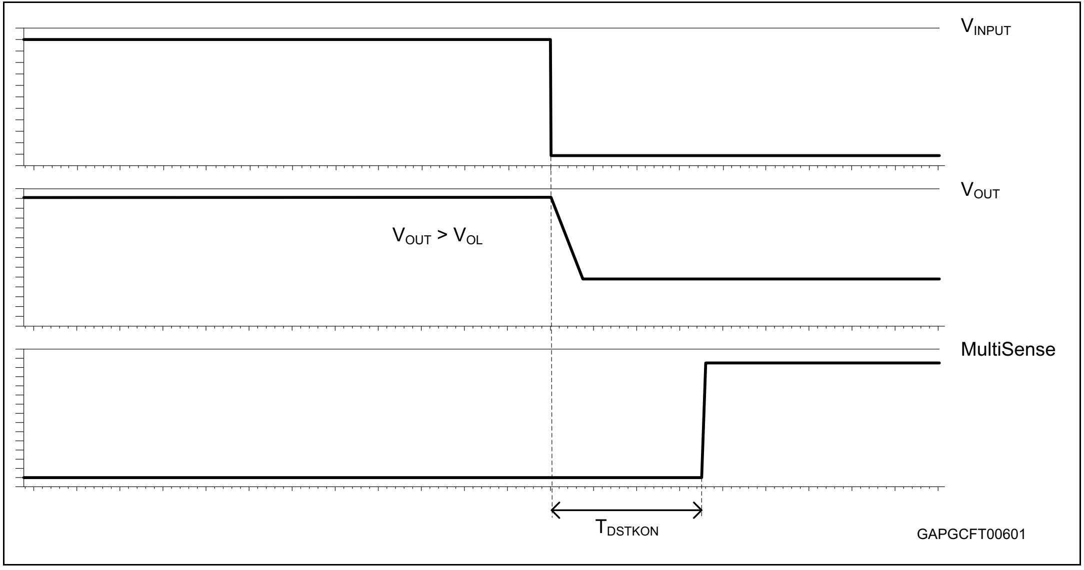


Figure 5. Definition of the low-side switching times

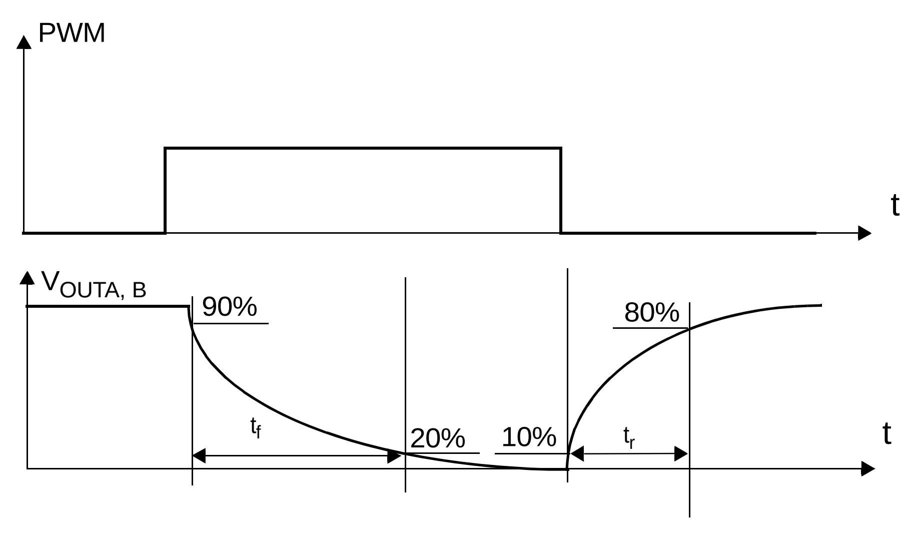


Figure 6. Definition of the high-side switching times

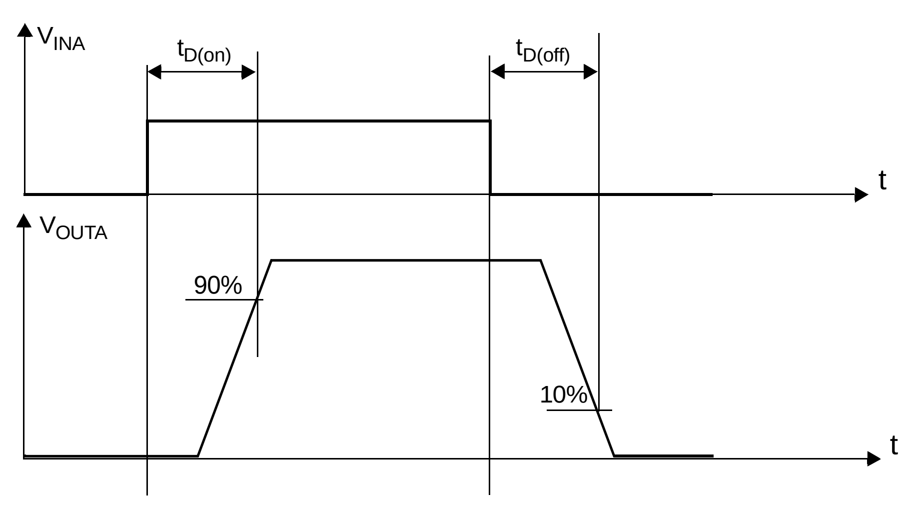


Figure 7. Low-side turn-on delay time

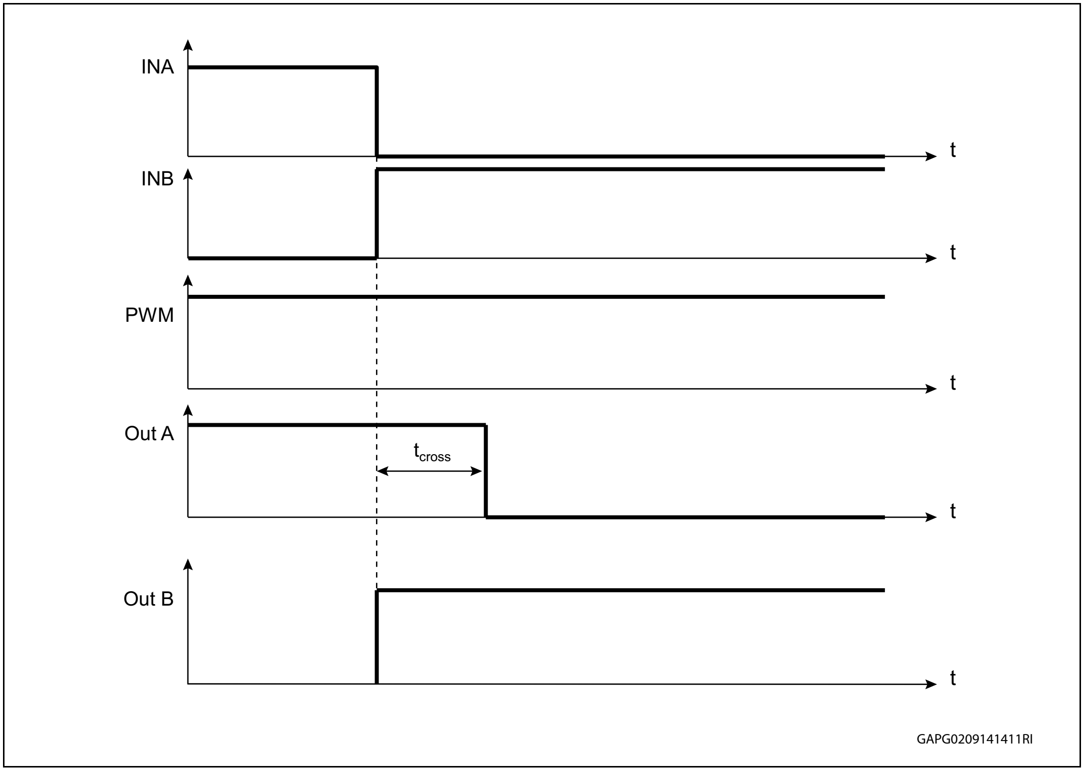


Figure 8. Time to shutdown for the low-side driver

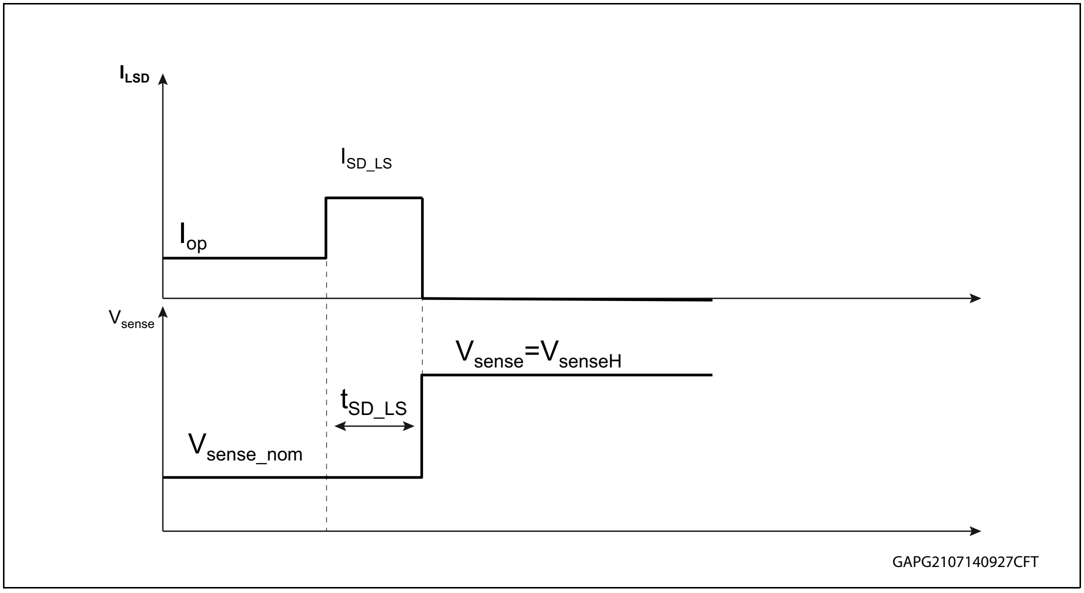


Table 11. Operative condition - truth table

Pin status					HSDs and LDSs Statu			
IN_A	IN_B	Sel_0	PWM	CS	HSDA	LSDA	HSDB	LSDB
1	1	1	x	Current Monitoring HSDA	On	Off	On	Off
		0		Current Monitoring HSDB				
1	0	1	1	Current Monitoring HSDA	On	Off	Off	On
			0		On	Off	Off	Off
1	0	0	1	Hi-Z	On	Off	Off	On
			0		On	Off	Off	Off
0	1	1	1	Hi-Z	Off	On	On	Off
			0		Off	Off	On	Off
0	1	0	1	Current Monitoring HSDB	Off	On	On	Off
			0		Off	Off	On	Off
0	0	1	1	Hi-Z	Off	On	Off	On
		0						
0	0	1	0	x(1)	Off	Off	Off	Off
		0(2)			Off	Off	Off	Off

1. Refer to *Table 13: Off-state -truth table*
2. For IN_A =IN_B=SEL_0 = PWM = 0, the device enters in standby after t_{D_STBY}

Table 12. On-state fault conditions- truth table Fault on leg A (preliminary)

IN_A	IN_B	SEL_0	PWM	Out_A	Out_B	CS	Fault description
On state diagnostic							
1	0	1	X	L	L	V_{SENSEH}	Out A short to GND
1	0	0	1	H	H	V_{SENSEH}	Out B short to V_{CC}
0	1	1	1	H	H	V_{SENSEH}	Out A short to V_{CC}
0	1	0	X	X	L	V_{SENSEH}	Out B short to GND

Table 13. Off-state -truth table

IN$_A$	IN$_B$	SEL$_0$	PWM	Out$_A$	Out$_B$	CS	Description
Off-state diagnostic							
0	0	1	0	$V_{outA}>V_{OL}$	x	V_{SENSEH}	Case 1. Out$_A$ shorted to V_{CC} if no pull-up is applied Case 2. No open-load in full bridge configuration with an external pull-up on Out$_B$ Case 3. open-load in half bridge configuration with an external pull-up on Out$_A$(motor connected between Out$_A$ and Ground)
				$V_{outA}<V_{OL}$	x	Hi-Z	Case 1. Open-load in full Bridge configuration with an external pull-up on Out$_B$ Case 2. No open-load in half Bridge configuration with external pull-up on Out$_A$ (motor connected between Out$_A$ and Ground)
		0[1]		X	$V_{outB}>V_{OL}$	V_{SENSEH}	Case 1. Out$_B$ shorted to V_{CC} if no pull-up is applied Case 2. No open-load in full bridge configuration with external pull-up on Out$_A$ Case 3. Open-load in half bridge configuration with external pull-up on Out$_B$ (motor connected between Out$_B$ and Ground)
				X	$V_{outB}<V_{OL}$	Hi-Z	Case1. Open-load in full Bridge configuration with an external pull-up on Out$_A$ Case 2. No open-load in half Bridge configuration with external pull-up on Out$_B$ (motor connected between Out$_B$ and Ground)

1. The device enters standby mode after t_{D_STBY}

3 Application information

3.1 GND protection network against reverse battery

3.1.1 Diode (D_{GND}) in the ground line

A resistor (typ. R_{GND} = 4.7 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

3.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 14*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 14. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S[1]		min	max	
1	III	-112 V	500 pulses	0,5 s		2ms, 10 Ω
2a	III	+55 V	500 pulses	0,2 s	5 s	50µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1µs, 50 Ω
4[2]	IV	-7 V	1 pulse			100ms, 0.0 1Ω
Load dump according to ISO 16750-2:2010						
Test B[3]		40 V	5 pulse	1 min		400 ms, 2 Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.
2. Test pulse from ISO 7637-2:2004(E).
3. With 40 V external suppressor referred to ground (-40°C < T_j < 150°C).

4 Package and packing information

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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4.2 SO-16N mechanical data

Figure 9. SO-16N package dimensions

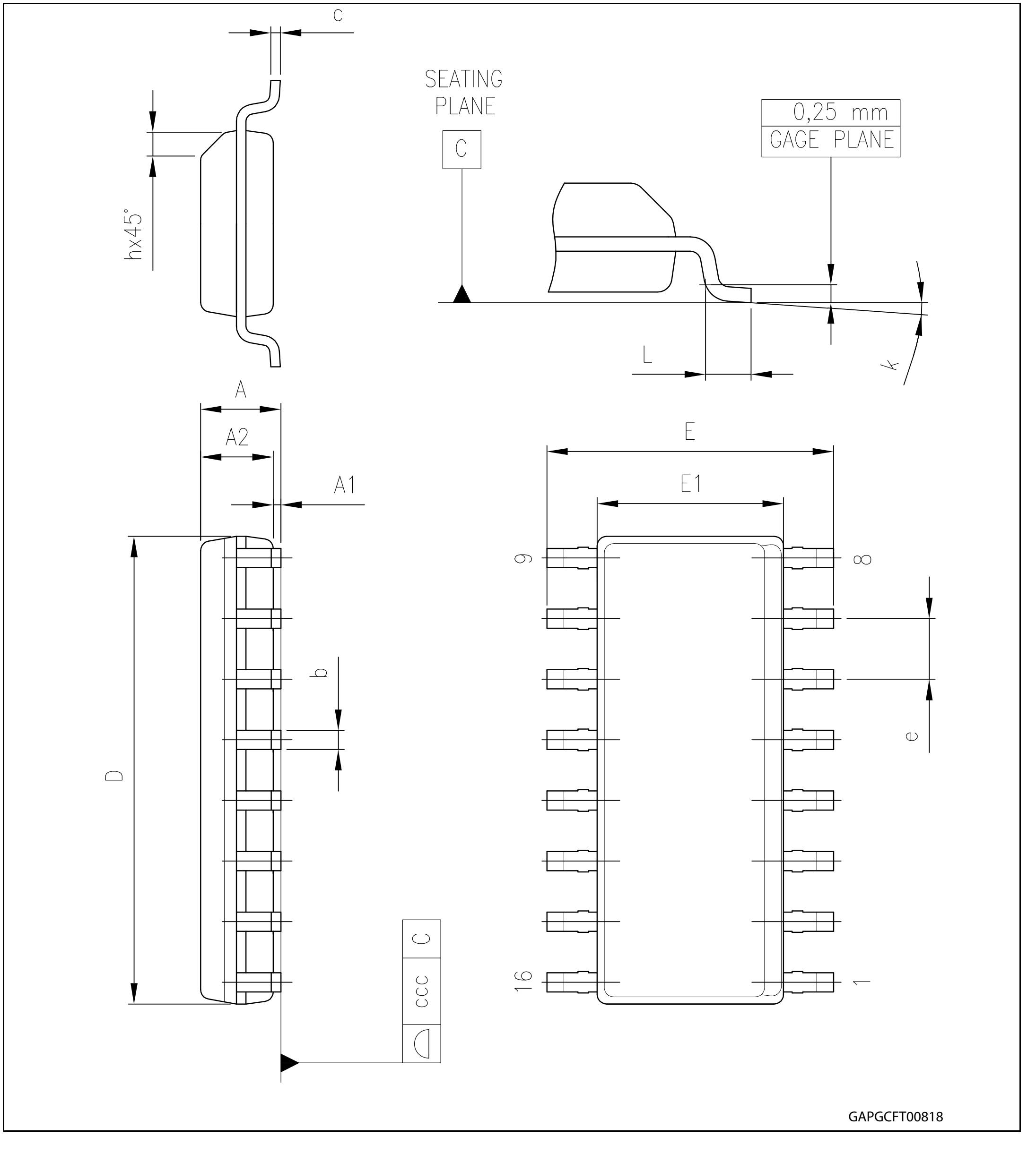

Table 15. SO-16N mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8
ccc			1.10

5 Revision history

Table 16. Document revision history

Date	Revision	Changes
19-May-2014	1	Initial release.
30-Jun-2014	2	Updated *Features* list Updated *Figure 1: Block diagram* and *Figure 2: Configuration diagram (top view)* *Table 3: Pin definitions and functions*: – Pin 13: updated symbol *Table 4: Absolute maximum ratings* – I_{SENSE}, V_{ESD}: updated parameter *Table 6: Power section* – I_S: updated values – T_{D_stby}, R_{ONHS}, R_{ONLS}, V_f, $I_{L(off)}$: updated test conditions – $I_{L(off\_h)}$: added row *Table 7: Logic inputs (INA, INB, PWM) (VCC = 7 V up to 28 V; -40°C < Tj < 150°C)* – I_{PWM}, I_{PWMH}, V_{PWMCL}: updated test conditions *Table 8: Switching (VCC = 13 V; RLOAD = 5.2 Ω)*: – $t_{d(on)}$, $t_{d(off)}$: updated values – t_{cross}: added row *Table 9: Protections and diagnostics (VCC = 7 V up to 18 V; -40°C < Tj < 150°C)* – I_{SD_LS}: updated value – t_{SD_LS}: updated value and test conditions – Renamed parameter V_{CLPHsd} into V_{CL_HSD}, V_{CLPLSD} into V_{CL_LSD} and V_{CLP} into V_{CL}; updated test conditions – V_{OL}, $I_{L(off2)}$, t_{DSTKON}, t_{D_VOL}: updated test conditions *Table 10: CS (7 V < VCC < 18 V; -40 °C < Tj < 150 °C)* – K_2, K_3, dK_2/K_2: updated test conditions – I_{SENSE0}: updated parameter, test conditions and value – Renamed V_{SENSE} parameter into V_{SENSEH}: updated value *Table 11: Operative condition - truth table*, *Table 12: On-state fault conditions- truth table Fault on leg A (preliminary)* and *Table 13: Off-state -truth table*: – Changed Multisense with CS

Table 16. Document revision history (continued)

Date	Revision	Changes
28-Jul-2014	3	*Table 4: Absolute maximum ratings*: – V_{ESD}: updated value *Table 6: Power section*: – t_{D_STBY}: updated test condition *Table 7: Logic inputs (INA, INB, PWM) (VCC = 7 V up to 28 V; -40°C < Tj < 150°C)*: – V_{SELCL}, V_{PMWCL}: updated value *Table 8: Switching (VCC = 13 V; RLOAD = 5.2 Ω)*: – updated R_{LOAD} value – $t_{d(on)}$, $t_{d(off)}$: updated value *Table 9: Protections and diagnostics (VCC = 7 V up to 18 V; -40°C < Tj < 150°C)*: – I_{SD_LS}, V_{CL_HSD}, V_{CL_LSD}, V_{CL}: updated value – t_{DSTKON}, t_{D_VOL}: updated test condition – $t_{Latch\_RST\_HD}$, $t_{Latch\_RST\_LS}$: added parameter *Table 10: CS (7 V < VCC < 18 V; -40 °C < Tj < 150 °C)*: – K_x, dK_x/K_x, $V_{SENSEsat}$, I_{SENSE0}: updated test conditions Updated *Figure 8: Time to shutdown for the low-side driver*
30-Oct-2014	4	*Table 6: Power section*: – t_{D_STBY}: updated test condition *Table 10: CS (7 V < VCC < 18 V; -40 °C < Tj < 150 °C)*: – V_{SENSE_CL}, I_{SENSE_SAT}, I_{OUT_SAT}, V_{OUT_MSD}: added parameters – V_{SENSE_SAT}, I_{SENSE0}, V_{SENSEH}, I_{SENSEH}: updated test conditions Updated *Figure 7: Low-side turn-on delay time*

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