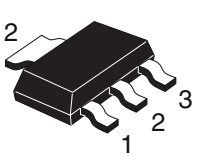
VNL5160N3-E
VNL5160S5-E

OMNIFET III
fully protected low-side driver

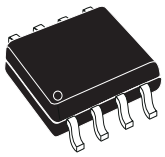
Features

Type	V_{clamp}	$R_{DS(on)}$	I_D
VNL5160N3-E	41 V	160 mΩ	3.5 A
VNL5160S5-E			

- Drain current:3.5A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC European directive
- Open drain status output[(a)]
- Specially intended for R10W or 2x R5W automotive signal lamps



SOT-223


SO-8

Description

The VNL5160N3-E and VNL5160S5-E are monolithic devices, made using STMicroelectronics® VIPower® Technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short circuit. Output current limitation protects the devices in an overload condition. In the case of a long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

a. Valid for VNL5160S5-E only.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SOT-223	VNL5160N3-E	VNL5160N3TR-E
SO-8	VNL5160S5-E	VNL5160S5TR-E

Contents

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List of figures

1 Block diagrams and pins configurations

Figure 1. VNL5160N3-E block diagram

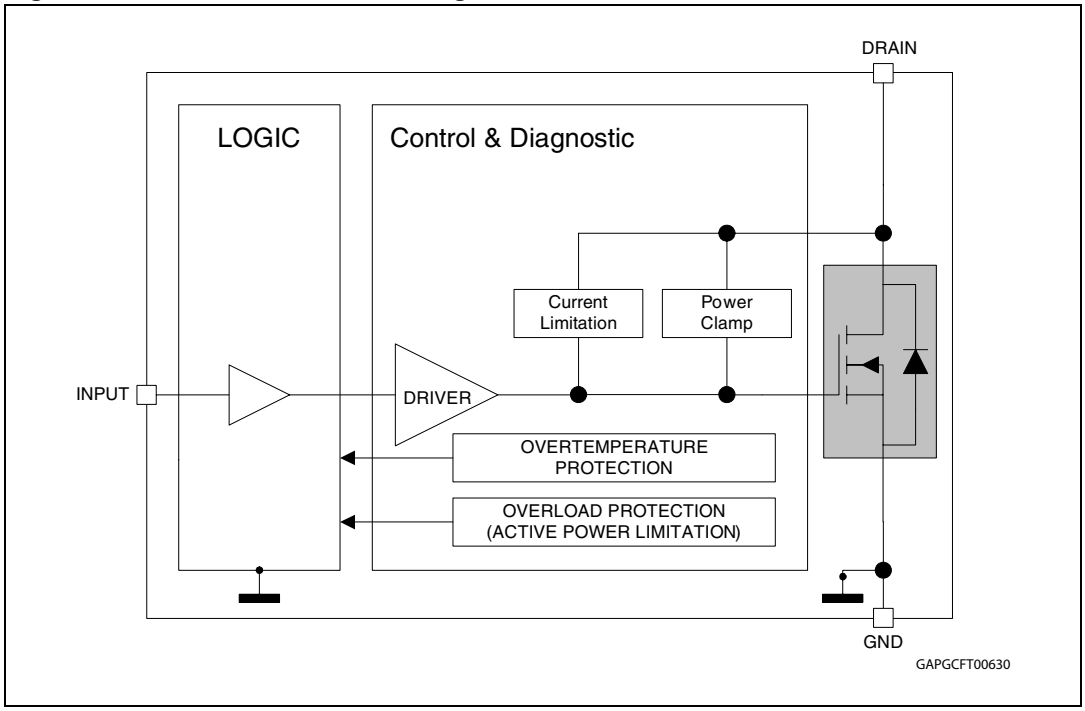


Figure 2. VNL5160S5-E block diagram

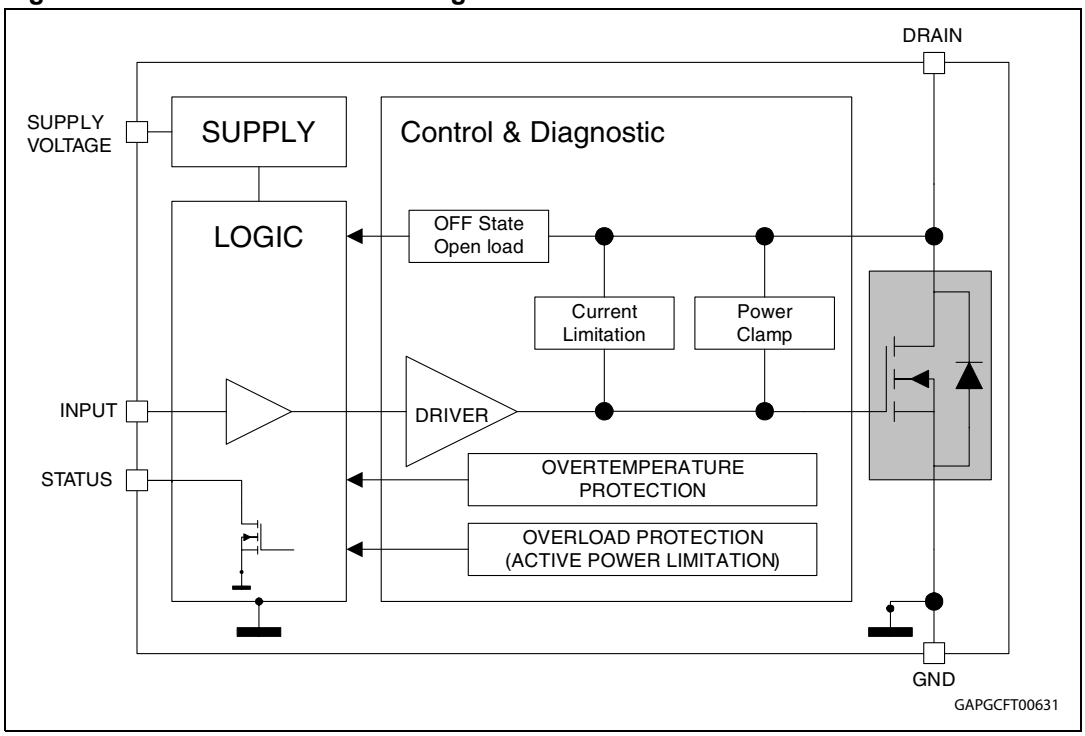


Table 2. Pin function

Name	Function
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state(1)
DRAIN	PowerMOS drain
SOURCE	PowerMOS source and ground reference for the control section
SUPPLY VOLTAGE	Supply voltage connected to the signal part (5V)
STATUS	Open drain digital diagnostic pin(2)

1. Internally connected to V_{supply} in the VNL5160N3-E.
2. Valid for VNL5160S5-E only.

Figure 3. VNL5160N3-E current and voltage conventions

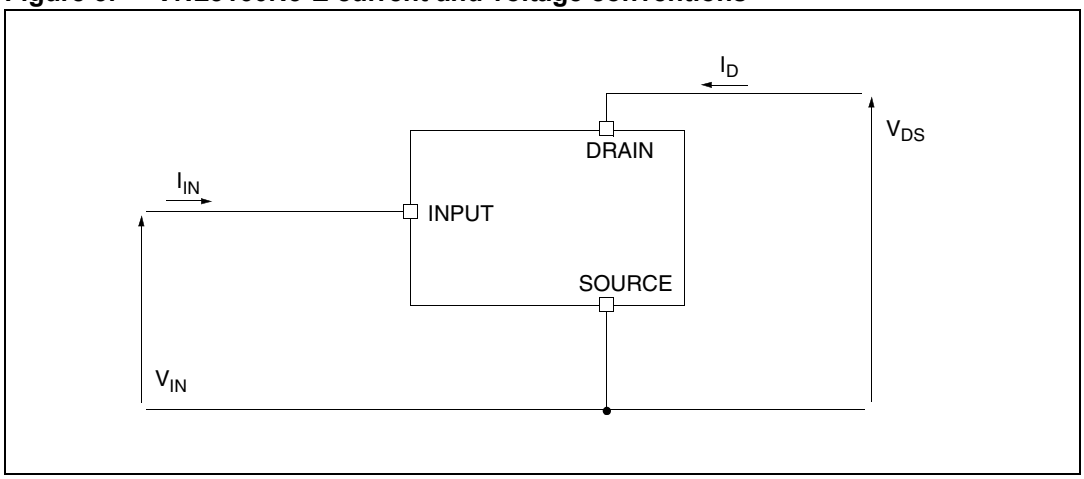


Figure 4. VNL5160S5-E current and voltage conventions

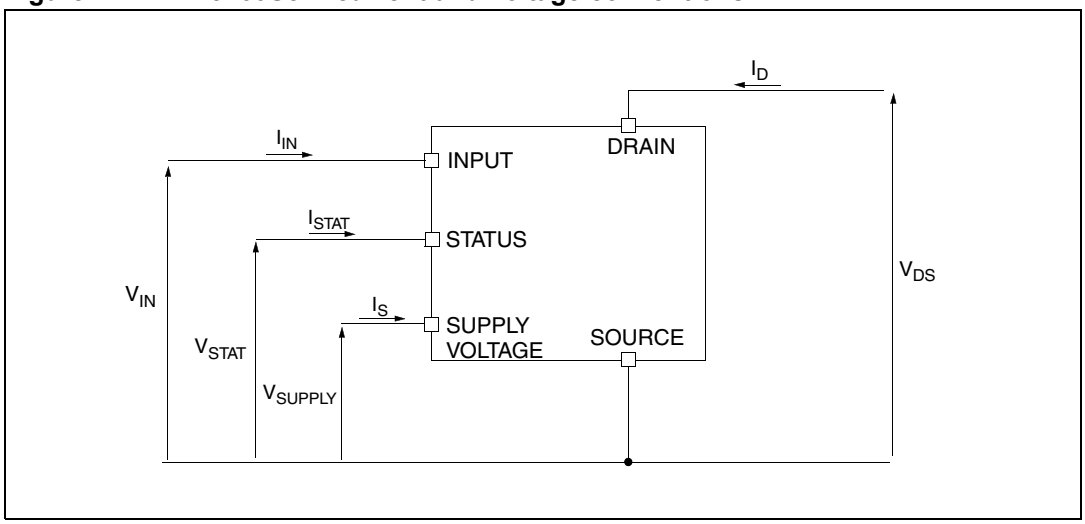


Figure 5. Configuration diagrams (top view)

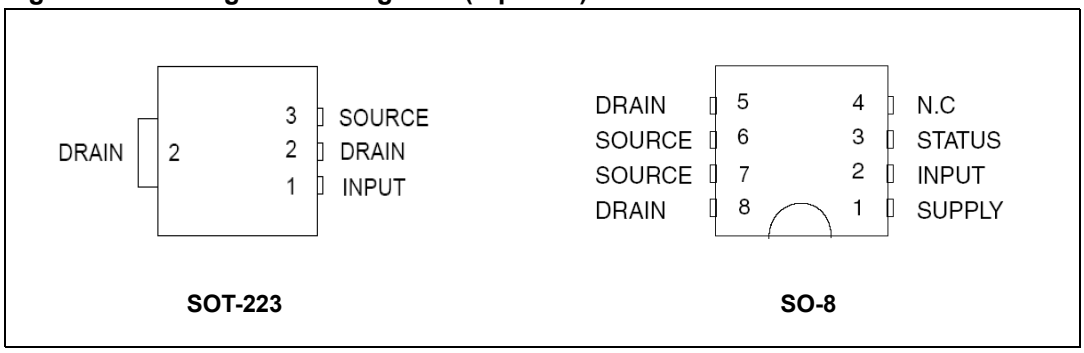


Table 3. Suggested connections for unused and not connected pins

Connection/pin	Status	N.C.	Input
Floating	X	X	X
To ground	Not allowed	X	Through 10kΩ resistor

2 Absolute maximum rating

Stressing the device above the rating listed in *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document

2.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
V_{DS}	Drain-source voltage (V_{IN}=0V)	Internally clamped		V
I_D	DC drain current	Internally limited		A
- I_D	Reverse DC drain current	-4		A
I_S	DC supply current	-	-1 to 10	mA
I_{IN}	DC input current	-1 to 10		mA
I_{STAT}	DC status current	-	-1 to 10	mA
V_{ESD1}	Electrostatic discharge (R=1.5kΩ; C=100pF) – INPUT – STATUS – SUPPLY – DRAIN	 4000 4000 4000 5000		V
V_{ESD2}	Electrostatic discharge on output pin only (R=330Ω, C=150pF)	2000		V
T_j	Junction operating temperature	-40 to 150		°C
T_{stg}	Storage temperature	-55 to 150		°C
E_{as}	Single pulse avalanche energy L = 8.5 mH, T_j = 150 °C, R_L = 0 Ω, V_{batt} = 13.5 V, I_{out} = I_{limL}	37		mJ

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Maximum value		Unit
		SOT-223	SO-8	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	146.8(1)	103.1	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5cm2 of Cu (at least 35 µm thick) connected to all DRAIN pins

3 Electrical characteristics

Values specified in this section are for $V_{IN} = V_{supply}$ = 4.5 V to 5.5 V, -40 °C < T_j < 150 °C, unless otherwise stated.

Table 6. PowerMOS section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{supply}	Operating supply voltage		3.5	5	5.5	V
R_{ON}	On-state resistance	$V_{IN} = V_{supply}$ = 5V I_D = 1 A; T_j = 25 °C I_D = 1 A; T_j = 150 °C		160	170 320	mΩ mΩ
V_{CLAMP}	Drain-source clamp voltage	V_{IN} = 0 V; I_D = 1 A	41	46	52	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN} = 0 V; I_D = 2 mA	36			V
I_{DSS}	Off-state output current	V_{IN} = 0 V; V_{DS} = 13 V; T_j = 25 °C V_{IN} = 0 V; V_{DS} = 13 V; T_j = 125 °C	0 0		3 5	µA

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	I_D = 1 A; V_{IN} = 0 V		0.8		V

Table 8. Input section(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ISS}	Supply current from input pin	On-state $V_{IN} = V_{supply}$ = 5 V; V_{DS} = 0 V		30	110	µA
V_{ICL}	Input clamp voltage	I_S = 1 mA I_S = -1 mA	5.5	 -0.7	7	V V
V_{INTH}	Input threshold voltage	$V_{DS} = V_{IN}$; I_D = 1 mA	1		3.5	V

1. Valid for VNL5160N3-E option (input & supply pins connected together).

Table 9. Status pin(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation, V_{STAT} = 5 V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation, V_{STAT} = 5 V			100	pF
V_{STCL}	Status clamp voltage	I_{STAT} = 1 mA I_{STAT} = -1 mA	5.5	 -0.7	7	V V

1. Valid for VNL5160S5-E option.

Table 10. Logic input(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.13			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA I_{IN} = -1 mA	5.5	 -0.7	7	V V

1. Valid for VNL5160S5-E option.

Table 11. Openload detection(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OI}	Open-load off-state voltage detection threshold	V_{IN} = 0 V	0.6	1.2	1.7	V
$t_{d(oloff)}$	Delay between INPUT falling edge and STATUS falling edge in openload condition	I_{OUT} = 0 A	45	425	1100	µs

1. Valid for VNL5160S5-E option.

Table 12. Supply section(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	Off-state T_j = 25 °C; V_{IN} = V_{DRAIN} = 0 V; On-state T_j = 25 °C; V_{IN} = 5 V; V_{DS} = 0 V		10 25	25 110	µA µA
V_{SCL}	Supply clamp voltage	I_{SCL} = 1mA I_{SCL} = -1mA	5.5	 -0.7	7	V V

1. Valid for VNL5160S5-E option.

Table 13. Switching characteristics (Vcc=13V[1])

Symbol	Parameter	Test conditions	SOT-223[2]			SO-8			Unit
			Min.	Typ.	Max	Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on delay time	R_L = 13Ω, V_{CC} = 13V[3]		8.9			8.9		µs
$t_{d(OFF)}$	Turn-off delay time	R_L = 13Ω, V_{CC} = 13V		13.2			13.2		µs
t_r	Rise time	R_L = 13Ω, V_{CC} = 13V		14.1			14.1		µs
t_f	Fall time	R_L = 13Ω, V_{CC} = 13V		11.5			11.5		µs
W_{ON}	Switching energy losses at turn-on	R_L = 13Ω, V_{CC} = 13V		34.3			34.3		µJ
W_{OFF}	Switching energy losses at turn-off	R_L = 13Ω, V_{CC} = 13V		34.3			34.3		µJ

1. See *Figure 7: VNL5160N3-E application schematic* and *Figure 8: VNL5160S5-E application schematic*.
2. 3.5 V < Vs_{upply} = Vin < 5.5 V.
3. See *Figure 6: Switching characteristics*.

Table 14. Protection and diagnostics

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{DS} = 13V; V_{IN} = V_{supply} = 5V	3.5	5	7.5	A
I_{limL}	Short circuit current during thermal cycling	V_{DS} = 13V; $T_R < T_j < T_{TSD}$; V_{IN} = V_{supply} = 5V		2.5		A
t_{dlim}	Step response current limit	V_{DS} = 13V; V_{input} = 5V		20		µs
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS}+1	T_{RS}+5		°C
T_{RS}[2]	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C

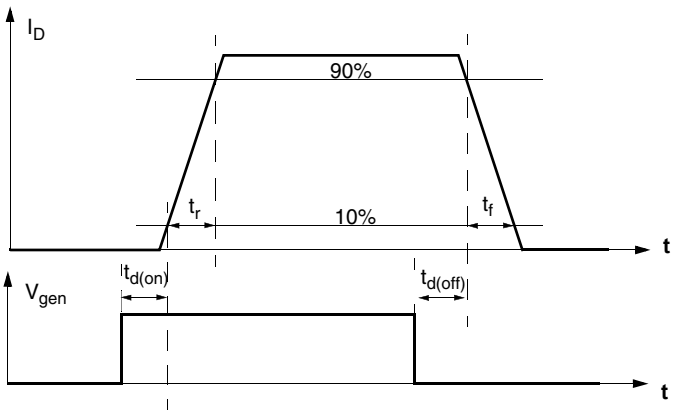
1. V_{supply}=V_{input} in VNL5160N3-E version.
2. Valid for VNL5160S5-E option.

Table 15. Truth table (1)

Conditions	INPUT	DRAIN	STATUS
Normal operation	L H	H L	H H
Current limitation	L H	H X	H H
Overtemperature	L H	H H	H L
Undervoltage	L H	H H	X X
Output voltage < V_{OL}	L H	L L	L H

1. Valid for VNL5160S5-E option

Figure 6. Switching characteristics



4 Application information

Figure 7. VNL5160N3-E application schematic

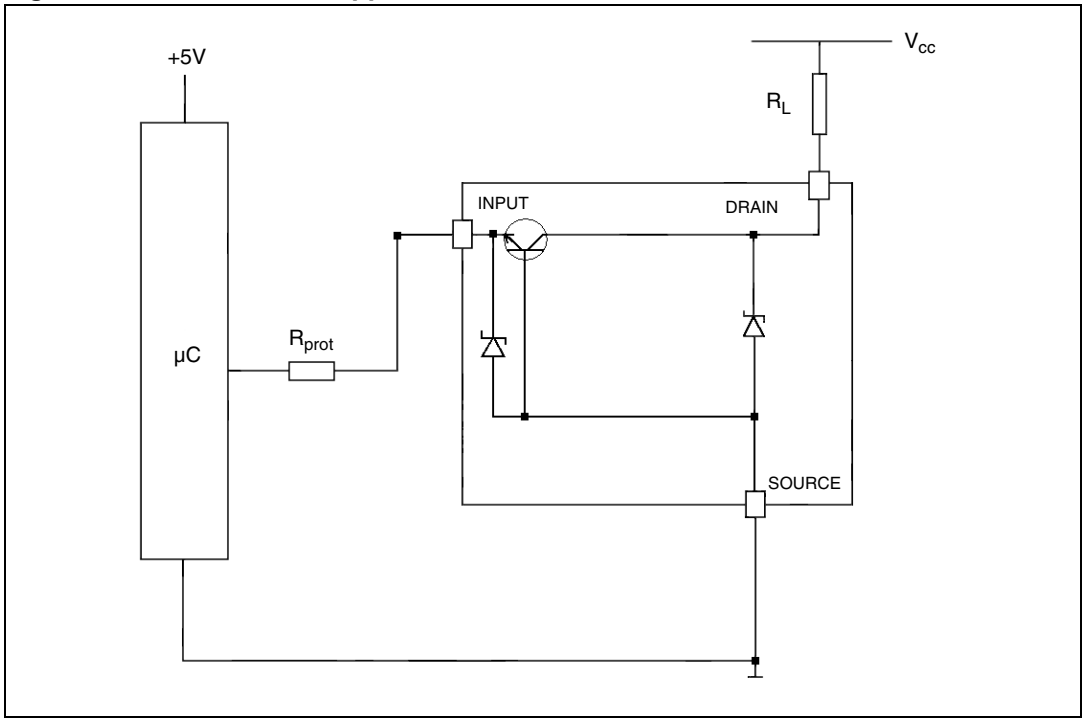
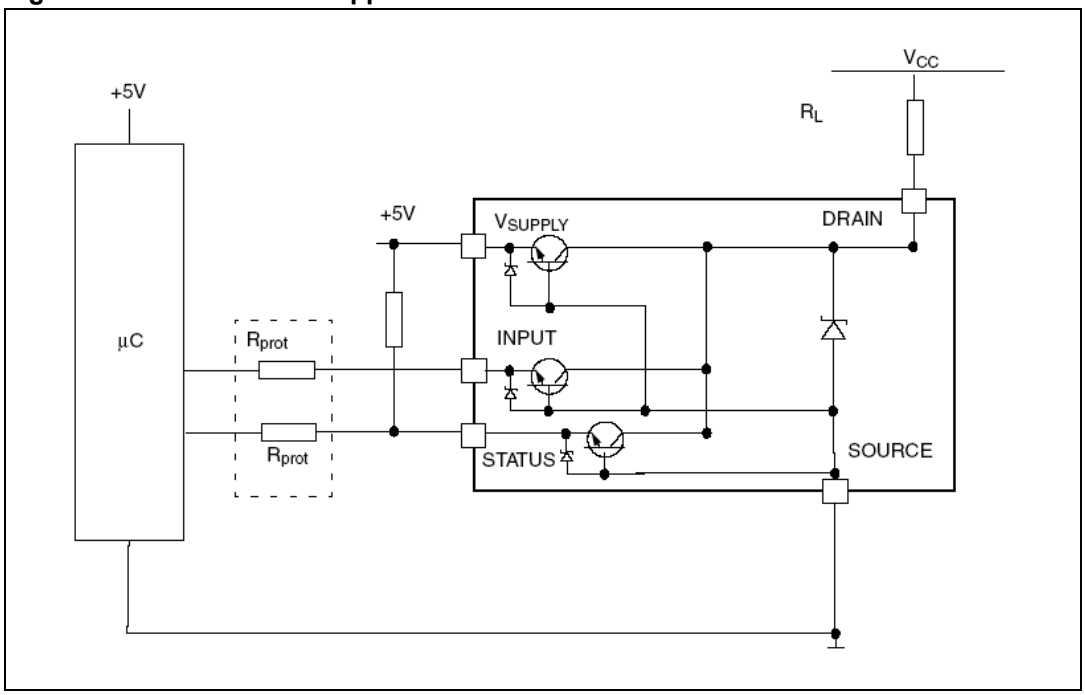


Figure 8. VNL5160S5-E application schematic



4.1 MCU I/O protection

ST suggests to insert a resistor (Rprot) in line to prevent the µC I/O pins from latching up[b]. The value of these resistors is a compromise between the leakage current of µC and the current required by the LSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os:

$0.7/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}) / I_{IHmax}$

Calculation example:

For the following conditions:

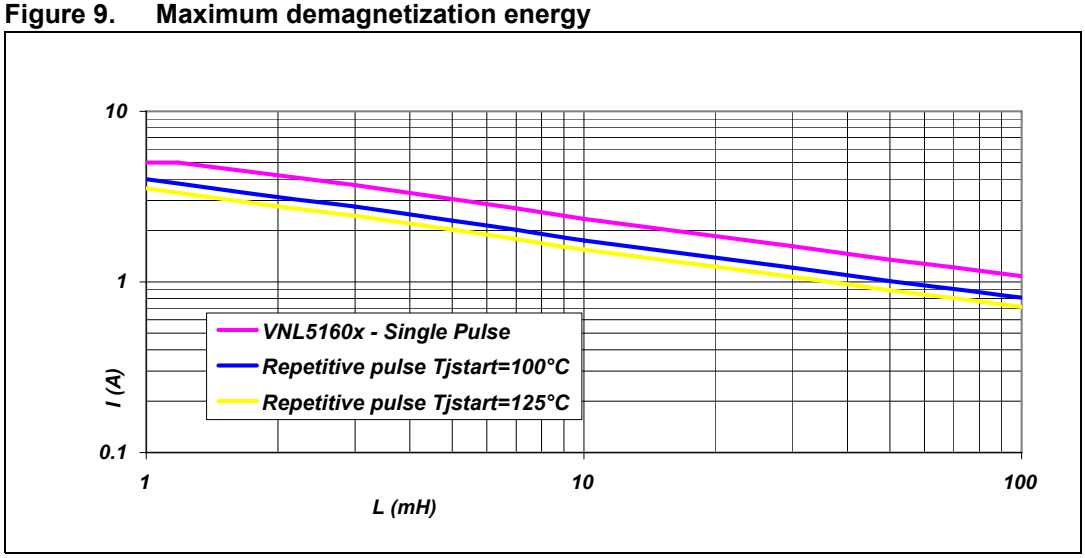
$I_{latchup} \geq 20mA$

$V_{OH\mu C} \geq 4.5V$

$35\Omega \leq R_{prot} \leq 100k\Omega$.

Recommended value is $R_{prot} = 10k\Omega$

Figure 9. Maximum demagnetization energy

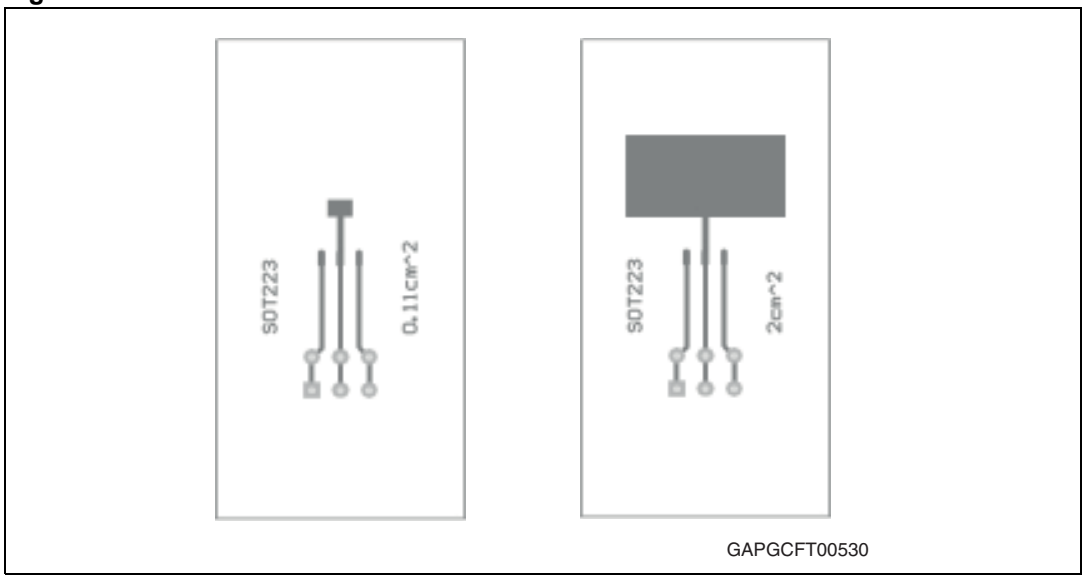


b. In case of negative transient on the drain pin.

5 Package and PC board thermal data

5.1 SOT-223 thermal data

Figure 10. SOT-223 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 30 mm x 30 mm,PCB thickness = 2 mm, Cu thickness=35 µm, Copper areas: from minimum pad layout to 0.8 cm^2).

Figure 11. SOT-223 $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

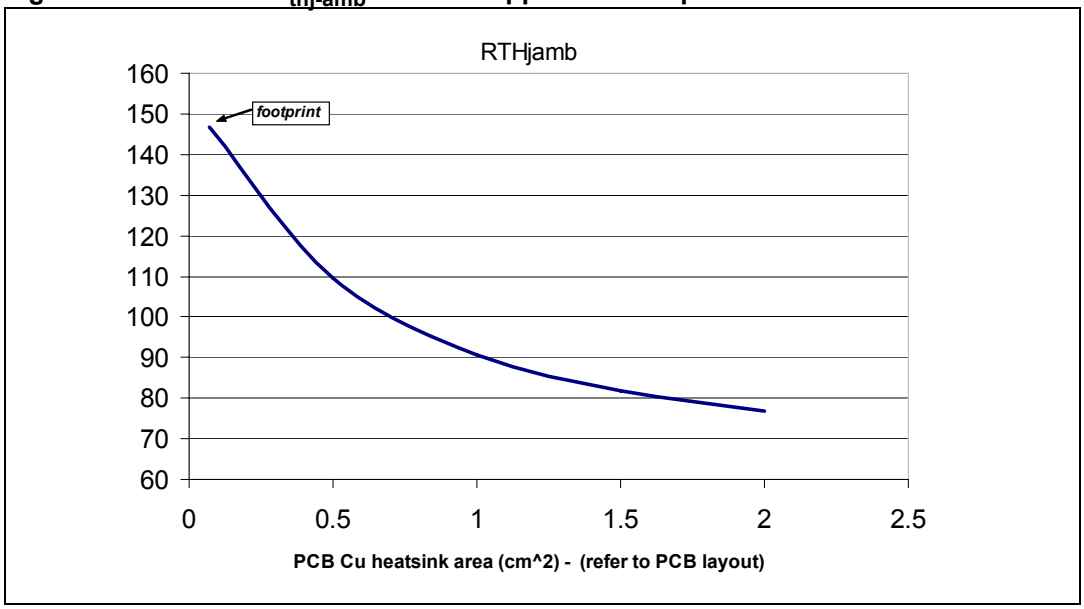
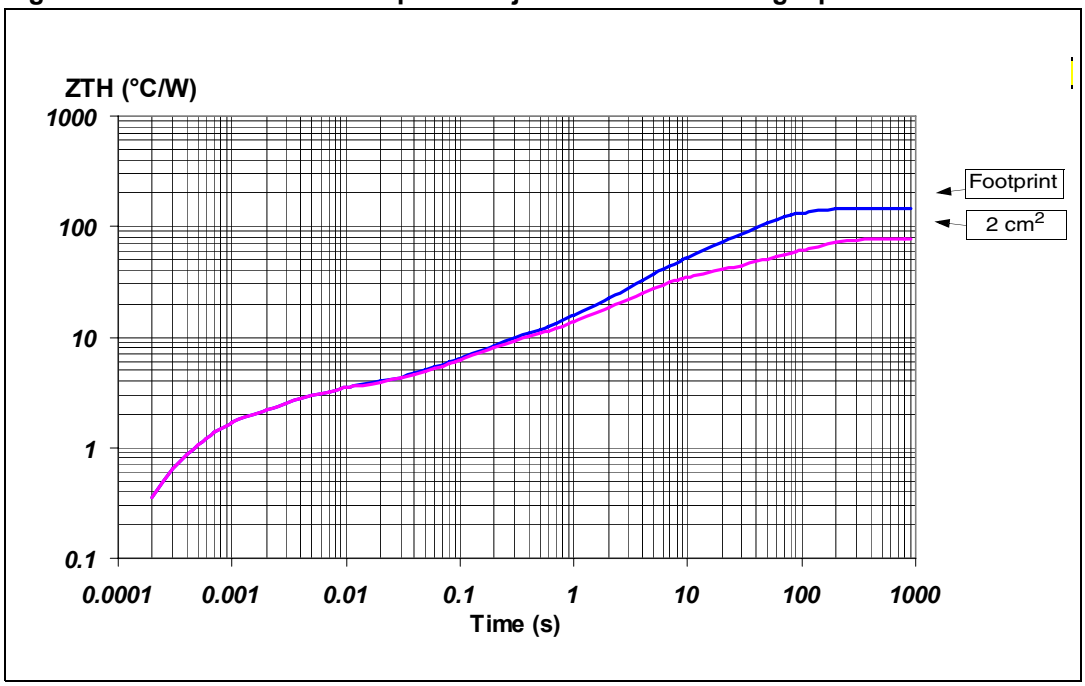


Figure 12. SOT-223 thermal impedance junction ambient single pulse

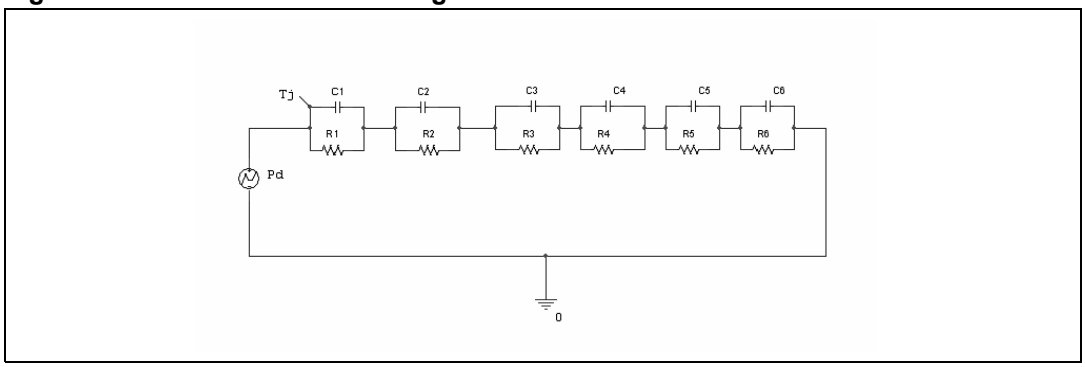


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 13. SOT-223 thermal fitting model(1)



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. SOT-223 thermal parameter

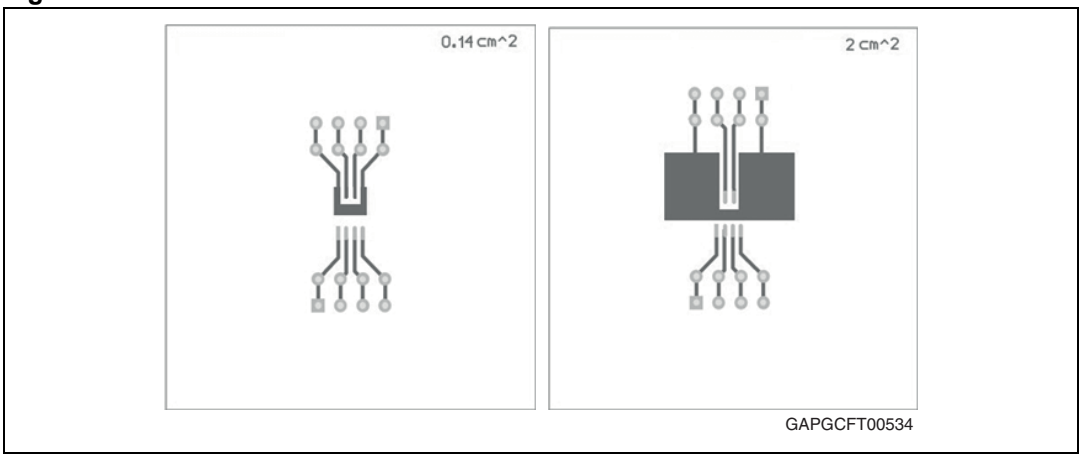
Area/island (cm^2)	FP	2
R1 (°C/W)	1.4	
R2 (°C/W)	1.8	
R3 (°C/W)	4.5	
R4 (°C/W)	24	

Table 16. SOT-223 thermal parameter (continued)

Area/island (cm^2)	FP	2
R5 (°C/W)	0.1	
R6 (°C/W)	115	45
C1 (W·s/°C)	0.0003	
C2 (W·s/°C)	0.002	
C3 (W·s/°C)	0.03	
C4 (W·s/°C)	0.16	
C5 (W·s/°C)	1000	
C6 (W·s/°C)	0.4	2

5.2 SO-8 thermal data

Figure 14. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm,PCB thickness = 2 mm, Cu thickness=35 µm, Copper areas: from minimum pad layout to 2 cm^2).

Figure 15. SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition

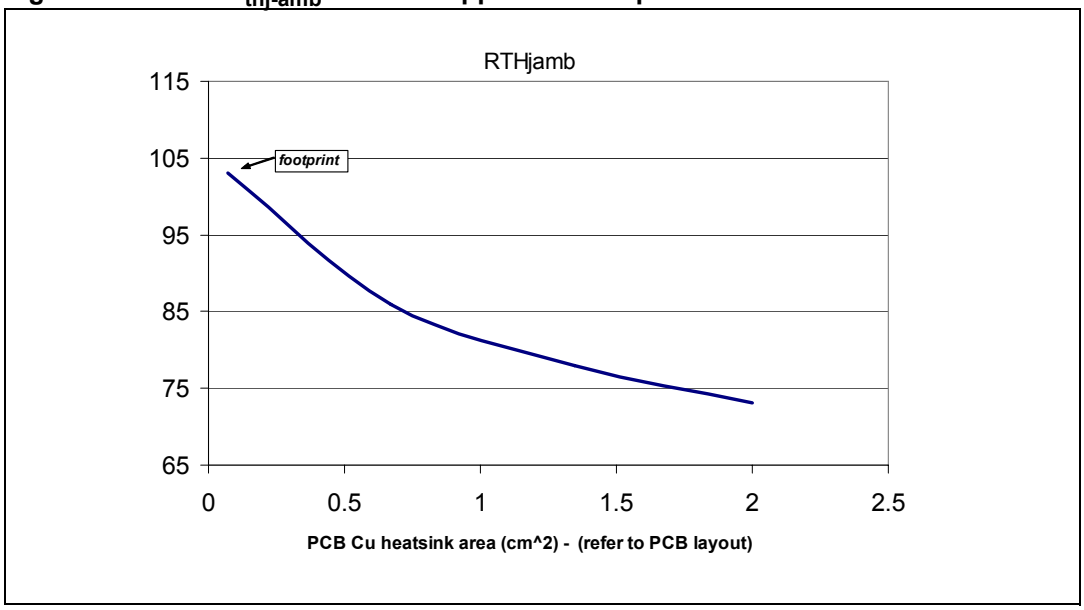
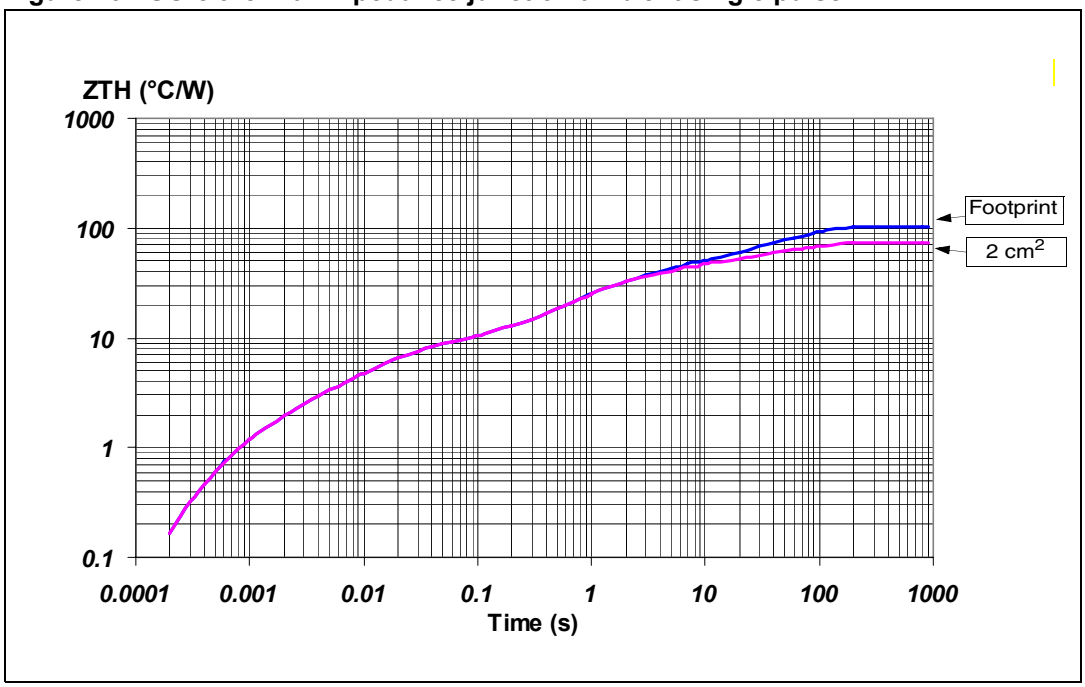


Figure 16. SO-8 thermal impedance junction ambient single pulse

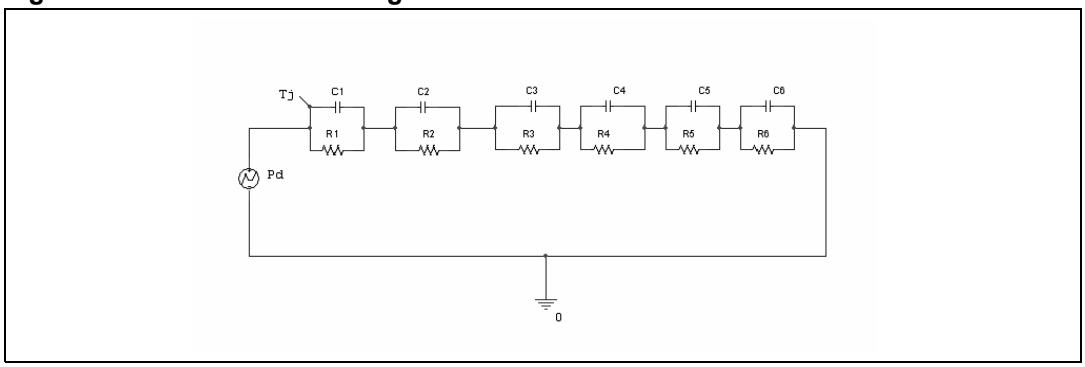


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 17. SO-8 thermal fitting mode(1)l



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. SO-8 thermal parameter

Area/island (cm^2)	0.07	2
R1 (°C/W)	1.4	
R2 (°C/W)	3.2	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.0008	
C2 (W·s/°C)	0.0032	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

6 Package and packing information

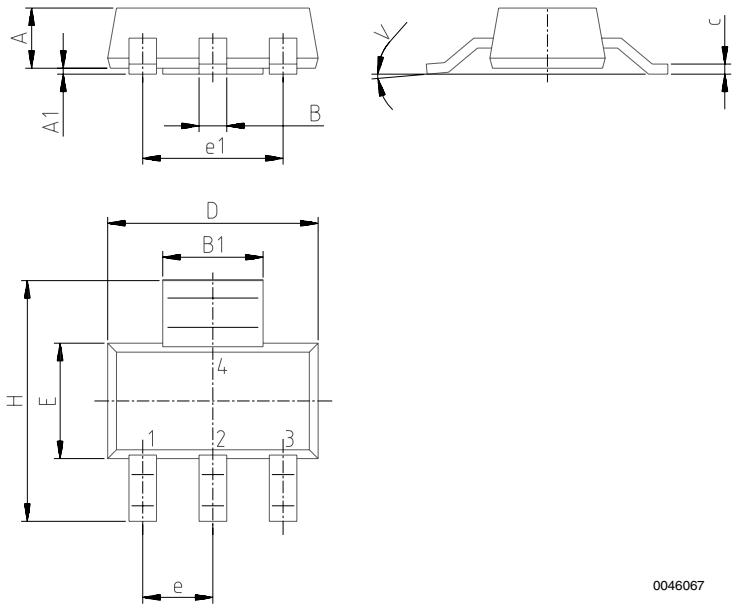
6.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 SOT-223 mechanical data

Figure 18. SOT-223 mechanical data & package outline



Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.8			0.071
B	0.6	0.7	0.85	0.024	0.027	0.033
B1	2.9	3	3.15	0.114	0.118	0.124
c	0.24	0.26	0.35	0.009	0.01	0.014
D	6.3	6.5	6.7	0.248	0.256	0.264
e		2.3			0.09	
e1		4.6			0.181	
E	3.3	3.5	3.7	0.13	0.138	0.146
H	6.7	7	7.3	0.264	0.276	0.287
V	10° (max)					
A1	0.02		0.1	0.0008		0.004

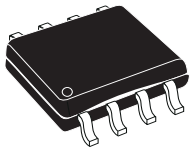
6.3 SO8 mechanical data

Figure 19. SO8 mechanical data & package outline

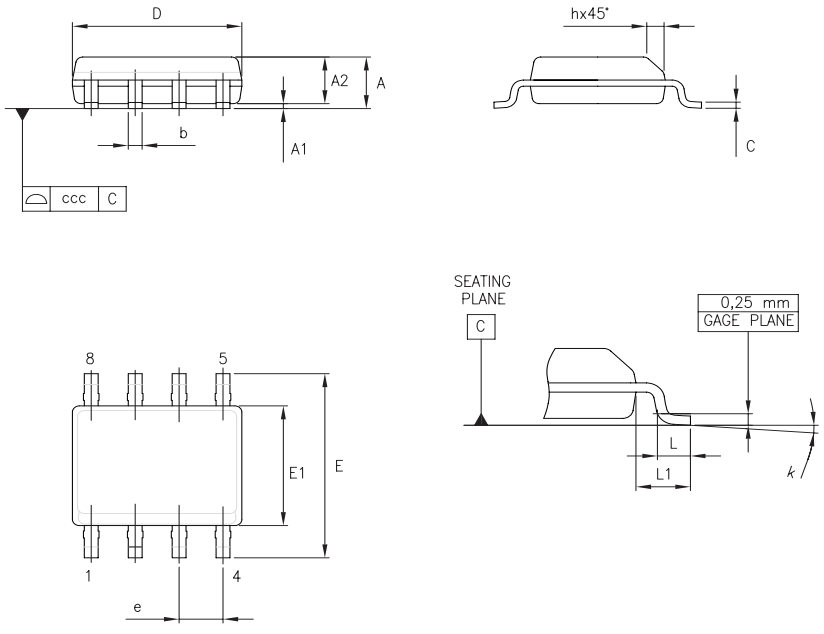
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
c	0.170		0.230	0.0067		0.0091
D (1)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(2)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0˚		8˚	0˚		8˚
ccc			0.100			0.0039

Notes: 1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

OUTLINE AND MECHANICAL DATA



SO-8

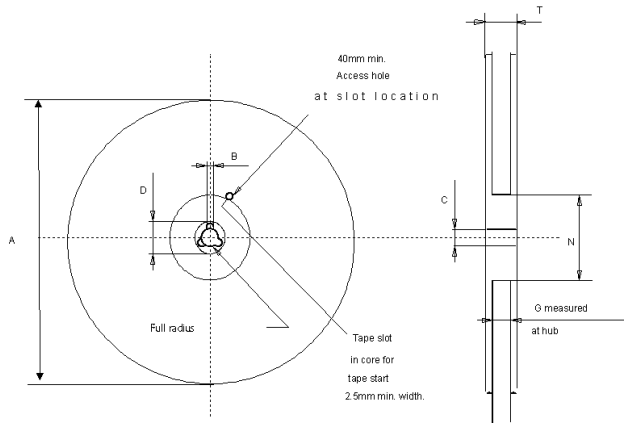


0016023 D

6.4 SOT-223 packing information

The devices can be packed in tube or tape and reel shipments (see the *Table 1: Device summary*).

Figure 20. SOT-223 tape and reel shipment (suffix “TR”)



Reel dimensions

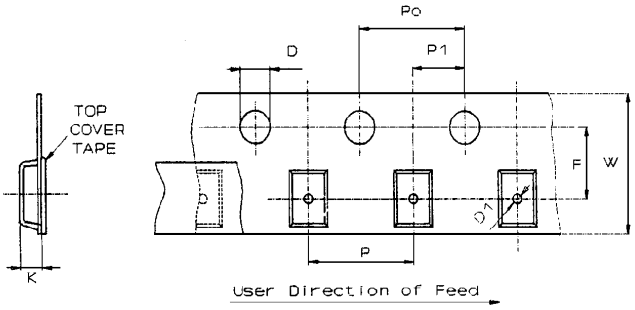
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

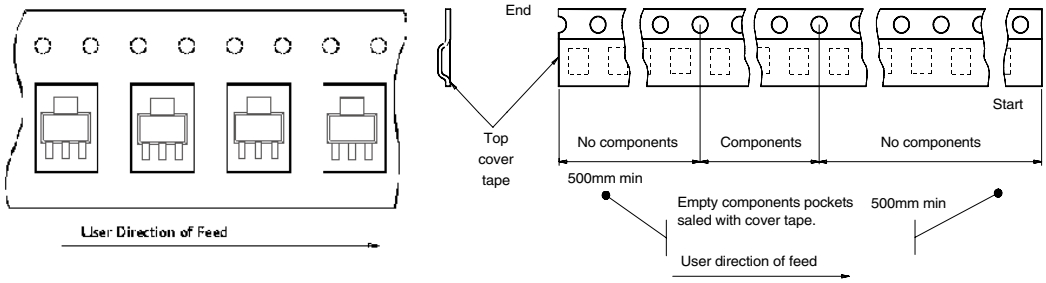
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

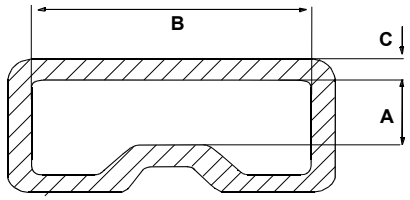
All dimensions are in mm.





6.5 SO8 packing information

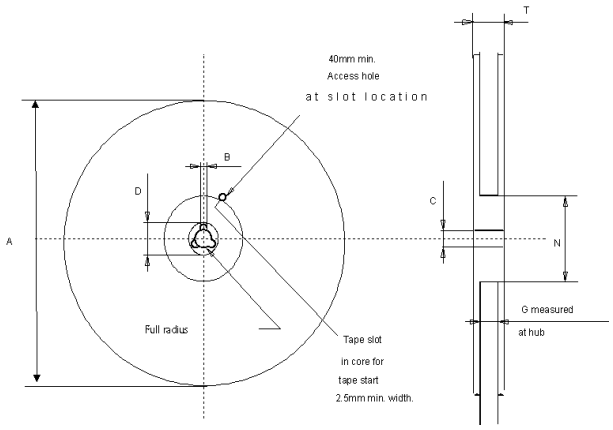
Figure 21. SO-8 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

Figure 22. SO-8 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

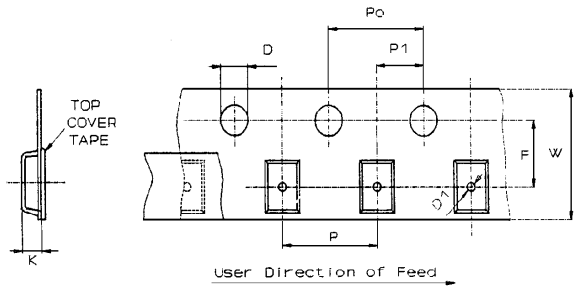
All dimensions are in mm.

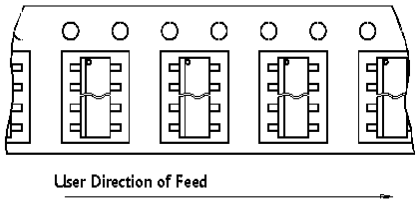
TAPE DIMENSIONS

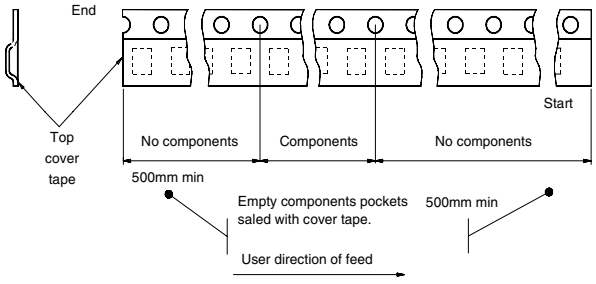
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







7 Revision history

Table 18. Document revision history

Date	Revision	Changes
17-Nov-2009	1	Initial release.
20-Feb-2012	2	Update the entire document in ST template. Update *Section : Features* in cover page.

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