



## ABSOLUTE MAXIMUM RATINGS\*

Supply Voltage, $V_{CC} - V_{DS}$ .....	0 to 5.5V
Input Volotage, $V_{IN}$ .....	$V_{DS}$ to $V_{CC}$
Operating Temperature, $T_{OP}$ .....	-10°C to 60°C
Storage Temperature, $T_{ST}$ .....	-20°C to 80°C

\* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## ELECTRICAL CHARACTERISTICS

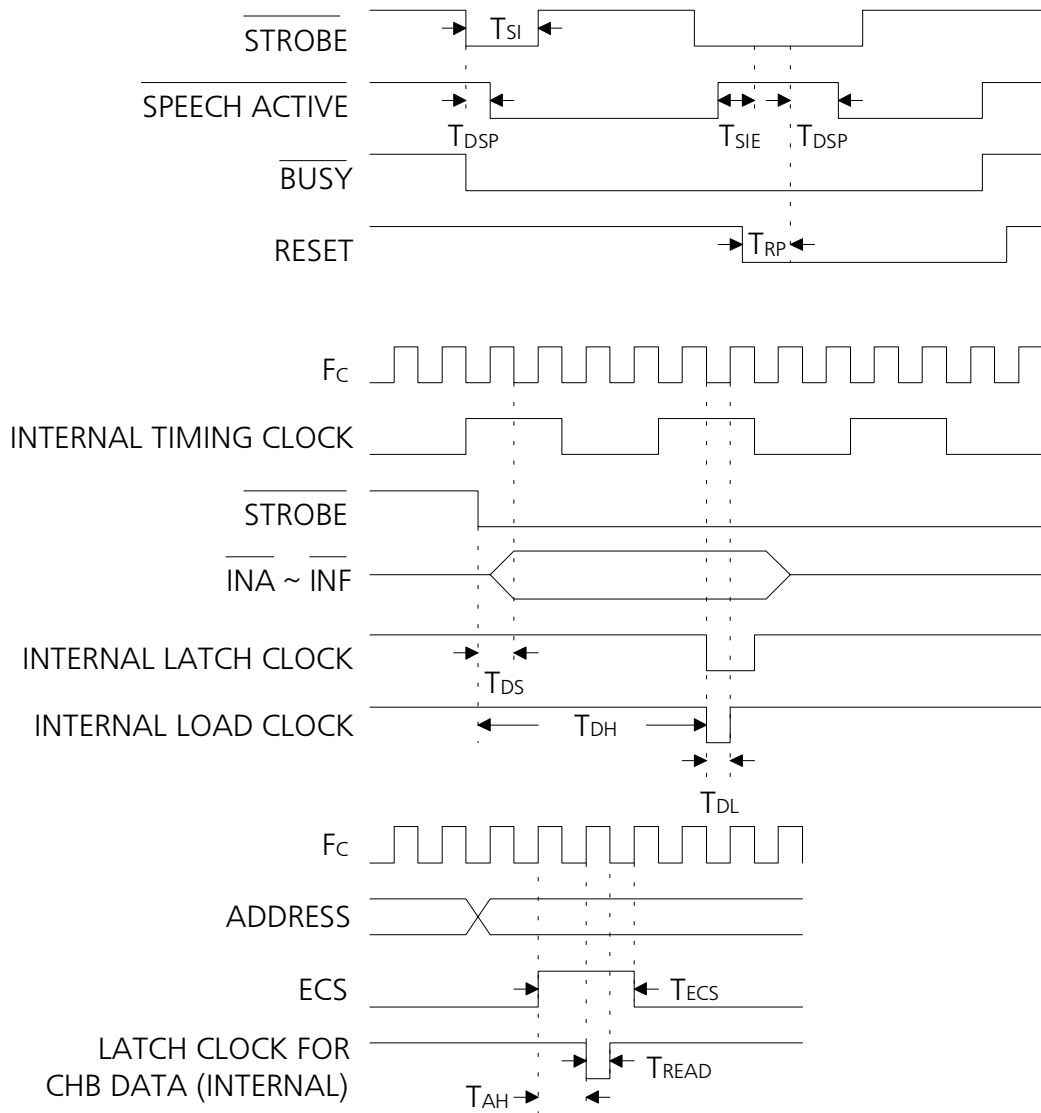
Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{CC}$	Supply Voltage	4.5	5	5.5	V
$I_{DD}$	Standby Current		50		uA
$I_{DRIVE}$	Output Current $V_{OH}=2.4V$		4		mA
$I_{SINK}$	Output Current $V_{OL}=0.4V$		4		mA
$V_{IH}$	Input Voltage (High)		3.5		V
$V_{IL}$	Input Voltage (Low)		1.5		V
$F_C$	Internal Scan Clock		8		MHz
$F_S$	Sampling Clock	20	32	128	KHz
$T_{RESET}$	Reset Pulse Width		1		us
$T_{SI}$	Strobe Input Pulse Width		1		us
$T_{SIE}$	Strobe Inhibit Time After EOS <sup>(1)</sup>		1.5		ms
$T_{DSP}$	Delay Time From Strobe To Play <sup>(2)</sup>			150	ms
$T_{RP}$	Edge-Triggered Reset Interval		1		us
$T_{DS}$	Data Setup Time For INA ~ INF			350	ns
$T_{DH}$	Data Hold Time For INA ~ INF		1		us
$T_{DL}$	Internal Load Pulse For INA ~ INF		65		ns
$T_{ECS}$	Address Valid Time For Ch. B EPROM		250		ns
$T_{READ}$	Internal Latch Pulse For Ch. B EPROM Data		65		ns
$T_{AH}$	Address Stable Time For Ch. B			125	ns

### Note:

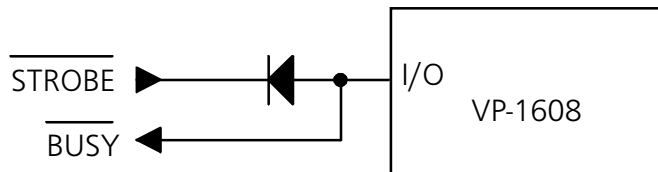
(1) EOS = End-Of-Speech

(2) Based on 1M EPROM scanning.

# TIMING DIAGRAM



## TEST CIRCUIT FOR I/O PIN



## PIN DESCRIPTIONS

### A0 ~ A19:

Address output to EPROM. Both channels share the same address lines in a 50-50 time sharing fashion. Pin ECS (described below) must be examined to tell who's address is valid at any particular moment.

### ANG1 & ANG1\:

Differential audio output for channel A, connect to LM324 or LM358.

### ANG2 & ANG2\:

Differential audio output for channel B, connect to LM324 or LM358.

### ANGD1:

Audio feedback input for channel A.

### ANGD2:

Audio feedback input for channel B.

### D0 ~ D7:

Data input from EPROM.

### ECS:

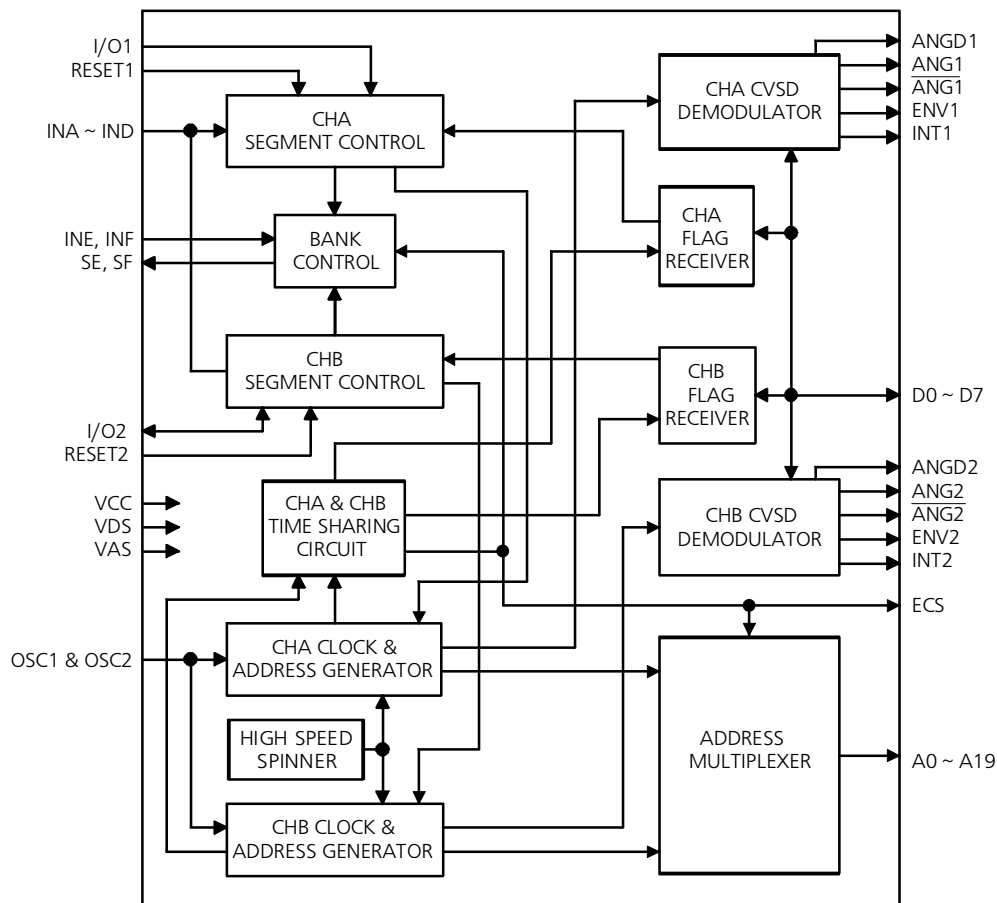
EPROM Channel Select output. This signal is used to indicate who's address is on the address lines. When the ECS is low, the address is for channel A. When the ECS is high, the address is for channel B.

If both channels share one EPROM, this signal is usually connected to the highest address line so that each channel uses exactly half the EPROM space. If more than one EPROM are used, this signal is usually used by the address decoder to select the proper EPROM.

### ENV1:

Envelop input for channel A, to be connected to INT1 with a feedback resistor.

## Block Diagram



**ENV2:**

Envelop input for channel B, to be connected to INT2 with a feedback resistor.

**INT1:**

Integrator output for channel A, to be connected to an external RC integration circuitry.

**INT2:**

Integrator output for channel B, to be connected to an external RC integration circuitry.

**I/O1:**

Strobe input/Busy output for channel A, active low. To play a message on channel A, place the segment/bank code on INA to INE and strobe this pin with a low pulse. During the playback this pin becomes an active-low "busy" output. If this pin is held low at the end of playback, the message will be re-triggered.

**I/O2:**

Same as I/O1 except that this pin is for channel B.

**INA ~ IND:**

Input for segment code in binary format. INA is the LSB and IND is the MSB.

**INE, INF:**

Input for bank code in binary format, max. 4 banks. INE is the LSB and INF is the MSB.

**APPLICATION NOTES****1. EOM (End Of Message) Flag**

The EOM flag consists of six consecutive bytes of "AA", or "10101010" in binary format. After a trigger signal is received, the VP-1608 uses the internal 8MHz system clock to scan through memory space and finds the correct message by counting the number of EOM flags. For example, to find the 5th message, it must scan through each and every memory location until it finds 4 EOM flags. The first byte following the 4th EOM flag is the first byte of the 5th message.

**2. Creating Master EPROM File on the VP-880 System**

Follow these steps to create the master EPROM file:

1. To maximize the EPROM usage, arrange your sound segments in banks of 16 or less, so that the total combined length for each bank is about the same. Do not mix channel A and channel B together.
2. Based on the total combined length of the largest bank, select a highest sampling rate that will fully utilize the EPROM. Use the following equation:

**OSC1, OSC2:**

Internal oscillator pins for external RC components. If external clock source is to be used, feed it through the OSC2 pin. Note that both channels share the same clock, so their sampling rate must be the same.

**RESET1:**

Reset input for channel A, active low. On the falling edge of this reset signal, channel A playback is stopped and all internal counters for channel A are cleared.

**RESET2:**

Reset input for channel B, active low. On the falling edge of this reset signal, channel B playback is stopped and all internal counters for channel B are cleared.

**SCK, TEST:**

For factory use only, do not make any connection.

**SE, SF:**

Output for EPROM bank select. These two pins are actually latched outputs for INE and INF.

**VDD:**

Input, supply voltage.

**VDS & VAS:**

VDS is digital ground and VAS is analog ground. Connect the two grounds together close to the power source to minimize noise.

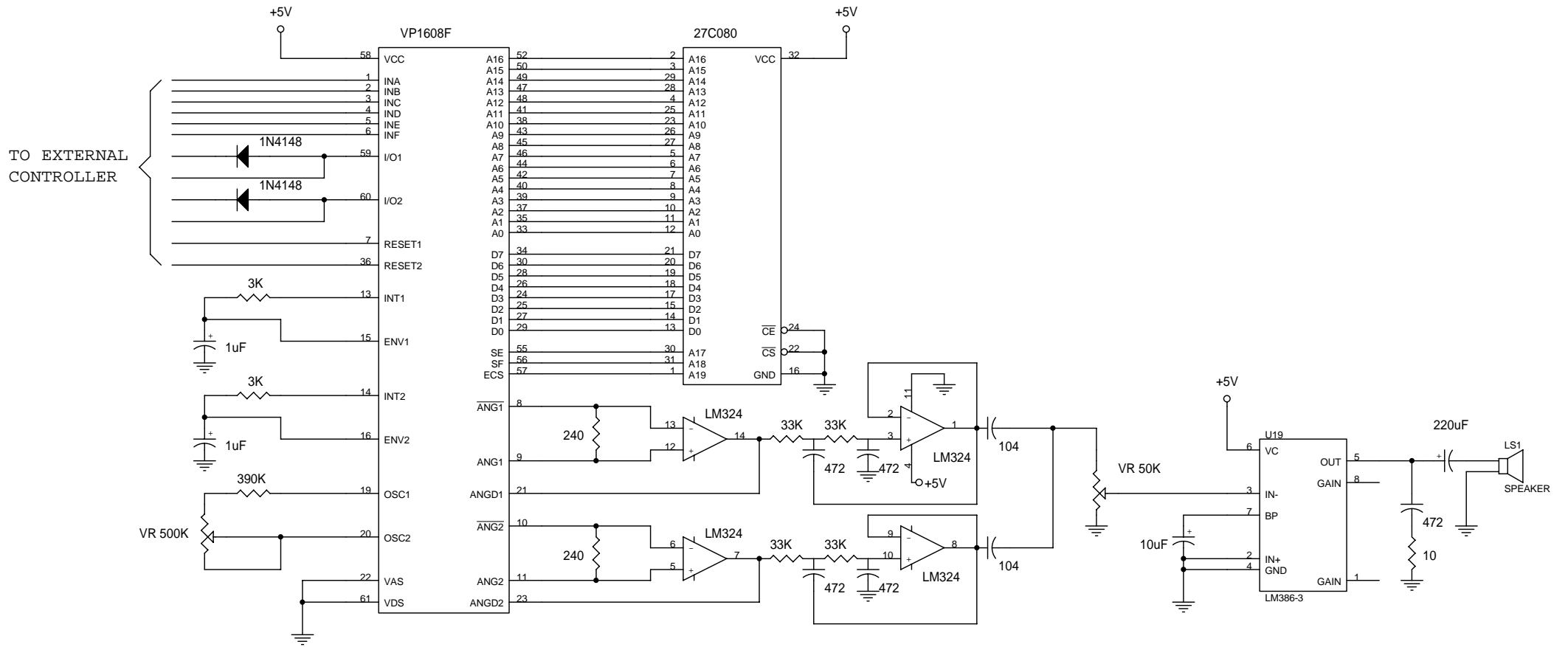
$$\text{Sampling Rate (Kbps)} = \frac{\text{EPROM Size (K-bits)}}{\text{Total Length (Second)}}$$

3. Digitize and edit each segment as a separate file. Use the "ROM Data Management" function to combine up to 16 messages into a "bank file". The first filename entered in the "ROM Data Management" is the first segment in that bank, and etc.

4. Depending on the hardware design, each EPROM chip may contain one or more sound banks. It is also possible to use just one EPROM to store all sound segments of both channel A and channel B. If you need to combine several bank files into one for programming into one EPROM chip, use the following DOS command:

```
COPY /b file_1+file_2+..+file_n destination_file
```

Do not use the "ROM Data Management" function to combine bank files, otherwise each bank file will be considered as a single message file.



TO EXTERNAL  
CONTROLLER

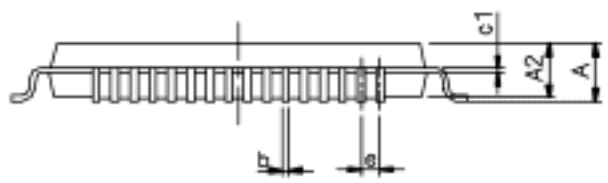
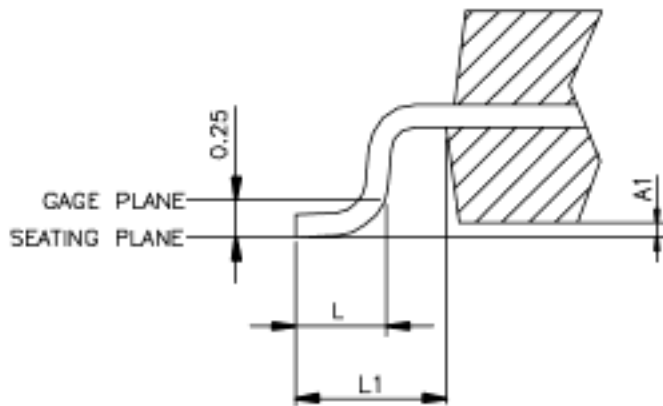
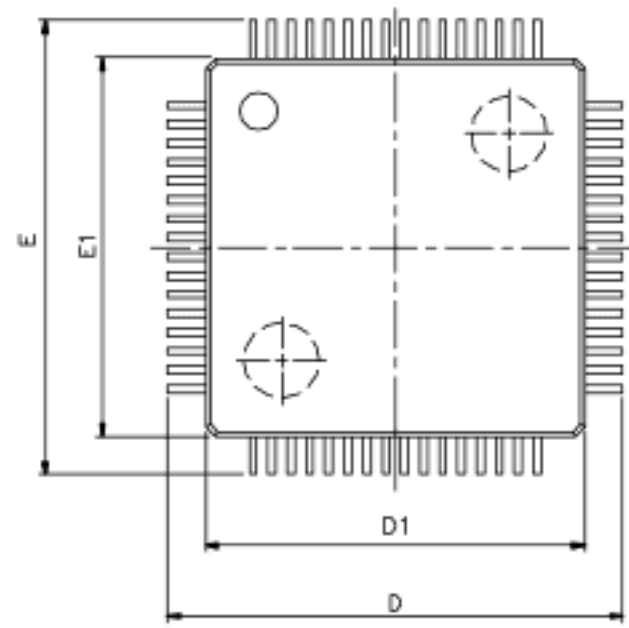
VR 500K

VR 50K

LS1  
SPEAKER

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
E	12.00 BSC	
E1	10.00 BSC	
e	0.50 BSC	
L	0.45	0.75
L1	1.00 REF	



- NOTES:
1. JEDEC OUTLINE: MS-026 BCD
  2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.