P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
-30V	2.5Ω	-1.5A	VP0300L

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

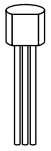
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor controls
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Package Options



TO-92

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	-0.32A	-0.87A	1.0W	170	125

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-30			V	V_{GS}= 0V, I_D =-10µA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-1.8	-4.5	V	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage			-100	nA	V_{GS} = ±30V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			-10	µA	V_{GS} = 0V, V_{DS} = -25V
				-500		V_{GS} = 0V, V_{DS} = -25V T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	-1.5	-1.7		A	V_{GS} = -12V, V_{DS} = -10V
$R_{DS(ON)}$	Static Drain-to-SourceON-State Resistance			2.5	Ω	V_{GS} = -12V, I_D = -1A
G_{FS}	Forward Transconductance	200			m℧	V_{DS} = -10V, I_D = -0.5A
C_{ISS}	Input Capacitance			150	pF	V_{GS} = 0V, V_{DS} = -15V f = 1MHz
C_{OSS}	Common Source Output Capacitance			120		
C_{RSS}	Reverse Transfer Capacitance			60		
$t_{(ON)}$	Turn-ON Time			30	ns	V_{DD} = -25V, I_D = -1A R_{GEN} = 25Ω
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop		-1.2		V	V_{GS} = 0V, I_{SD} = -1.5A

Notes
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit