



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package			
			TO-39	TO-92	TO-220	DICE
-350V	25Ω	-0.4A	VP0635N2	VP0635N3	VP0635N5	VP0635ND
-400V	25Ω	-0.4A	VP0640N2	VP0640N3	VP0640N5	VP0640ND

Features

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

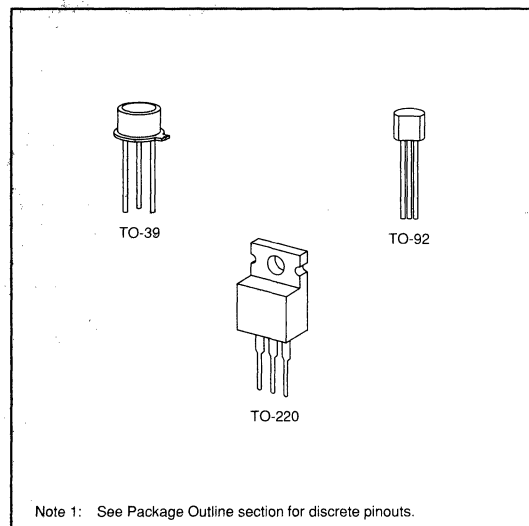
9

Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jC} $^\circ\text{C/W}$	θ_{jA} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-92	-0.30A	-0.6A	1W	125	170	-0.30A	-0.6A
TO-39	-0.40A	-0.75A	6W	21	125	-0.40A	-0.75A
TO-220	-0.40A	-0.75A	28W	2.7	70	-0.40A	-0.75A

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

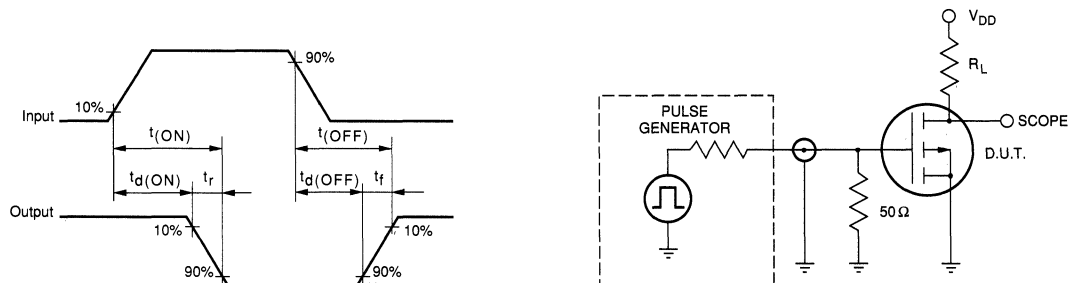
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0640	-400			$V_{GS} = 0, I_D = -2\text{mA}$
		VP0635	-350			
$V_{GS(th)}$	Gate Threshold Voltage	-2		-4	V	$V_{GS} = V_{DS}, I_D = -2\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.8	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -2\text{mA}$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			-10	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				-1	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		-300			$V_{GS} = -5\text{V}, V_{DS} = -25\text{V}$
		-400	-550			$V_{GS} = -10\text{V}, V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		20			$V_{GS} = -5\text{V}, I_D = -100\text{mA}$
			19	25	Ω	$V_{GS} = -10\text{V}, I_D = -100\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/ $^\circ\text{C}$	$V_{GS} = -10\text{V}, I_D = -100\text{mA}$
G_{FS}	Forward Transconductance	100			m \mathcal{S}	$V_{DS} = -25\text{V}, I_D = -100\text{mA}$
C_{ISS}	Input Capacitance		75	130	pF	$V_{GS} = 0, V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		50	75		
C_{RSS}	Reverse Transfer Capacitance		10	20		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = -25\text{V}$ $I_D = -100\text{mA}$ $R_S = 50\Omega$
t_r	Rise Time			10		
$t_{d(OFF)}$	Turn-OFF Delay Time			20		
t_f	Fall Time			10		
V_{SD}	Diode Forward Voltage Drop			1.8		
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0, I_{SD} = -100\text{mA}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

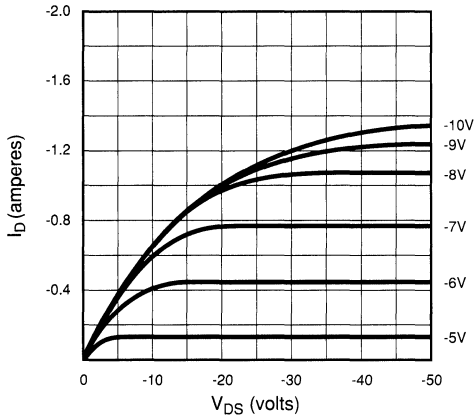
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

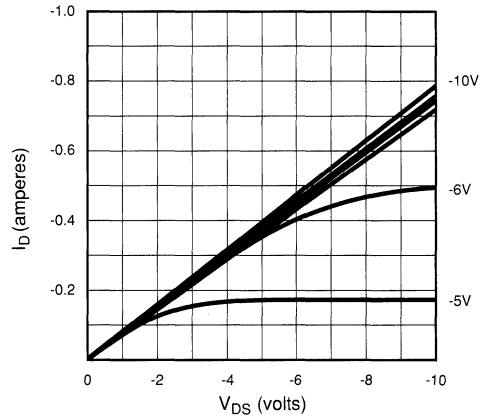


Typical Performance Curves

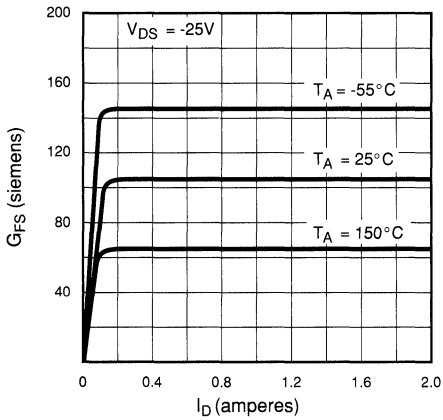
Output Characteristics



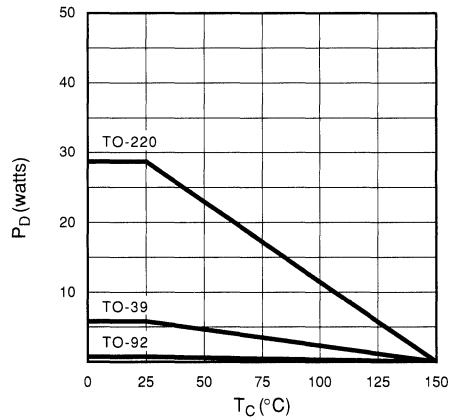
Saturation Characteristics



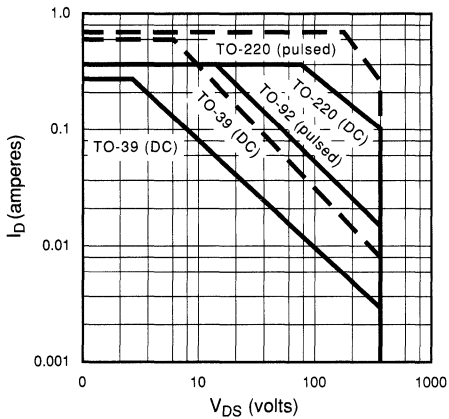
Transconductance vs. Drain Current



Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics

