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VP101

30/50MHz 8-BIT CMOS VIDEO DAC

The VP101 is a CMOS 8-bit video DAC designed for use in high performance, high resolution colour graphics applications.

The device uses video control inputs ($\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ and REF WHITE) to provide the VP101 with the video pedestal levels required to generate RS-343A compatible video signals into a doubly-terminated 75Ω load, or alternatively to produce RS-170 video signals across a singly-terminated 75Ω load.

Data and control inputs are fully pipelined to maintain synchronisation between the DAC outputs.

The full scale output current is defined by a 1.2V reference and a single resistor. The reference voltage is included on-chip in the VP101, but may be supplied externally if required (see Fig. 2).

Differential and integral linearity errors of the D-A converters are guaranteed to be a maximum of ±1LSB over the full operating temperature range.

FEATURES

- 30/50MHz Pipeline Operation
- Triple 8-Bit D-A Converters
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Levels
- Drives Doubly Terminated 75Ω Load
- Single 5V Power Supply
- Typical Power Dissipation 500mW
- Direct Replacement for Bt101
- On-Chip Reference Available

APPLICATIONS

- High Resolution Colour Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

ORDERING INFORMATION

VP101-3 BA DP (Commercial - Plastic DIL Package)
VP101-3 BA HP (Commercial - J-lead Package)
VP101-5 BA DP (Commercial - Plastic DIL Package)
VP101-5 BA HP (Commercial - J-lead Package)
VP101-3 BA GP (Commercial - Plastic Leaded Chip Carrier, Gullwing formed leads)

ABSOLUTE MAXIMIM RATINGS (Referenced to AGND)

DC supply voltage (V_{AA}) -0.3 to +7V
Digital input voltage-0.3 to V_{AA} +0.3V
Analog output short circuit duration Indefinite
Ambient operating temperature 0°C to +70°C
Storage temperature range-55°C to +125°C

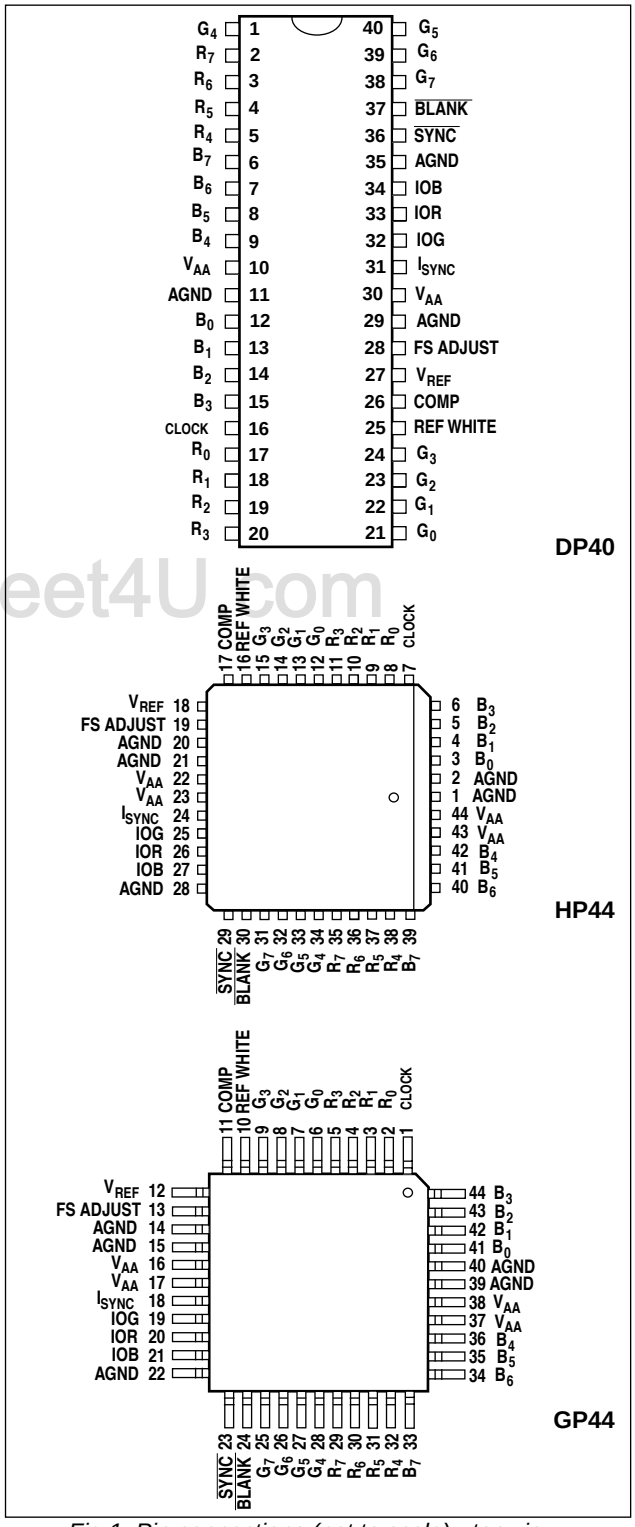


Fig.1 Pin connections (not to scale) - top view

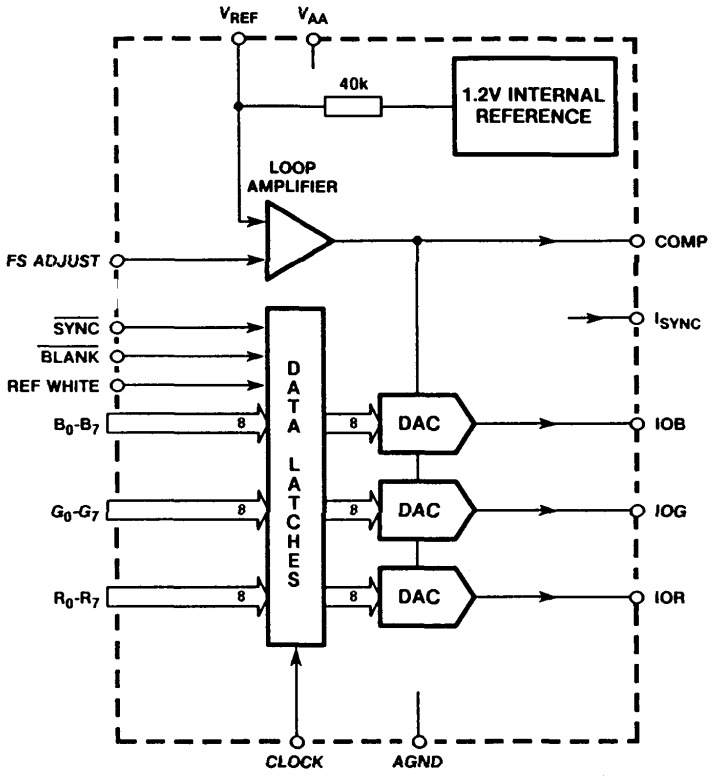


Fig.2 functional block diagram of VP101

RECOMENDED OPERATING CONDITIONS

Parameter	Symbol	Value Min.	Typ.	Max.	Units	Conditions
Supply voltage	V_{AA}	4.75	5.00	5.25	V	
Ambient operating temperature	T_{amb}	0		+70	°C	
Output load	R_L		37.5		Ω	for RS-343A compatible output levels
Reference voltage (internal or external)	V_{REF}	1.14	1.20	1.26	V	
FS ADJUST resistor	R_{SET}		542		Ω	

THERMAL CHARACTERISTICS

	DP	HP	GP	
Thermal resistance, chip-to-case θ_{jc} =	12	17	17	°C/W
Thermal resistance, chip-to-ambient θ_{jc} =	45	50	50	°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in recommended operating conditions.

DC CHARACTERISTICS

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution (each DAC)		8			Bits	
Accuracy (each DAC)						
Integral linearity error	INL		±0.3	±1	LSB	
Differential linearity error	DNL		±0.3	±1	LSB	
Grey scale error			±1%	±5%	% grey scale	
Monotonicity			guaranteed			
Digital inputs						
Input high voltage	V_{IH}	3.0		V_{AA}+0.3	V	binary coding
Input low voltage	V_{IL}	AGND-0.3		1.2	V	
Input high current	I_{IH}			+1	µA	
Input low current	I_{IL}			-1	µA	
Analog outputs						
Grey scale current range		15		20	mA	RS-343A tolerances assumed
			255		LSB	
Output currents						
White level relative to blank level		17.69	19.06	20.40	mA	
			276		LSB	
White level relative to black level		16.74	17.62	18.50	mA	
			255		LSB	
Black level relative to blank level		0.95	1.44	1.90	mA	
			21		LSB	
Blank level on IOR, IOB		0	5	50	mA	
			0		LSB	
Blank level on IOG		6.29	7.62	8.96	mA	
			111		LSB	
Sync level on IOG		0	5	50	µA	
					LSB	
LSB size	LSB		69.1		µA	
DAC to DAC matching			2		%	
Output compliance	V_{OC}	-0.5		+1.4	V	
External V_{REF} input current	I_{REF}			10	µA	
Internal voltage reference	V_{REF}	1.14	1.20	1.26	V	
Internal V_{REF} temperature coefficient			40		ppm/°C	

AC CHARACTERISTICS

Parameter	Symbol	VP101-5 Min.	VP101-5 Typ.	VP101-5 Max.	VP101-3 Min.	VP101-3 Typ.	VP101-3 Max.	Units	Conditions
Max clock rate	f_{max}	50			30			MHz	
Data and control setup time	t_{SU}	6			8			ns	
Data and control hold time	t_H	2			2			ns	
Clock cycle time	t_{CYC}	20			33.3			ns	
Clock pulse width high time	t_{CLKH}	8			10			ns	
Clock pulse width low time	t_{CLKL}	8			10			ns	
Analog output delay	t_{DLY}		10			10		ns	
Analog output rise/fall time	t_{VRF}			8			9	ns	
Analog output settling time	t_S		12			15		ns	
Glitch energy			100			100		pV-sec	
Analog output skew			0	3		0	3	ns	
Pipeline delay		1	1	1	1	1	1	Clock	
V_{AA} supply current	I_{AA}		120	175		100	140	mA	at f_{max}, V_{AA} = 5V

CIRCUIT DESCRIPTION

As shown in the Fig. 2, the VP101 contains three 8-bit D-A converters, input latches, and a loop amplifier.

On the rising edge of each clock cycle, (see Fig. 4), 24 bits of colour information (R_0-R_7, G_0-G_7, and B_0-B_7) are latched into the device and presented to the three 8-bit D-A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, and will force the inputs of each D-A converter to $FF.

$\overline{SYNC}$ and $\overline{BLANK}$ are latched on the rising edge of the clock to maintain synchronisation with the colour data. These inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as shown in Fig. 3. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$, and REFWHITE inputs modify the output levels.

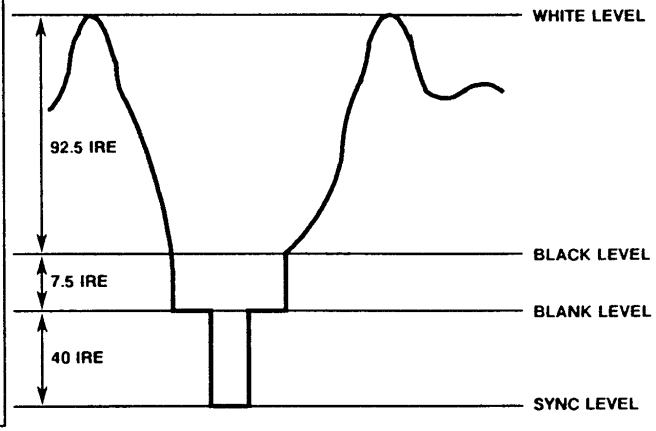
The I_{SYNC} current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If I_{SYNC} is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG and IOB outputs will have the same full scale output current.

Full Scale output current is set by an external resistor (R_{SET}) between the FS ADJUST pin and AGND. R_{SET} has a typical value of 542Ω for generation of RS-343A video into a 37.5Ω load. The VP101 may be used in applications where an external 1.2V (typical) reference is provided, in which case the external reference should be temperature compensated and provide a low impedance output.

The D-A converters on the VP101 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme.This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch energy are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilises the full scale output current against temperature and power supply variations.

The analog outputs of the VP101 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω co-axial cable or interpolation filters.

Red/Blue		Green	
mA	V	mA	V
19.06	0.714	26.68	1.000
1.44	0.054	9.06	0.340
0.00	0.000	7.62	0.286
		0.000	0.000



NOTE: 75Ω doubly terminated load, R_{SET} = 542Ω, V_{REF} = 1.2V, I_{SYNC} connected to IOG, RS-343A levels assumed

Fig.3 Composite video output waveform

Description	IOG (mA)	IOR/IOB (mA)	REF WHITE	$\overline{SYNC}$	$\overline{BLANK}$	DAC I/P Data
White Level	26.68	19.06	1	1	1	$XX
White Level	26.68	19.06	0	1	1	$FF
Data	Data + 9.06	Data + 1.44	0	1	1	Data
Data-Sync	Data + 1.44	Data + 1.44	0	0	1	Data
Blank Level	9.06	1.44	0	1	1	$00
Blank-Sync	1.44	1.44	0	0	1	$00
Blank Level	7.62	0	X	1	0	$XX
Sync Level	0	0	X	0	0	$XX

NOTE: Typical with full scale IOG = 26.68mA, R_{SET} = 542Ω, V_{REF} = 1.2V, I_{SYNC} connected to IOG

Table 1: Video output truth table

Pin name	Description
$\overline{BLANK}$	Composite blank control input. A logic '0' forces the IOR, IOG and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When $\overline{BLANK}$ is a logic zero, the R_0-R_7, G_0-G_7, B_0-B_7, and REF WHITE inputs are ignored.
$\overline{SYNC}$	Composite sync control input. A logic '0' on this input switches off a 40 IRE current source on the I_{SYNC} output. $\overline{SYNC}$ does not override any other control or data input as shown in Table 1; therefore it should be asserted only during the blanking interval. It is latched to the rising edge of CLOCK.
REF WHITE	Reference white level control input. A logic '1' on this input forces the IOR, IOG and IOB outputs to the white level, regardless of the R_0-R_7, G_0-G_7 and B_0-B_7 inputs. It is latched on the rising edge of CLOCK. See table 1.
R_0-R_7 G_0-G_7 B_0-B_7	Red, Green, and Blue data inputs. R_0, G_0, and B_0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input. The rising edge of CLOCK latches the R_0-R_7, G_0-G_7 and B_0-B_7 $\overline{SYNC}$, $\overline{BLANK}$, and REFWHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated CMOS buffer.
IOR,IOG, IOB	Red, Green, and Blue current outputs. these high impedance current sources are capable of directly driving a doubly terminated 75Ω co-axial cable. All outputs, whether used or not, should have the same output load (Note: A DC path to ground must be maintained).
I_{SYNC}	Sync current output. Typically this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logic '0' on the $\overline{SYNC}$ input results in no current being output to this pin, while logic '1' results in the following current being output: $I_{SYNC}\ (mA) = 3468 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 111\ LSBs$ If sync information is not required on the green channel, this output may be connected to V_{AA} and the $\overline{SYNC}$ input tied high, causing the I_{SYNC} current source to be turned off, reducing the power consumption.
FS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and AGND controls the magnitude of the full video signal (Fig. 3). The current flowing in the R_{SET} resistor is equal to 32 LSBs. note that the IRE relationships in Fig. 3 are maintained, regardless of the full scale output current. The relationship between R_{SET} and full scale current on IOG (assuming I_{SYNC} is connected to IOG) is: $IOG\ (mA) = 12082 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 387\ LSBs$ The full scale output current on IOR, IOB (mA) for a given R_{SET} is defined as: $IOR, IOB\ (mA) = 8624 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 276\ LSBs$
COMP	Compensation pin. This pin provides compensation for the internal loop amplifier. A 0.01µF ceramic capacitor must be connected between this pin and the nearest V_{AA} pin. Connecting the capacitor to V_{AA} rather than to the AGND provides the highest possible power supply noise rejection.
V_{REF}	Voltage reference output. The output from an internal reference circuit, providing 1.2V (typical) reference.A 0.1µF ceramic capacitor must be used to decouple this output to V_{AA}.
AGND	Analog ground. All AGND pins must be connected.
V_{AA}	Analog power. All V_{AA} pins must be connected.

APPLICATION NOTES

RS-343A and RS-170 Video Generation

For generation of RS-343A compatible video levels it is recommended that a doubly terminated 75Ω load be used with an R_{SET} resistor value of approximately 542Ω

Similarly for generation of RS-170-compatible video, it is recommended that a singly terminated 75Ω load be used with an R_{SET} value of about 774Ω. If the VP101 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads.t

If driving a large capacitive load (load RC >1/20Πf_c) it is recommended that an output buffer with unloaded gain >2 be used to drive a doubly terminated 75Ω load.

COMP Resistor

To optimise the settling time of the VP101, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

Non-Video Applications

The VP101 may be used in non-video applications by disabling the video specific control inputs. REF WHITE should be a logic '0' while $\overline{BLANC}$ and $\overline{SYNC}$ should be a logic '1'. I_{SYNC} should be connected to V_{AA} or AGND. All three outputs will have the same full scale output current.

The relationship between R_{SET} and full scale output current (I_{OUT}) in this configuration is as follows:

$$I_{out}\ (mA) = 7968 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 255\ LSBs$$

$$\text{Note that } 1\ LSB \equiv \frac{V_{REF}\ (V)}{32 \times R_{SET}\ (\Omega)}$$

With the data inputs at $00, there is a DC offset current (I_{min}) defined as follows:

$$I_{min}\ (mA) = 656 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 21\ LSBs$$

Therefore the total full scale output current will be I_{OUT} + I_{min}. The REF WHITE input may optionally be used as a 'force to full scale' control.

TIMING WAVEFORMS

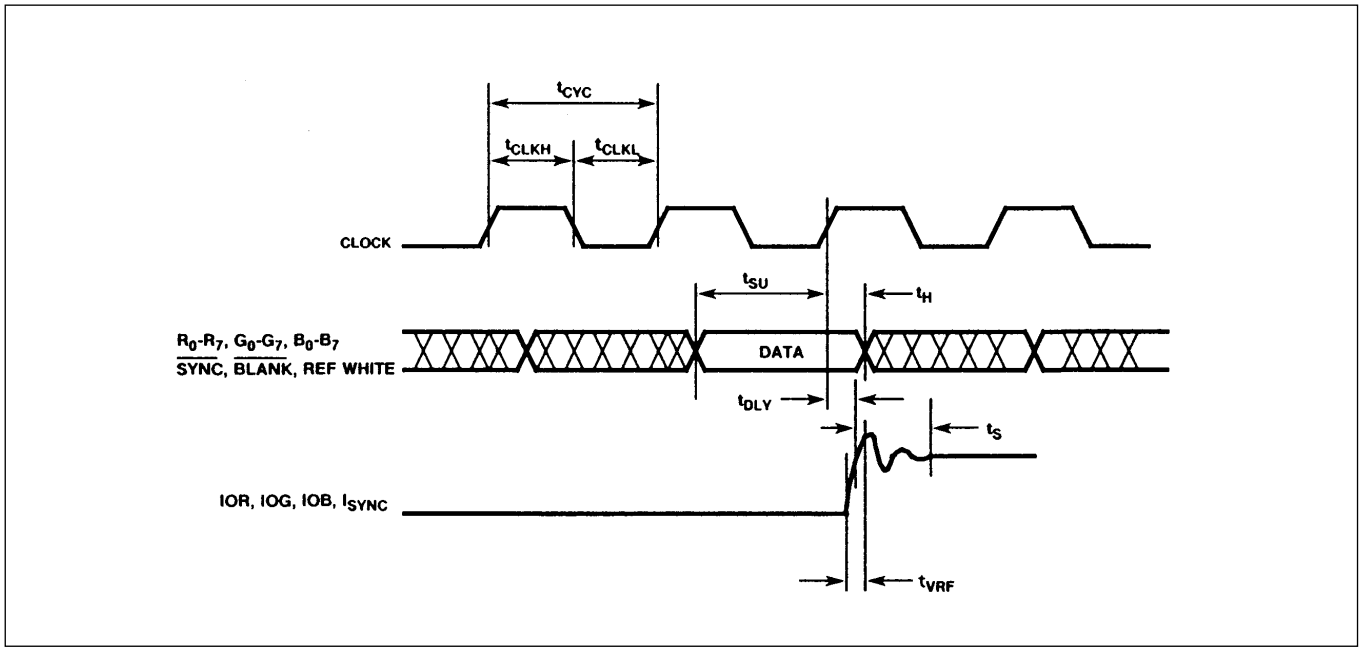


Fig.4 Input/output timing

NOTES
1. Output delay, t_{DLY}, measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
2. Settling time, t_s, measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.
3. Output rise/fall time, t_{VRF}, measured between the 10% and 90% points of full scale transition.

PCB LAYOUT CONSIDERATIONS

To obtain the optimum performance from the VP101 great care must be taken in the PCB layout to ensure low noise power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling.

Power and Ground Planes

The VP101 and its associated circuitry should have its own power/ground planes connected at a single point through a ferrite bead. It is important that the regular PCB and ground planes do not overlay any portions of the analog power or ground planes to minimise plane-to-plane noise coupling.

Digital Signal Interconnect

The digital signal lines to the VP101 should be isolated as much as possible from the analog circuitry. Due to the high clock rates used, the clock lines to the VP101 should be as short as possible to minimise noise pickup.

Any pull-up resistors used on the inputs should be connected to the regular PCB power plane, not to the analog power plane.

Supply Decoupling

Noise on the analog power plane will be further reduced by the use of multiple decoupling capacitors (See Fig. 5).

Optimum performance is obtained with 0.1µF chip ceramic capacitors placed as close as possible to the V_{AA} pins, with the shortest leads possible to reduce lead inductance.

It should be noted that while the loop amplifier circuitry of the VP101 will reject power supply noise, this rejection decreases with frequency. Any high frequency noise on the regular supply (such as produced by a switch mode power supplies) must be adequately suppressed, else the designer should consider using a three terminal regulator to supply the analog power plane.

Analog Signal Interconnect

For optimum performance the analog output connectors and source termination resistors should be as close as possible to the VP101 to minimise noise pickup and reflections due to impedance mismatch. The video out signals should overlay the ground plane and not the analog power plane, to maximise the high frequency power supply rejection.

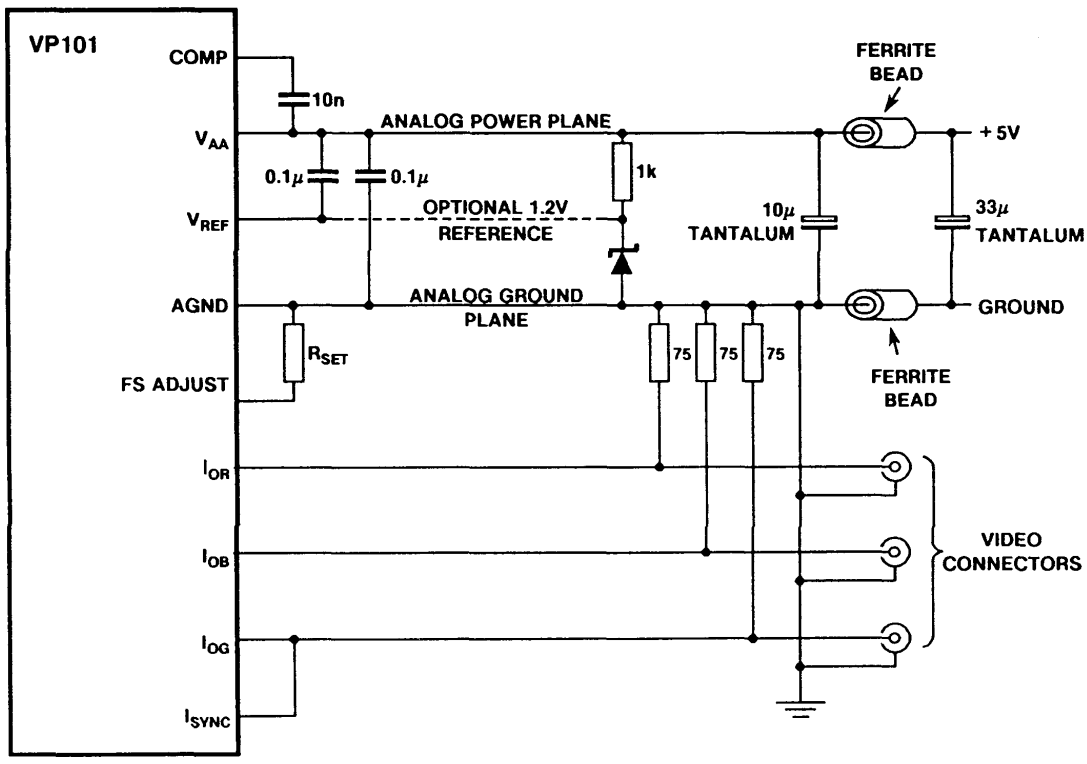


Fig.5 VP101 typical connections

VP101

GEC PLESSEY
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HEADQUARTERS OPERATIONS
GEC PLESSEY SEMICONDUCTORS
Cheney Manor, Swindon,
Wiltshire SN2 2QW, United Kingdom.
Tel: (01793) 518000
Fax: (01793) 518411

GEC PLESSEY SEMICONDUCTORS
P.O. Box 660017,
1500 Green Hills Road,
Scotts Valley, California 95067-0017,
United States of America.
Tel: (408) 438 2900
Fax: (408) 438 5576

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