# N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

## Ordering Information

| $BV_{DSS}$ / $BV_{DGS}$ | $R_{DS(ON)}$ (max) | $I_{D(ON)}$ (min) | Order Number / Package | |
|---|---|---|---|---|
| | | | 14-Pin P-DIP | 14-Pin C-DIP |
| 60V | 5.5Ω | 0.5A | VQ1000N6 | VQ1000N7 |

## Features

- ☐ Very high input impedance
- ☐ Very high speed
- ☐ Low on-resistance
- ☐ No secondary breakdown
- ☐ High reliability

## Applications

- ☐ Logic to high current interface
- ☐ High speed line driver
- ☐ LED digit strobe driver
- ☐ Linear amplifiers
- ☐ Stepper motor drive

## Absolute Maximum Ratings

| | |
|---|---|
| Drain-to-Source Voltage | $BV_{DSS}$ |
| Drain-to-Gate Voltage | $BV_{DGS}$ |
| Gate-to-Source Voltage | ± 15V |
| Operating and Storage Temperature | -55°C to +150°C |
| Soldering Temperature* | 300°C |

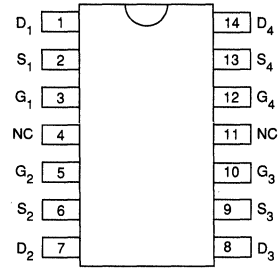
*Distance of 1.6 mm from case for 10 seconds.

## Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Pin Configuration




top view

14-pin DIP

# Thermal Characteristics (@ $T_A$ = 25°C)

| Test | Unit | Each Transistor | All four Transistors |
|---|---|---|---|
| | | | VQ1000N7 |
| Total Power Dissipation | Watts | 1.30 | 2.0 |
| Linear Derating Factor | mW/ °C | 10.5 | 16 |
| Thermal Resistance | °C/W | 96 | 62.5 |
| Thermal Coupling Factor (K) | | | |
| $Q_1$ - $Q_4$ or $Q_2$ - $Q_3$ | % | 60 | |
| $Q_1$ - $Q_2$, $Q_3$ - $Q_4$, $Q_1$ - $Q_3$ or $Q_4$ - $Q_2$ | % | 50 | |
| Continuous Drain Current [2,3] | A | 0.225 | — |
| Pulsed Drain Current [1,3] | A | 1.0 | — |

Note 1: All D.C. parameter 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs, 2% duty cycle.)
Note 2: $I_D$ (continuous) is limited by max rated $T_j$.
Note 3: $T_C$ = 25°C.

# Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 60 | | | V | $V_{GS}$ = 0, $I_D$ = 100µA |
| $V_{GS(th)}$ | Gate Threshold Voltage | 0.8 | | 2.5 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = 1.0mA |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with Temperature | | -3.0 | -5.0 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = 1.0mA |
| $I_{GSS}$ | Gate Body Leakage | | | 100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0 |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | | 10 | µA | $V_{GS}$ = 0, $V_{DS}$ = Max Rating |
| | | | | 500 | | $V_{GS}$ = 0, $V_{DS}$ = 0.8 Max Rating, $T_A$ = 125°C |
| $I_{D(ON)}$ | ON-State Drain Current | 0.2 | | | A | $V_{GS}$ = 5V, $V_{DS}$ = 25V |
| | | 0.5 | | | | $V_{GS}$ = 10V, $V_{DS}$ = 25V |
| $R_{DS(ON)}$ | Static Drain-to-Source ON-State Resistance | | | 7.5 | Ω | $V_{GS}$ = 5V, $I_D$ = 0.2A |
| | | | | 5.5 | | $V_{GS}$ = 10V, $I_D$ = 0.3A |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with Temperature | | 0.6 | 1.1 | %/°C | $V_{GS}$ = 10V, $I_D$ = 0.3A |
| $G_{FS}$ | Forward Transconductance | 100 | | | m℧ | $V_{DS}$ = 15V, $I_D$ = 0.5A |
| $C_{ISS}$ | Input Capacitance | | | 60 | pF | $V_{GS}$ = 0, $V_{DS}$ = 25V, f = 1 MHz |
| $C_{OSS}$ | Common Source Output Capacitance | | | 25 | | |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 5 | | |
| $t_{d(ON)}$ | Turn-ON Delay Time | | | 5 | ns | $V_{DD}$ = 15V, $I_D$ = 0.6A, $R_S$ = 50Ω |
| $t_r$ | Rise Time | | | 5 | | |
| $t_{d(OFF)}$ | Turn-OFF Delay Time | | | 5 | | |
| $t_f$ | Fall Time | | | 5 | | |
| $V_{SD}$ | Diode Forward Voltage Drop | | -0.85 | | V | $V_{GS}$ = 0, $I_{SD}$ = 0.5A |
| $t_{rr}$ | Reverse Recovery Time | | 165 | | ns | $V_{GS}$ = 0, $I_{SD}$ = 0.3A |

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

# Thermal Coupling and Effective Thermal Resistance

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

$$\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4} \quad (1)$$

where $\Delta T_{J1}$ is the change injunction temperature of die 1.

$R_{\theta 1}$ thru 4 is the thermal resistance of die 1 through 4.

$P_{D1}$ thru 4 is the power dissipated in die 1 through 4.

$K_{\theta 2}$ thru 4 is the thermal coupling between die 1 and die 2 through 4.

An effective package thermal resistance can be defined as follows:

$$R_{\theta (EFF)} = \Delta T_{J1}/P_{DT} \quad (2)$$

where $P_{DT}$ is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to:

$$\Delta T_{J1} = R_{\theta 1}(P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4}) \quad (3)$$

For conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$, $P_{DT} = 4P_D$, equation (3) can be further simplifed and, by substituting into equation (2), results in:

$$R\theta_{(EFF)} = R_{\theta 1}\,(1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4})/4 \quad (4)$$

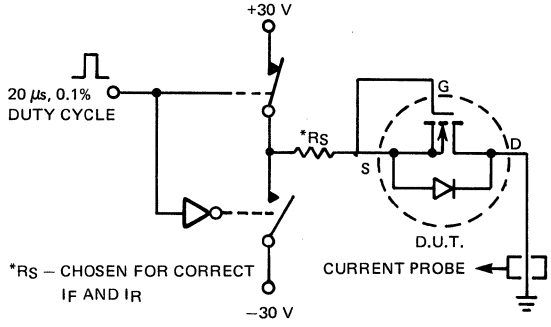
Values for the coupling factors when the ambient is used as a reference are given in the previous table. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest position junction temperatures will result.

# Drain-Source Diode ($t_{rr}$ - Reverse Recovery Time)

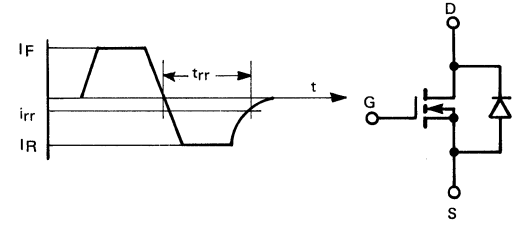
The internal drain-source diodes of DMOS Power FETs may be used as catch diodes or free-wheeling diodes. Current ratings for these diodes are the same as the contnuous and peak drain current ratings for the DMOS FET.

Reverse recovery time is measured using the circuit below. Forward and reverse current $I_F$ and $I_R$ are equal and are tested at the continuous and peak current ratings of the DMOS FET.

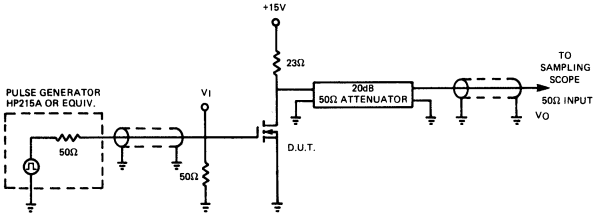
# Switching Waveforms and Test Circuits



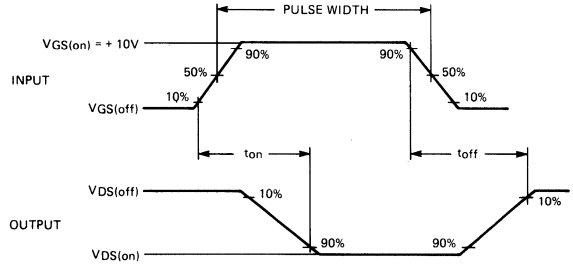

**$T_{RR}$ Test Circuit**




**$T_{RR}$ Test Waveforms**



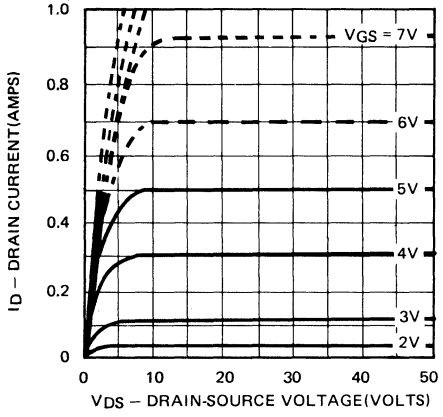

**Switching Time Test Circuit**



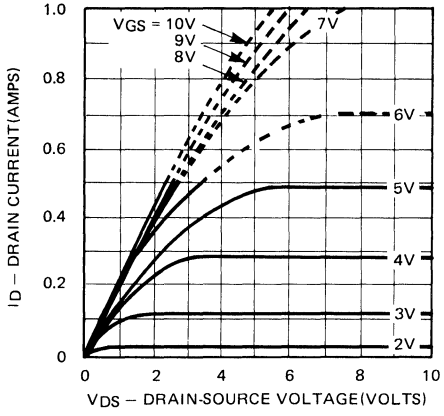

**Switching Time Test Waveform**

# Typical Performance Curves

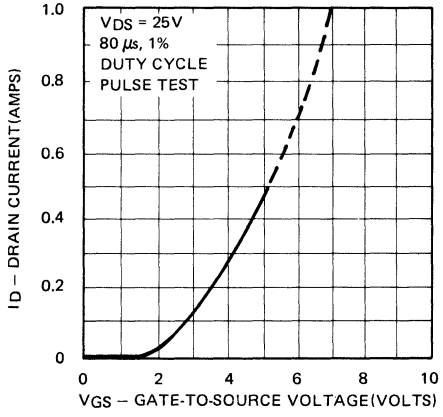
Output Characteristics



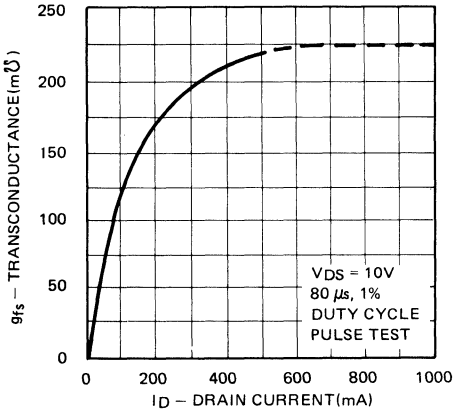

Saturation Characteristics



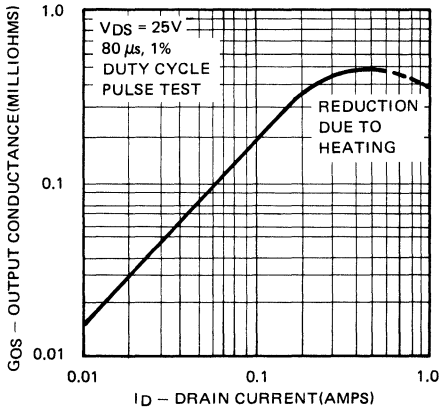

Static
Transfer Characteristics



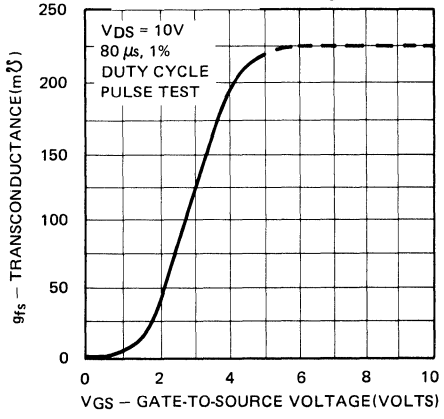

Transconductance vs Drain
Current



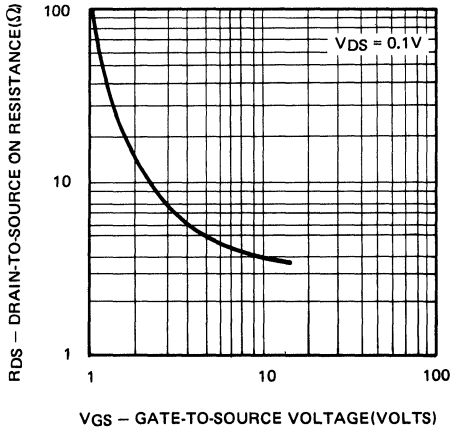

Output Conductance vs
Drain Current




Transconductance vs
Gate-Source Voltage



Drain-to-Source ON Resistance
vs Gate-to-Source Voltage




Capacitance vs Drain-to-Source
Voltage