Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			Quad Ceramic DIP*	Quad Plastic DIP
60V	3.5Ω	1.5A	VQ1004P	VQ1004J

*14-pin side-brazed ceramic DIP.

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

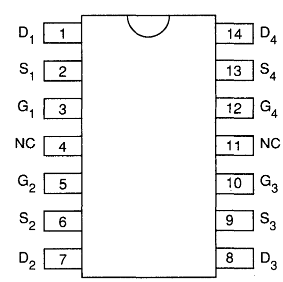
Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view

14-pin DIP

Thermal Characteristics ($T_A = 25°C$)

Test	Unit	Each Transistor		All Four Transistors	
		VQ1004P	VQ1004J	VQ1004P	VQ1004J
Total Power Dissipation	Watts	1.3	1.3	2.0	2.0
Linear Derating Factor	mW/°C	10.4	10.4	16	16
Thermal Resistance	°C/W	96.2	96.2	62.5	62.5
Continuous Drain Current	A	.46	.46		
Pulsed Drain Current	A	2.0	2.0		

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm15V$, $V_{DS} = O$
I_{DSS}	Zero Gate Voltage Drain Current			1	μA	$V_{GS} = O$, V_{DS} = Max Rating
				500		$V_{GS} = O$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	1.5			A	$V_{GS} = 10V$, $V_{DS} \geq 2\ V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
				3.5		$V_{GS} = 10V$, $I_D = 1A$
G_{FS}	Forward Transconductance	170			m℧	$V_{DS} \geq 2V_{DS(ON)}$, $I_D = .5A$
C_{ISS}	Input Capacitance			60	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1MHz
C_{OSS}	Common Source Output Capacitance			50		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 25V$ $I_D = 1A$ $R_S = 50\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.9		V	$V_{GS} = 0$, $I_{SD} = 1A$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit