VQ2000 SERIES

Siliconix incorporated

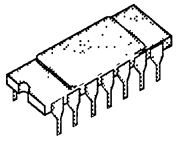
P-Channel Enchancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

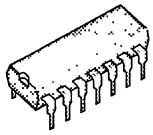
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ2000J	-60	10	-0.24	Plastic
VQ2000P	-60	10	-0.24	Side Braze

Performance Curves: **VPDS06** (See Section 7)

14-PIN DIP
SIDE BRAZE

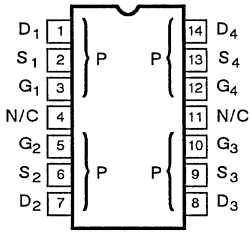


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ2000J	VQ2000P	UNITS
Drain-Source Voltage		V_{DS}	-60	-60	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.24	-0.24	A
	T_A = 100°C		-0.15	-0.15	
Pulsed Drain Current[1]		I_{DM}	±0.8	±0.8	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation – Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ2000J	VQ2000P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VQ2000		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.7	-1	-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
		T_J = 125°C	±5		±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V	-0.02		-1	µA
		T_J = 125°C	-0.2		-200	
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-80	-40		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -25 mA	15		25	Ω
		V_{GS} = -10 V, I_D = -0.25 A	8		10	
		T_J = 125°C	15		20	
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -0.1 A	90	60		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = -10 V, I_D = -0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	15		60	pF
Output Capacitance	C_{oss}		10		25	
Reverse Transfer Capacitance	C_{rss}		3		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		15	ns
	t_r		10		20	
Turn-Off Time	$t_{d(OFF)}$		7		15	
	t_f		8		20	

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.