

## **VR61F1**

# Varistors 0.37A, 0.28A

## **Feature**

- Bi-directional surge can be absorted
- · Low junction capacitance
- · Pb free terminal
- RoHS:Yes

## **OUTLINE**



## **Equivalent circuit**



## **Absolute Maximum Ratings** (unless otherwise specified : TI=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 150	°C
Junction temperature	Tj		-55 to 150	°C
R.M.S. forward current	I <sub>F(R.M.S.)</sub>	50Hz, Sine wave, Resistance load, On alumina substrate, Root mean square value, Ta=25°C *	0.37	Α
R.M.S. forward current	I <sub>F(R.M.S.)</sub>	50Hz, Sine wave, Resistance load, On glass-epoxy substrate, Root mean square value, Ta=25°C *	0.28	А
Surge forward current	I <sub>FSM(R.M.S.)</sub>	50Hz, sine wave, Non-repetitive, 1cycle, Root mean squarevalue, Tj=25°C	7.5	А
Surge forward current	I <sub>FSM</sub>	10/200µs, Non-repetitive, Peak value, Application in single direction, Exponential wave *	60	А
Surge forward current	I <sub>FSM</sub>	0/1000µs, Non-repetitive, Peak value, Application a single direction, Exponential wave *		А

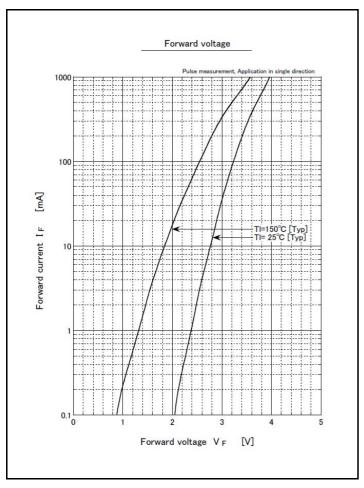
<sup>\* :</sup> See the original Specifications

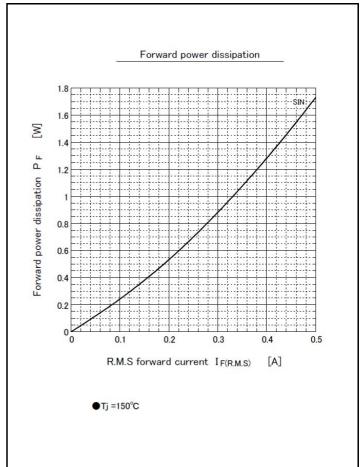
## **Electrical Characteristics** (unless otherwise specified : TI=25°C)

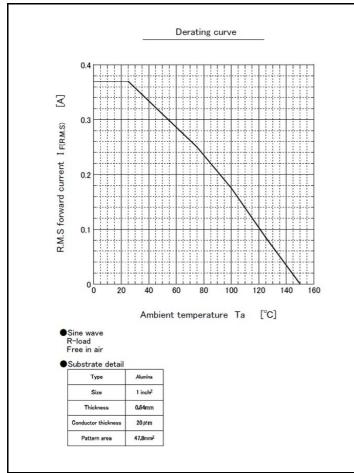
Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	Oilit
Forward voltage	V <sub>F</sub>	IF=1mA, Pulse measurement, Application in single direction	2.05		2.55	V
Forward voltage	V <sub>F</sub>	IF=10mA, Pulse measurement, Application in single direction	2.5		3	V
Forward voltage	V <sub>F</sub>	IF=70mA, Pulse measurement, Application in single direction	2.85		3.35	V
Total capacitance	Ct	f=100kHz, VD=1V, OSC(R.M.S.)=50mVrms, Application in single direction		15		pF
Thermal resistance	Rth(j-a)	Junction to ambient, Application in single direction, on alumina substrate *			108	°C/W
Thermal resistance	Rth(j-a)	Junction to ambient, Application in single direction, on glass-epoxy substrate *			157	°C/W

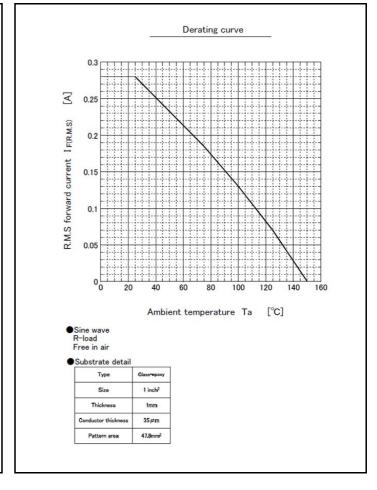
<sup>\* :</sup>See the original Specifications

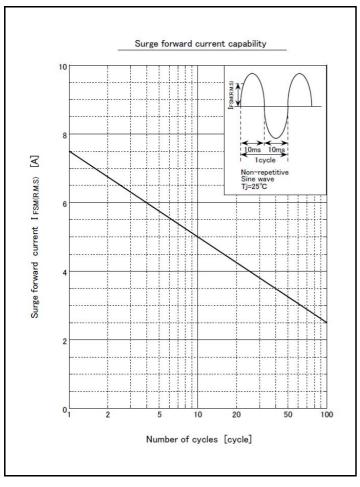
## **CHARACTERISTIC DIAGRAMS**

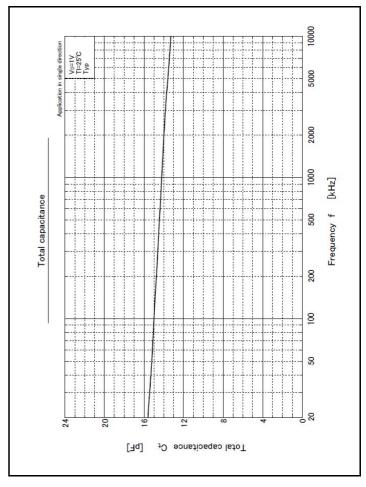


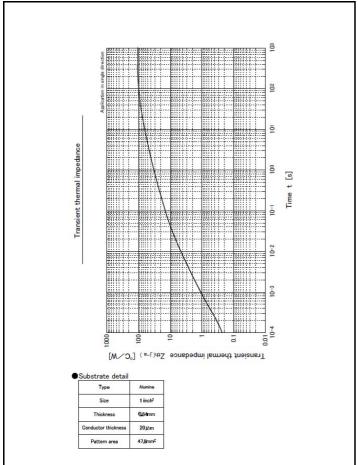


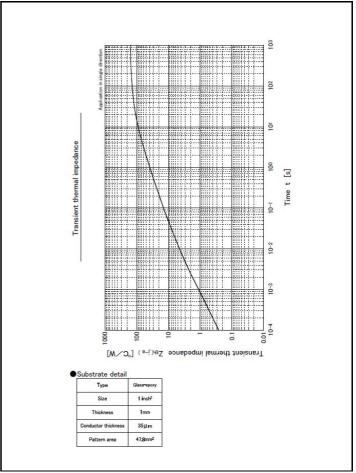








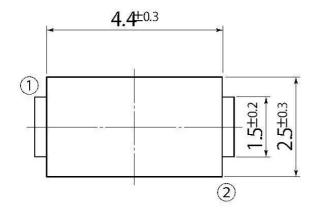


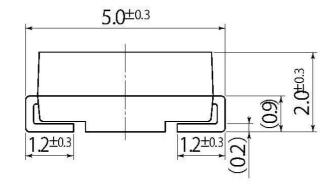


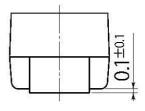
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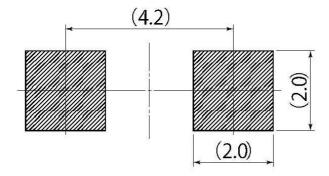
**B4** 

JEDEC Code	DO-214AC		
JEITA Code	_		
House Name	1F		









Referential Soldering Pad

 $\bullet$  Optimize soldering pad to the board design and soldering condition.

#### **Notes**

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