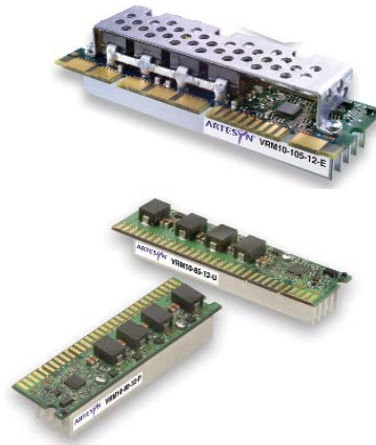


VRM10 Series Single Output

Input Voltage: 12VDC
of Outputs: Single



Special Features

- Designed for use in low profile applications where VRM10.0 or 10.1 specifications are required
- Output current up to 105 A continuous
- Open-collector power good (PWRGD) output
- 6-bit microprocessor voltage identification input (VID)
 - 0.8375 Vdc to 1.6000 Vdc in 12.5mV steps
 - Allows dynamic VID code changes
- Differential remote sense for improved load regulation
- Vertical plug-in to standard motherboard connector
- Selectable output load line impedances, via LL0 and LL1
- Output over-voltage signal (OVP)
- Monotonic output turn-on and turn-off with no overshoot or undershoot
- RoHS compliant
- 2 Year Warranty

Safety

VDE Certificate
No. 2487000-3336-0016

The VRM10 non-isolated DC-DC converters are designed to meet the exceptionally fast transient response requirements of today's microprocessors and fast switching logic in a compact size at a very affordable price. Advanced circuit techniques, component selection and placement optimization, state-of-the-art thermal packaging, and surface-mount technologies provide a high power density, highly reliable, and very precise voltage regulation system for advanced microprocessors.



Specifications

Unless otherwise stated, all specifications are typical at nominal input, maximum continuous rated load at 25 °C and voltages are referenced to Vin-.

OUTPUT SPECIFICATIONS		
Voltage adjustability	(See VID codes, Table 3)	0.8375-1.6000 Vdc
Output current (Iout)		0 A min. 85 A max.
VRM10-85-12-UY	Continuous	85 A max.
	Peak non-sustained	100 A max.
VRM10-80-12-PY	Continuous	80 A max.
	Peak non-sustained	91 A max.
VRM10-105-12-EJ	Continuous	105 A max.
	Peak non-sustained	120 A max.
Load line (LL) adjustability (See LL codes, Table 1)		0.91-1.25 mW
Output voltage (Vout) (Vo sen+ minus Vo sen-) (See Notes 3, B)	Vo max Vo min Vo min Where Rout Iout	VID - Rout * Iout V VID - Rout * Iout - 0.040V (-U/-E) VID - Rout * Iout - 0.038V (-P) VID = programmed voltage (V) Fixed or programmable output impedance (W) Output current (A)
Ripple and noise (See Notes 1, 2)	20 MHz bandwidth	8 mV pk-pk
Short circuit protection		Continuous current limit, brickwall automatic recovery
Remote sensing compensating voltage		Up to 300 mV max.

INPUT SPECIFICATIONS		
Input voltage range	12 Vin nominal	11.0-12.6 Vdc
Input current		
VRM10-85-12-UY	11Vin, VID=1.325 V, Iout=100 A	15.3 A
VRM10-80-12-PY	11Vin, VID=1.400 V, Iout=91 A	14.2 A
VRM10-105-12-EJ	11VIN, VID=1.325V, Iout=120 A	18.5 A
No load	25 0 mA typ.,	300 mA max.
OUTEN OFF		50 mA max.
UVLO turn ON voltage	0 °C <tamb <60 °C	9.5 V ± 2.6%
UVLO turn OFF voltage	0 °C <tamb <60 °C	8.7 V ± 4.5%
Hysteresis		0.8 V typ
Start-up time (using OUTEN)	11.0 V < Vin <12.6 V (PWRGD transitioning high)	10 ms max.

INPUT SPECIFICATIONS CONTD.		
OUTEN, VID and LL signal valid states: ON or Logic '1' OFF or Logic '0'		0.8 Vdc min., 5.5 Vdc max. -0.3 Vdc min., 0.4 Vdc max.

GENERAL CHARACTERISTICS		
Efficiency	See table 2 on page 2	VID = 1.325 V
Switching frequency Fixed (See Note 4)	80 A/85 A 105 A	2.2 MHz 1.1 MHz
Approvals and standards	(See Note 5)	IEC/EN60950 VDE
Material flammability		UL94V-0
Weight	80 A/85 A 105 A	38 g (1.34 oz) 70 g (2.47 oz)
MTBF Telecordia SR-332	80 A/85 A 105 A	2,000,000 hours 1,648,000 hours
Mating connector	80 A/85 A 105 A	See Figure 7 See Figure 8
Connector fingers		Gold plated, 30 μ-inches

ENVIRONMENTAL SPECIFICATIONS		
Temperature shock	Operating non-operating	10 °C/hour 20 °C/hour
Humidity (Non-condensing)	Operating storage	85% RH 95% RH
Altitude	Operating storage	10,000 feet max. 50,000 feet max.
Shock	Operational and non-operational	30 G 11ms Half sine wave
Vibration (See Note 6)	Operational and non-operational	0.02 G ² /Hz max.
Thermal performance (See Note 7)	Operating ambient temperature	0 °C to +60 °C
Storage temperature	(Non-condensing)	-40 °C to + 100 °C

Specifications

INPUT VOLTAGE	OUTPUT VOLTAGE	OVP ⁽⁹⁾	OUTPUT CURRENT	OUTPUT CURRENT	OUTPUT CURRENT	EFFICIENCY (TYP.)	REGULATION LOAD	MODEL NUMBER
			(MIN)	(MAX.) CONTINUOUS	(MAX.) NON-SUSTAINED			
12 Vdc	0.8375-1.6000 Vdc	1.8 V	0 A	80 A	91 A	85%	1.24 mV/A	VRM10-80-12-PY ⁽¹¹⁾
12 Vdc	0.8375-1.6000 Vdc	1.8 V	0 A	85 A	100 A	85%	See Table 1	VRM10-85-12-UY ⁽¹¹⁾
12 Vdc	0.8375-1.6000 Vdc	1.8 V	0 A	105 A	120 A	84%	See table 1	VRM10-105-12-EY ⁽¹¹⁾

MODEL	LL0	LL1	LOAD LINE SLOPE, Rout	UNITS
VRM10-85-12-UY	0	0	1.25	mW
VRM10-85-12-UY	0	1	1.25	mW
VRM10-85-12-UY	1	0	1.25	mW
VRM10-85-12-UY	1	1	Reserved	mW
VRM10-80-12-PY	N/A	N/A	1.24	mW
VRM10-105-12-EJ	0	0	1.25	mW
VRM10-105-12-EJ	0	1	1.25	mW
VRM10-105-12-EJ	1	0	1.25	mW
VRM10-105-12-EJ	1	1	Reserved	mW

Table 1: LL0, LL1 Load Line Codes

EFFICIENCY TABLE	
OUTPUT VOLTAGE	EFFICIENCY (typ.)
VID = 1.325 V @ 85 A	85%
VID = 1.325 V @ 80 A	85%
VID = 1.325 V @ 105 A	84%

Table 2: Efficiency Values

Notes

- Recommended output capacitance, 12 x 560 μ F aluminium polymer and 44 x 10 μ F MLCC for slew rates up to 430 A/ μ s, 14 x 560 μ F aluminum polymer and 45 x 10 μ F MLCC for slew rates up to 930 A/ μ s.
- 8 mV pk-pk ripple. Vin = 12 V, Vout = 1.35 V, Iout = 85 A.
- With the recommended capacitors (See Note 1) across the output, the output voltage stays within the load regulation window for all loads and transient events, up to 100 A for the VRM10-85-12-UY (91 A for the VRM10-80-12-PY) over a 20MHz bandwidth, 0 °C < T_{amb} < 60 °C.
- VRM10 uses a four phase buck topology. Each phase switches at 550 KHz for the VRM10-85-12-UY and VRM10-80-12-PY. This gives an equivalent switching frequency of 2.2 MHz. For the VRM10-105-12-EJ, each phase switches at 275 KHz. This gives an equivalent switching frequency of 1.1 MHz
- Recommended input fusing: one 20 A (or two 10 A in parallel) very fast acting fuse(s). The VRM10 is a high current device. Use appropriate care in handling and installation of this device, which is intended only for use within enclosed equipment.
- 0.01 G²/Hz from 5 Hz to 20 Hz, maintaining 0.02 G²/Hz from 20 Hz to 500 Hz, all axes.
- Maximum current requires adequate forced air over the converter. Please consult Figures 2 and 3 for thermal de-rating.
- When the VRM detects an output over-voltage event, the OVP pin transitions to logic high. This signal can be used to shut down the supply to the VRM, or drive a crowbar device.
- Pins 12 and 51 are not connected on VRM10-80-12-PY. On VRM10-85-12-UY, do not leave these pins floating.
- When included in the users system ESD event shall cause no out-of-regulation conditions.
- The 'Y' suffix indicates that these parts are TSE RoHS 5/6 (non Pb-free) compliant.

Specifications

VOLTAGE IDENTIFICATION (VID) CODES							VOLTAGE IDENTIFICATION (VID) CODES (CONTD.)						
VID4	VID3	VID2	VID1	VID0	VID5	VID (V)	VID4	VID3	VID2	VID1	VID0	VID5	VID (V)
0	1	0	1	0	0	0.8375	1	1	0	1	0	0	1.2125
0	1	0	0	1	1	0.8500	1	1	0	0	1	1	1.2250
0	1	0	0	1	0	0.8625	1	1	0	0	1	0	1.2375
0	1	0	0	0	1	0.8750	1	1	0	0	0	1	1.2500
0	1	0	0	0	0	0.8875	1	1	0	0	0	0	1.2625
0	0	1	1	1	1	0.9000	1	0	1	1	1	1	1.2750
0	0	1	1	1	0	0.9125	1	0	1	1	1	0	1.2875
0	0	1	1	0	1	0.9250	1	0	1	1	0	1	1.3000
0	0	1	1	0	0	0.9375	1	0	1	1	0	0	1.3125
0	0	1	0	1	1	0.9500	1	0	1	0	1	1	1.3250
0	0	1	0	1	0	0.9625	1	0	1	0	1	0	1.3375
0	0	1	0	0	1	0.9750	1	0	1	0	0	1	1.3500
0	0	1	0	0	0	0.9875	1	0	1	0	0	0	1.3625
0	0	0	1	1	1	1.0000	1	0	0	1	1	1	1.3750
0	0	0	1	1	0	1.0125	1	0	0	1	1	0	1.3875
0	0	0	1	0	1	1.0250	1	0	0	1	0	1	1.4000
0	0	0	1	0	0	1.0375	1	0	0	1	0	0	1.4125
0	0	0	0	1	1	1.0500	1	0	0	0	1	1	1.4250
0	0	0	0	1	0	1.0625	1	0	0	0	1	0	1.4375
0	0	0	0	0	1	1.0750	1	0	0	0	0	1	1.4500
0	0	0	0	0	0	1.0875	1	0	0	0	0	0	1.4625
1	1	1	1	1	1	OFF	0	1	1	1	1	1	1.4750
1	1	1	1	1	0	OFF	0	1	1	1	1	0	1.4875
1	1	1	1	0	1	1.1000	0	1	1	1	0	1	1.5000
1	1	1	1	0	0	1.1125	0	1	1	1	0	0	1.5125
1	1	1	0	1	1	1.1250	0	1	1	0	1	1	1.5250
1	1	1	0	1	0	1.1375	0	1	1	0	1	0	1.5375
1	1	1	0	0	1	1.1500	0	1	1	0	0	1	1.5500
1	1	1	0	0	0	1.1625	0	1	1	0	0	0	1.5625
1	1	0	1	1	1	1.1750	0	1	0	1	1	1	1.5750
1	1	0	1	1	0	1.1875	0	1	0	1	1	0	1.5875
1	1	0	1	0	1	1.2000	0	1	0	1	0	1	1.6000

Table 3: Voltage Identification Codes

Specifications

SIGNAL ELECTRICAL INTERFACE						
CHARACTERISTIC - SIGNAL NAME	SYMBOL	MIN	TYP	MAX	UNITS	NOTES AND CONDITIONS
OUTEN - on	$V_{OUTEN(on)}$	0.8		5.5	V	No pull up resistor provided by the VRM
OUTEN - off	$V_{OUTEN(off)}$	-0.3		0.4	V	No pull up resistor provided by the VRM
OUTEN - leakage current		-1		1	μ A	
PWRGD - low	$V_{PWRGD(low)}$			0.4	V	Sink current 4 mA
PWRGD - sink current	$I_{PWRGD(sink)}$			4	mA	Open-collector output to not more than 5.5 V
PWRGD - low threshold		72	74	76	%	Percentage of VID code setting
PWRGD - turn-on response to OUTEN going high	T_{rise}	0	4	10	ms	For waveforms, refer to Application Note 171
VID - high	$V_{ih(VID)}$	0.8		5.5	V	
VID - low	$V_{il(VID)}$	-0.3		0.4	V	
VID - pull up current	$I_{(VID)}$	35	50	65	μ A	
OVP signal trip point	$R_{(VID)}$	1.7		VID + 0.2	V	
OVP drive voltage			1.9 (5.5)	V		$I_{ovp} = -100$ mA ($I_{ovp} = -1$ mA)
LL - high	$V_{ih(LL)}$	0.8		5.5	V	VRM10-85-12-UY only
LL - low	$V_{il(LL)}$	-0.3		0.4	V	VRM10-85-12-UY only
LL - input impedance	$Z_{i(LL)}$	2.18	2.21		k Ω	VRM10-85-12-UY only
VR_Hot# - low	$V_{VR_HOT\#(low)}$	0		0.4	V	Sink current 30 mA. VR_HOT# is pulled as a thermal event is present in the VRM
VR_Hot# - sink current	$I_{VR_HOT\#(sink)}$	0		30mA		Open-collector output to not more than V_{in} . Sinks current as long as thermal event is present in the VRM

ELECTROMAGNETIC COMPATIBILITY						
CHARACTERISTIC - SIGNAL NAME	SYMBOL	MIN	TYP	MAX	UNITS	NOTES AND CONDITIONS
ESD - operating (See Note 10)		15	kV			IEC61000-4-2. In end user equipment
ESD - non-operating				25	kV	IEC61000-4-2. In end user equipment
Radiated emissions		B			Class	FCC and EN55022. In end user equipment
Input characteristics: Input current - operating	I_{IN}		10.7		A	$V_{in} = V_{in}(typ.)$, $I_{out(cont.)} = 85A$, VID = 1.325 V
Input capacitance - external bypass	C_{INext}	680	1000		μ F	

Specifications

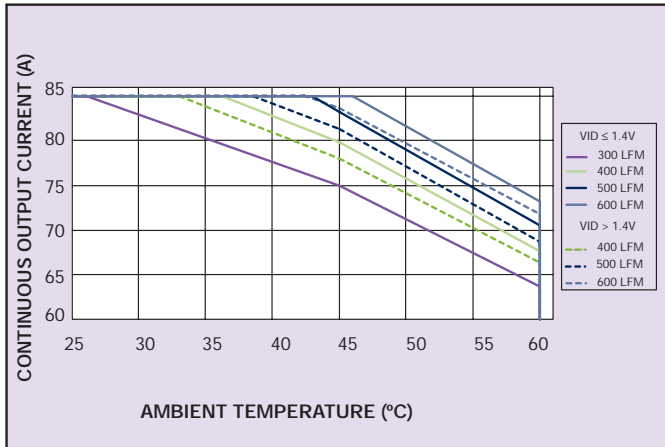


Figure 1: Thermal Derating Curve for VRM10-85-12-UY
(See Note A)

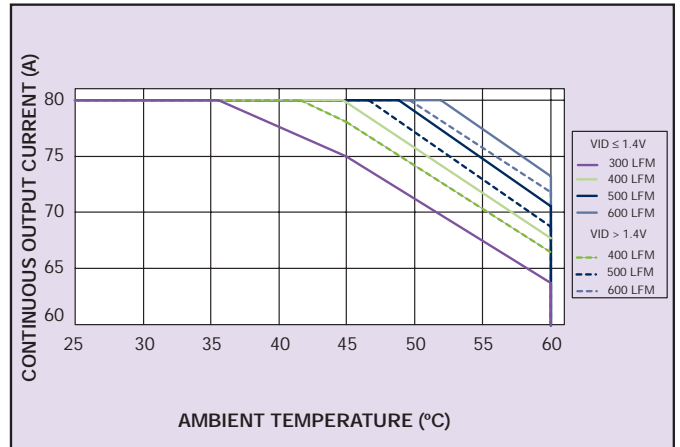


Figure 2: Thermal Derating Curve for VRM10-80-12-PY
(See Note A)

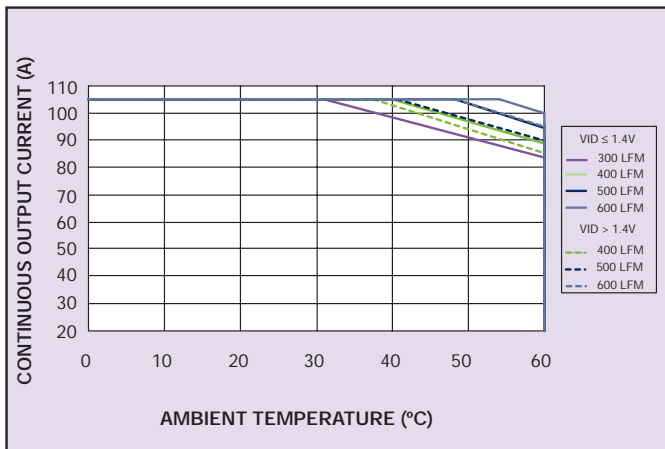


Figure 3: Thermal Derating Curve for VRM10-105-12-EY
(See Note A)

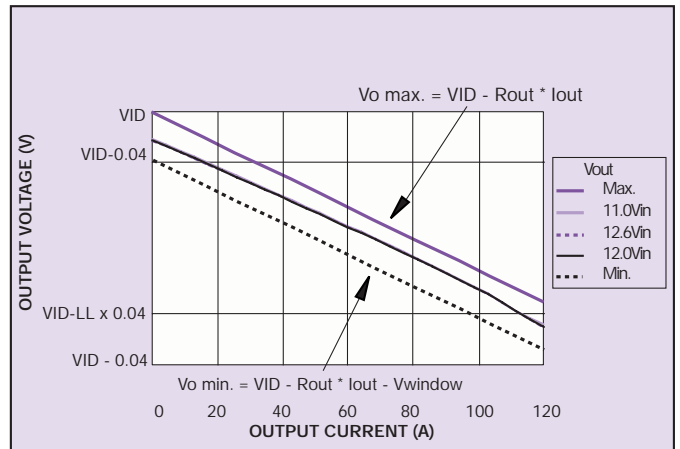


Figure 4: Load Regulation (See Notes 3 and B)

Notes

- A For the LFM and VID conditions graphed, there is no derating between 0 °C and 25 °C.
- B For load regulation equations: VID is in Volts, programmed by the VID bits (refer to Table 3); Rout is in W's, programmed by the LL bits (refer to Table 1); and the output current, Iout is in amps. V_{Window} is 0.040 for VRM10-85-12-UY and 0.038 for VRM10-80-12-PY.
- C Efficiency Vs load plotted is representative of a typical VRM10-85-12-UY with VID = 1.4 V, LL0 = 0, LL1 = 1.
- D Shown for a VRM10-80-12-P with VID = 1.4 V.

Specifications

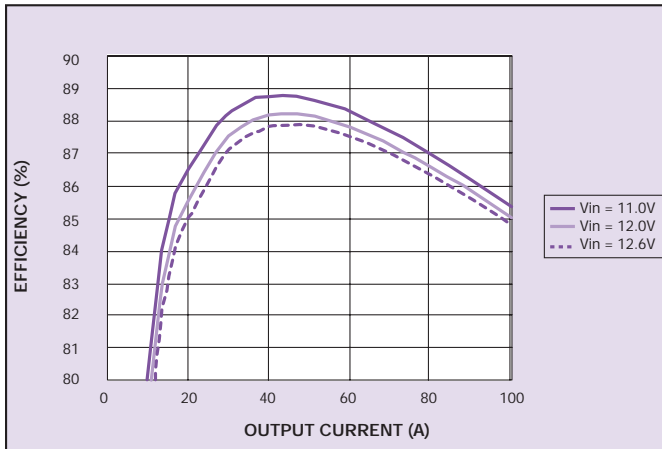


Figure 5: Typical Efficiency Vs Load (See Note C)
For VRM10-85-12-UY and VRM10-80-12-PY

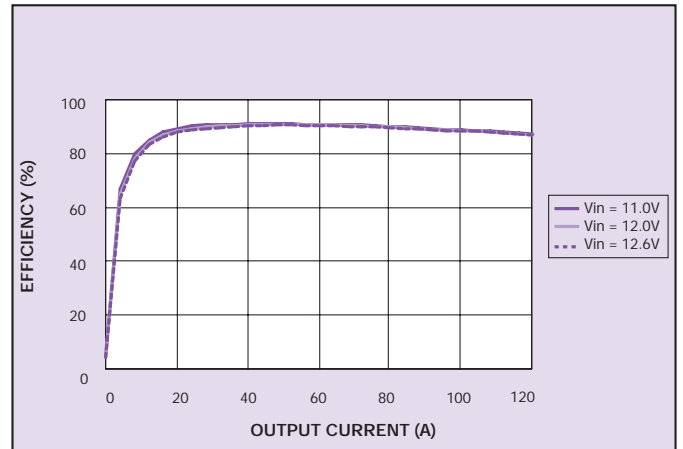


Figure 5a: Typical Efficiency Vs Load (See Note C)
For VRM10-105-12-EJ

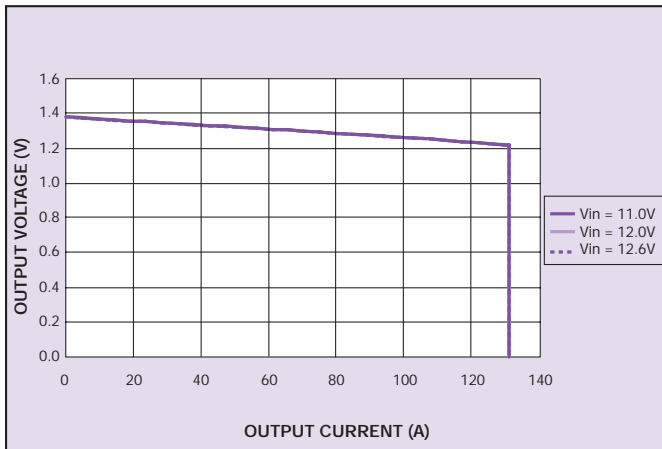
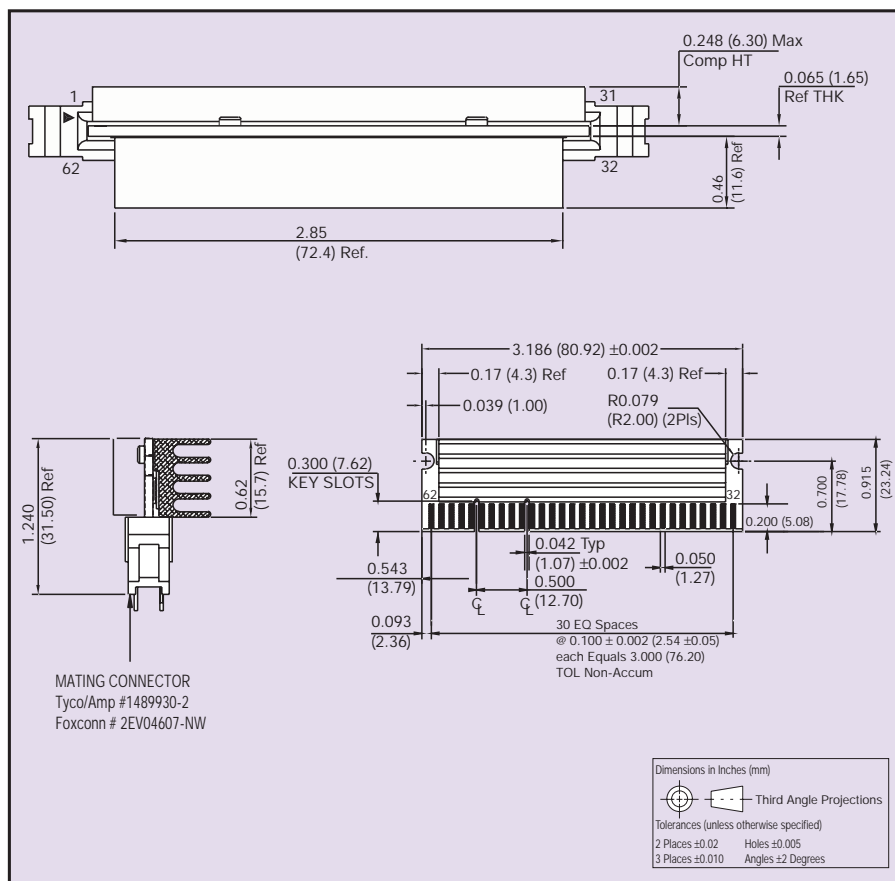


Figure 6: Short Circuit and Over Current Protection (See Note D)
For VRM10-85-12-UY and VRM10-80-12-PY

Specifications

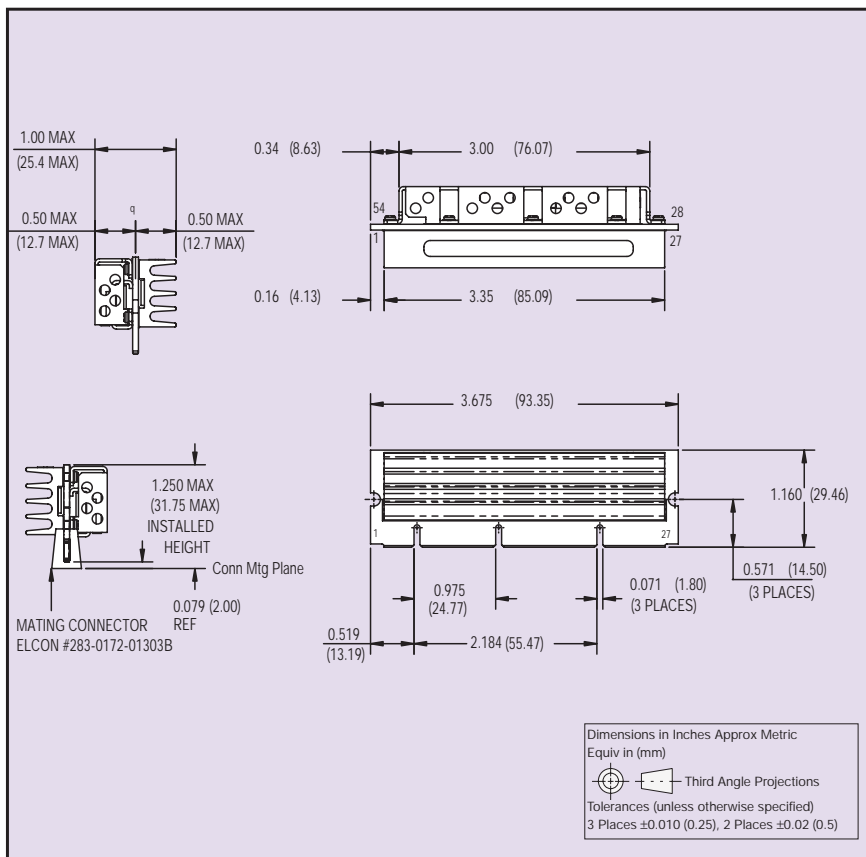
Rev.07.20.07
vrml0 series
8 of 10



PIN CONNECTIONS			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Vin+	62	Vin-
2	Vin+	61	Vin-
3	Vin+	60	Vin-
4	Vin+	59	Vin-
5	N/U	58	VRM_pres#
6	VID4	57	Key
7	VID3	56	VID2
8	VID1	55	VID0
9	OVP	54	VID5
10	PWRGD	53	Outen
11	Vo sen-	52	Vo sen+
12	LL0 ⁽⁹⁾	51	LL1 ⁽⁹⁾
13	Vo-	50	Vo+
14	Vo+	49	Vo+
15	Vo-	48	Vo-
16	Vo+	47	Vo+
17	Vo-	46	Vo-
18	Vo+	45	Vo+
19	Vo-	44	Vo-
20	Vo+	43	Vo+
21	Vo-	42	Vo-
22	Vo+	41	Vo+
23	Vo-	40	Vo-
24	Vo+	39	Vo+
25	Vo-	38	Vo-
26	Vo+	37	Vo+
27	Vo-	36	Vo-
28	Vo+	35	Vo+
29	Vo-	34	Vo-
30	Vo+	33	Vo+
31	Vo-	32	Vo-

Figure 7: 80/85 A Mechanical Drawing and Pinout Table

Specifications



PIN CONNECTIONS			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Vin-	54	Vin+
2	Vin-	53	Vin+
3	Vin-	52	Vin+
4	VID4	51	VID3
5	VID2	50	VID1
6	VID0	49	VID5
7	Vo sen+	48	Vo sen-
8	V _{CC} PWRGD	47	VR_HOT#
9	Outen	46	LL0 ⁽⁹⁾
10	OVP	45	LL1 ⁽⁹⁾
11	NA	44	NA
12	VRM_pres#	43	NA
13	Vo+	42	Vo+
14	Vo+	41	Vo+
15	Vo+	40	Vo+
16	Vo-	39	Vo-
17	Vo-	38	Vo-
18	Vo-	37	Vo-
19	Vo+	36	Vo+
20	Vo+	35	Vo+
21	Vo+	34	Vo+
22	Vo-	33	Vo-
23	Vo-	32	Vo-
24	Vo-	31	Vo-
25	Vo+	30	Vo+
26	Vo+	29	Vo+
27	Vo+	28	Vo+

Figure 8: 105 A Mechanical Drawing and Pinout Table

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