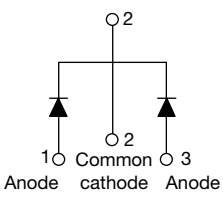
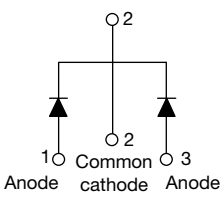
Schottky Rectifier, 2 x 20 A

D²PAK

TO-262



VS-43CTQ...SPbF



VS-43CTQ...-1PbF

FEATURES

- 175 °C T_J operation
- Center tap configuration
- Low forward voltage drop
- High purity, high temperature epoxy encapsulation for enhanced mechanical strength and moisture resistance
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- Halogen-free according to IEC 61249-2-21 definition
- Compliant to RoHS Directive 2002/95/EC
- AEC-Q101 qualified

Pb e3 RoHS COMPLIANT HALOGEN FREE

DESCRIPTION

This center tap Schottky rectifier series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in switching power supplies, freewheeling diodes, and reverse battery protection.

PRODUCT SUMMARY	
$I_{F(AV)}$	2 x 20 A
V_R	80 V/100 V

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	40	A
V_{RRM}		80/100	V
I_{FSM}	t_p = 5 µs sine	850	A
V_F	20 Apk, T_J = 125 °C (per leg)	0.67	V
T_J	Range	- 55 to 175	°C

VOLTAGE RATINGS				
PARAMETER	SYMBOL	VS-43CTQ080SPbF VS-43CTQ080-1PbF	VS-43CTQ100SPbF VS-43CTQ100-1PbF	UNITS
Maximum DC reverse voltage	V_R	80	100	V
Maximum working peak reverse voltage	V_{RWM}			

ABSOLUTE MAXIMUM RATINGS						
PARAMETER		SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current See fig. 5	per leg	$I_{F(AV)}$	50 % duty cycle at T_C = 135 °C, rectangular waveform		20	A
	per device				40	
Maximum peak one cycle non-repetitive surge current per leg See fig. 7		I_{FSM}	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with rated V_{RRM} applied	850	
			10 ms sine or 6 ms rect. pulse		275	
Non-repetitive avalanche energy per leg		E_{AS}	T_J = 25 °C, I_{AS} = 0.50 A, L = 60 mH		7.50	mJ
Repetitive avalanche current per leg		I_{AR}	Current decaying linearly to zero in 1 µs Frequency limited by T_J maximum V_A = 1.5 x V_R typical		0.50	A

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop per leg See fig. 1	V_{FM} (1)	20 A	T_J = 25 °C	0.81	V
		40 A		0.98	
		20 A	T_J = 125 °C	0.67	
		40 A		0.81	
Maximum reverse leakage current per leg See fig. 2	I_{RM} (1)	T_J = 25 °C	V_R = Rated V_R	1	mA
		T_J = 125 °C		11	
Threshold voltage	$V_{F(TO)}$	T_J = T_J maximum		0.71	V
Forward slope resistance	r_t			0.43	mΩ
Maximum junction capacitance per leg	C_T	V_R = 5 V_{DC} (test signal range 100 kHz to 1 MHz), 25 °C		1480	pF
Typical series inductance per leg	L_S	Measured lead to lead 5 mm from package body		8.0	nH
Maximum voltage rate of change	dV/dt	Rated V_R		10 000	V/µs

Note

(1) Pulse width < 300 µs, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS

PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range		T_J, T_{Stg}		- 55 to 175	°C
Maximum thermal resistance, junction to case per leg		R_{thJC}	DC operation	2.0	°C/W
Maximum thermal resistance, junction to case per package				1.0	
Typical thermal resistance, case to heatsink		R_{thCS}	Mounting surface, smooth and greased	0.50	
Approximate weight				2	g
				0.07	oz.
Mounting torque	minimum			6 (5)	kgf · cm (lbf · in)
	maximum			12 (10)	
Marking device			Case style D^2PAK	43CTQ080S	
				43CTQ100S	
			Case style TO-262	43CTQ080-1	
				43CTQ100-1	

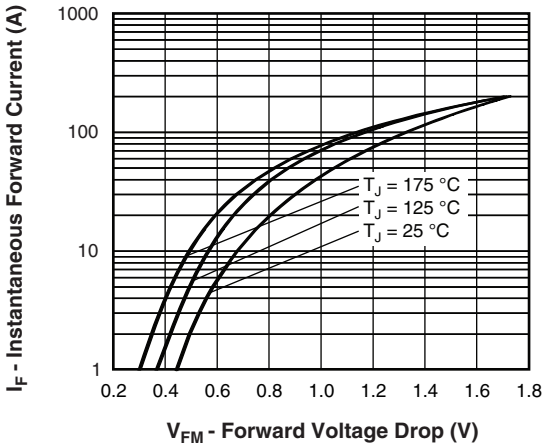


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

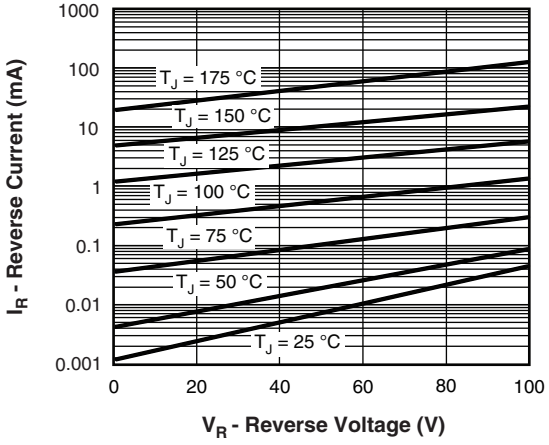


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

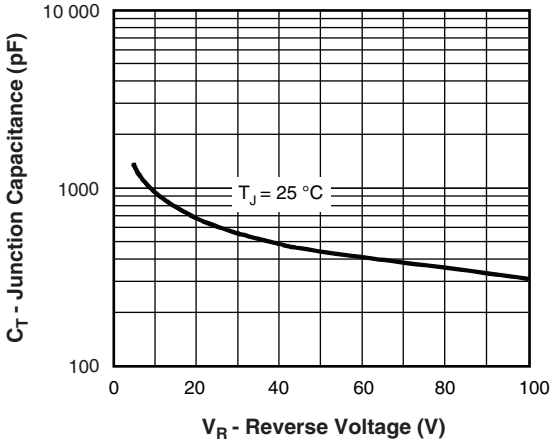


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

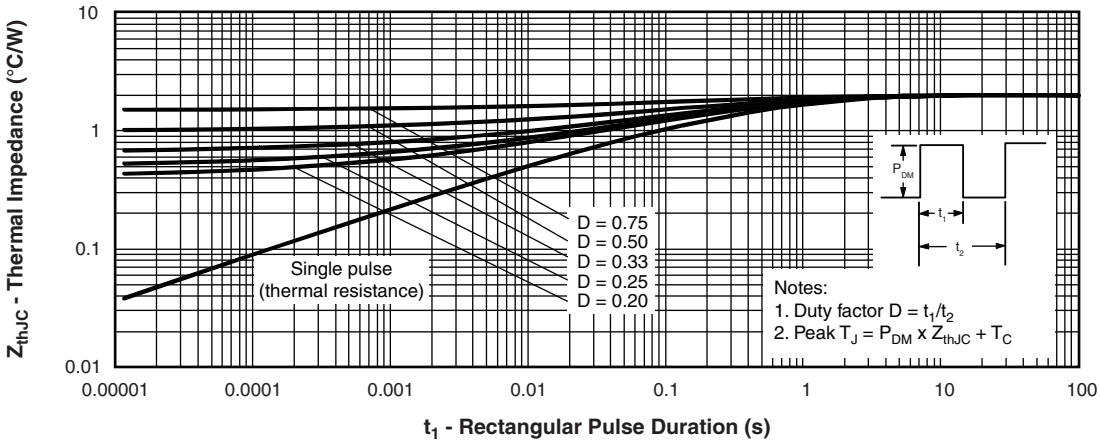


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics (Per Leg)

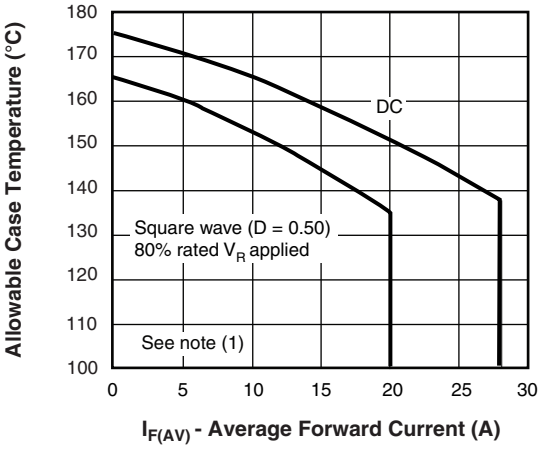


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

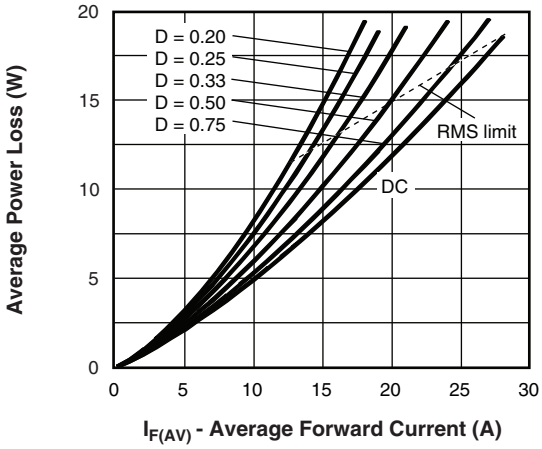


Fig. 6 - Forward Power Loss Characteristics (Per Leg)

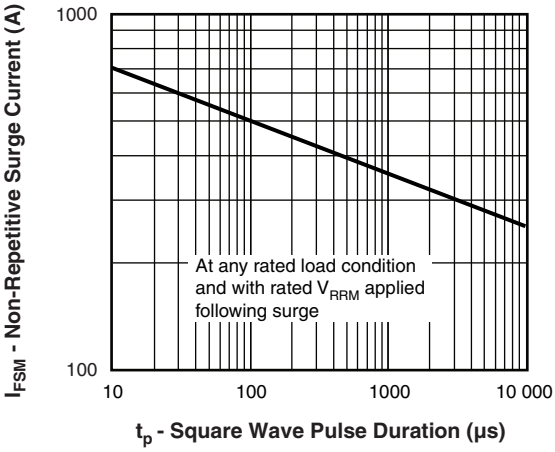


Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

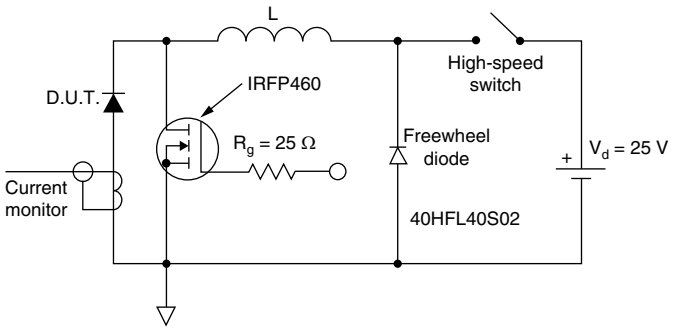


Fig. 8 - Unclamped Inductive Test Circuit

Note

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$;
Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}$/D) (see fig. 6);
Pd_{REV} = Inverse power loss = $V_{R1} \times I_R$ (1 - D); I_R at V_{R1} = 10 V

ORDERING INFORMATION TABLE

Device code

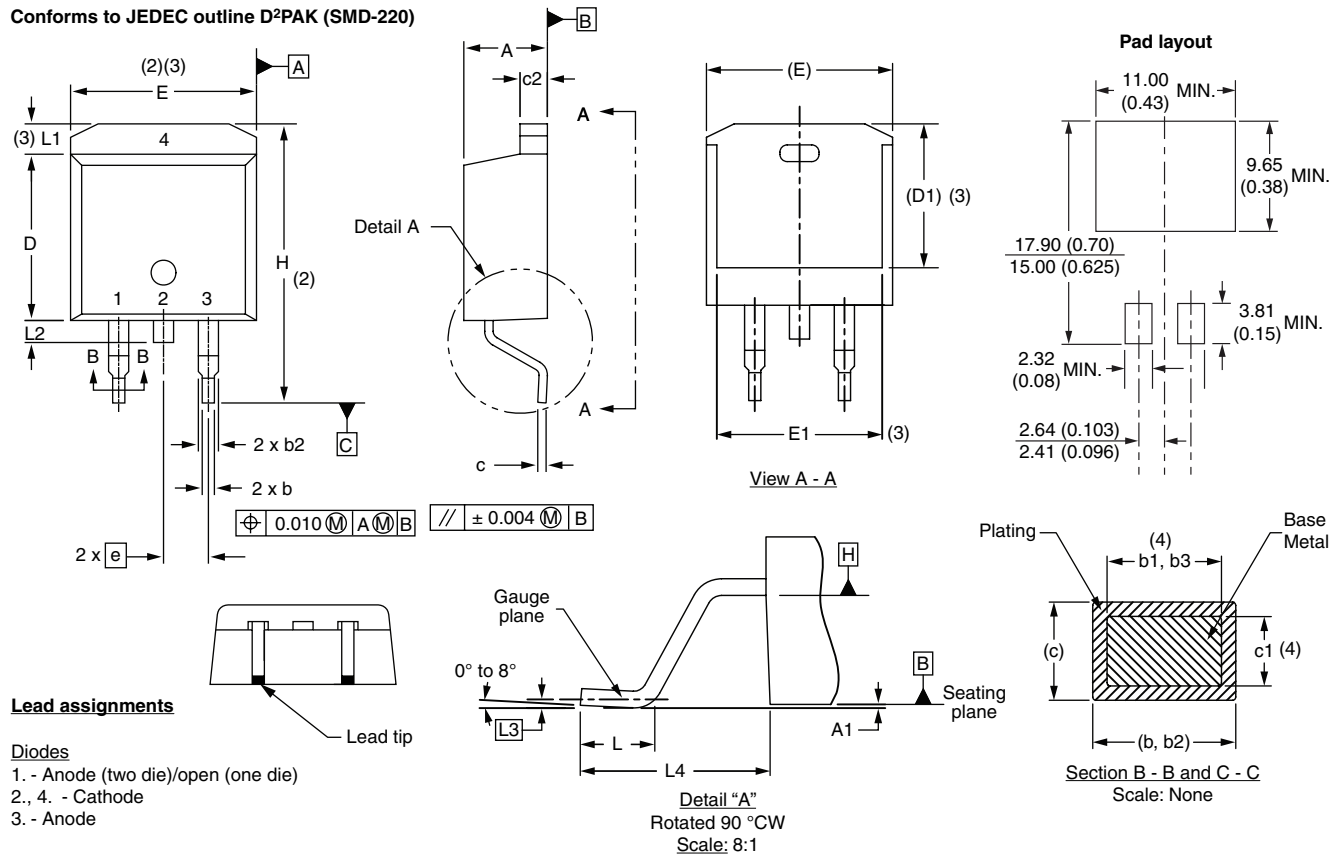
VS-	43	C	T	Q	100	S	TRL	PbF
1	2	3	4	5	6	7	8	9

- 1 - Vishay Semiconductors product
- 2 - Current rating (40 A)
- 3 - Circuit configuration: C = Common cathode
- 4 - T = TO-220
- 5 - Schottky “Q” series
- 6 - Voltage ratings (080 = 80 V, 100 = 100 V)
- 7 - • S = D^2PAK
  • -1 = TO-262
- 8 - • None = Tube (50 pieces)
  • TRL = Tape and reel (left oriented - for D^2PAK only)
  • TRR = Tape and reel (right oriented - for D^2PAK only)
- 9 - PbF = Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95014
Part marking information	www.vishay.com/doc?95008
Packaging information	www.vishay.com/doc?95032
SPICE model	www.vishay.com/doc?95065

D²PAK, TO-262

DIMENSIONS FOR D²PAK in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	0.00	0.254	0.000	0.010	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
H	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	-	1.65	-	0.066	3
L2	1.27	1.78	0.050	0.070	
L3	0.25 BSC		0.010 BSC		
L4	4.78	5.28	0.188	0.208	

Notes

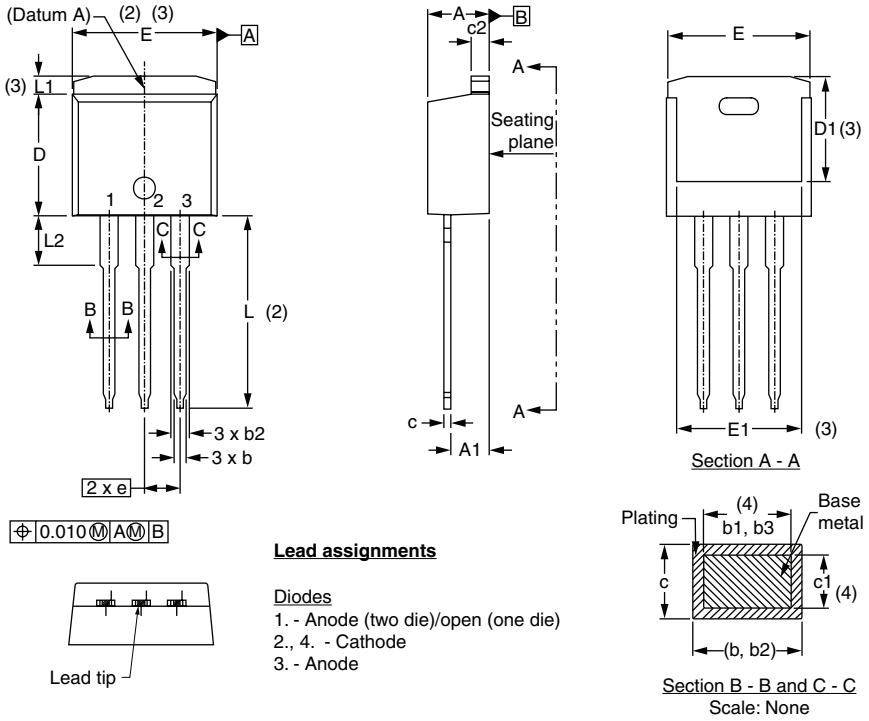
(1) Dimensioning and tolerancing per ASME Y14.5 M-1994
(2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
(3) Thermal pad contour optional within dimension E, L1, D1 and E1
(4) Dimension b1 and c1 apply to base metal only
(5) Datum A and B to be determined at datum plane H
(6) Controlling dimension: inch
(7) Outline conforms to JEDEC outline TO-263AB

Outline Dimensions

Vishay High Power Products D²PAK, TO-262

DIMENSIONS FOR TO-262 in millimeters and inches

Modified JEDEC outline TO-262



Lead assignments

Diodes
1. - Anode (two die)/open (one die)
2., 4. - Cathode
3. - Anode

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	2.03	3.02	0.080	0.119	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
L	13.46	14.10	0.530	0.555	
L1	-	1.65	-	0.065	3
L2	3.56	3.71	0.140	0.146	

Notes

(1) Dimensioning and tolerancing as per ASME Y14.5M-1994
(2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
(3) Thermal pad contour optional within dimension E, L1, D1 and E1
(4) Dimension b1 and c1 apply to base metal only
(5) Controlling dimension: inches
(6) Outline conform to JEDEC TO-262 except A1 (maximum), b (minimum) and D1 (minimum) where dimensions derived the actual package outline

For technical questions concerning discrete products, contact: diodes-tech@vishay.com
For technical questions concerning module products, contact: ind-modules@vishay.com

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