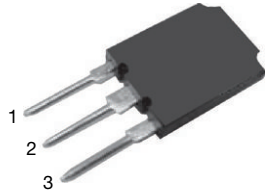
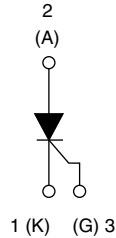


Thyristor High Voltage, Phase Control SCR, 70 A



Super TO-247



FEATURES

- High surge capability
- High voltage input rectification
- 150 °C maximum operating junction temperature
- Designed and qualified according to JEDEC®-JESD 47
- Halogen-free
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

LINKS TO ADDITIONAL RESOURCES



PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	70 A
V_{DRM}/V_{RRM}	1200 V, 1600 V
V_{TM}	1.40 V
I_{GT}	100 mA
T_J	-40 °C to 150 °C
Circuit configuration	Single SCR
Package	Super TO-247

APPLICATIONS

- AC switches
- High voltage input rectification (soft start)
- High current crow-bar
- Other phase-control circuits
- Designed to be used with Vishay input diodes, switches, and output rectifiers which are available in identical package outlines

DESCRIPTION

The VS-70TPS...M3 high voltage series of silicon controlled rectifiers are specifically designed for high and medium power switching, and phase control applications.

MECHANICAL DATA

Case: Super TO-247

Molding compound meets UL 94 V-0 flammability rating

Terminal: matte tin plated leads, solderable per J-STD-002

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$	Sinusoidal waveform	70	A
I_{RMS}	Lead current limitation	75	
V_{RRM}/V_{DRM}	Range	1200 to 1600	V
I_{TSM}		930	A
V_{TM}	100 A, $T_J = 25\text{ °C}$	1.40	V
dV/dt		500	V/ μ s
dI/dt		150	A/ μ s
T_J		-40 to +150	°C

VOLTAGE RATINGS			
PART NUMBER	V_{RRM}/V_{DRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 150 °C mA
VS-70TPS12-M3	1200	1300	42
VS-70TPS16-M3	1600	1700	42



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current	$I_{T(AV)}$	$T_C = 109\text{ }^\circ\text{C}$, 180° conduction half sine wave		70	A
Maximum continuous RMS on-state current as AC switch	$I_{T(RMS)}$	Lead current limitation		75	
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	10 ms sine pulse, rated V_{RRM} applied		780	A ² s
		10 ms sine pulse, no voltage reapplied		930	
Maximum I^2t for fusing	I^2t	10 ms sine pulse, rated V_{RRM} applied		3060	
		10 ms sine pulse, no voltage reapplied		4325	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1\text{ ms to }10\text{ ms}$, no voltage reapplied		43250	
Low level value of threshold voltage	$V_{T(TO)1}$	$T_J = 150\text{ }^\circ\text{C}$		0.95	V
High level value of threshold voltage	$V_{T(TO)2}$			1.05	
Low level value of on-state slope resistance	r_{T1}			4.15	mΩ
High level value of on-state slope resistance	r_{T2}			3.65	
Maximum peak on-state voltage	V_{TM}	100 A, $T_J = 25\text{ }^\circ\text{C}$		1.4	V
Maximum rate of rise of turned-on current	di/dt	$T_J = 25\text{ }^\circ\text{C}$		150	A/μs
Maximum holding current	I_H	Anode supply = 6 V, resistive load, initial $I_T = 1\text{ A}$, $T_J = 25\text{ }^\circ\text{C}$		250	mA
Maximum latching current	I_L	Anode supply = 6 V, resistive load, $T_J = 25\text{ }^\circ\text{C}$		400	
Maximum reverse and direct leakage current	I_{RRM}/I_{DRM}	$T_J = 25\text{ }^\circ\text{C}$	$V_R = \text{rated } V_{RRM}/V_{DRM}$ ($T_J = T_J \text{ max.}$, linear to 80 % $V_{DRM} = R_g\text{-k} = \text{Open}$)	1.0	V/μs
		$T_J = 150\text{ }^\circ\text{C}$		42	
Maximum rate of rise of off-state voltage	dV/dt	$T_J = 150\text{ }^\circ\text{C}$		500	

TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P_{GM}	$T = 30\text{ }^\circ\text{C}$		10	W
Maximum average gate power	$P_{G(AV)}$			2.5	
Maximum peak gate current	I_{GM}			2.5	A
Maximum peak negative gate voltage	$-V_{GM}$			10	V
Maximum required DC gate voltage to trigger	V_{GT}	$T_J = -40\text{ }^\circ\text{C}$	Anode supply = 6 V resistive load	1.8	
		$T_J = 25\text{ }^\circ\text{C}$		1.5	
		$T_J = 150\text{ }^\circ\text{C}$		1.0	
Maximum required DC gate current to trigger	I_{GT}	$T_J = -40\text{ }^\circ\text{C}$	Anode supply = 6 V resistive load	150	mA
		$T_J = 25\text{ }^\circ\text{C}$		100	
		$T_J = 150\text{ }^\circ\text{C}$		65	
Maximum DC gate voltage not to trigger	V_{GD}	$T_J = 150\text{ }^\circ\text{C}$, $V_{DRM} = \text{rated value}$		0.14	V
Maximum DC gate current not to trigger	I_{GD}			3.0	mA

SWITCHING						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Turn-on time	t_{gt}	$I_R = 70\text{ A}$, $V_D = 50\% V_{DRM}$, $I_{gt} = 300\text{ mA}$, $T_J = 25\text{ }^\circ\text{C}$		2	-	μs
Turn-off time	t_q	$I_R = 70\text{ A}$, $V_D = 80\% V_{DRM}$, $dV/dt = 20\text{ V}/\mu\text{s}$, $t_p = 200\text{ }^\circ\text{C}$, $I_{gt} = 100\text{ mA}$, $di/dt = 10\text{ A}/\mu\text{s}$, $V_R = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$		170	-	



THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction temperature range	T_J		-40 to +150	°C
Maximum storage temperature range	T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.27	°C/W
Maximum thermal resistance, junction to ambient	R_{thJA}		40	
Typical thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth and greased	0.2	
Approximate weight			6	g
Mounting torque	minimum		6 (5)	kgf · cm (lb · in)
	maximum		12 (10)	
Marking device		Case style Super TO-247	70TPS12	
			70TPS16	

ΔR_{thJ-hs} CONDUCTION PER JUNCTION											
DEVICE	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VS-70TPS...-M3	0.078	0.092	0.117	0.172	0.302	0.053	0.092	0.125	0.180	0.306	°C/W

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

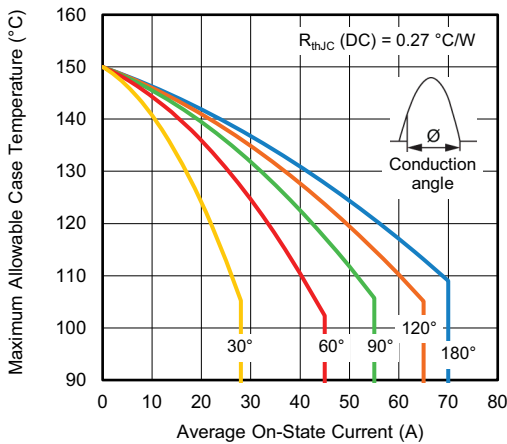


Fig. 1 - Current Rating Characteristics

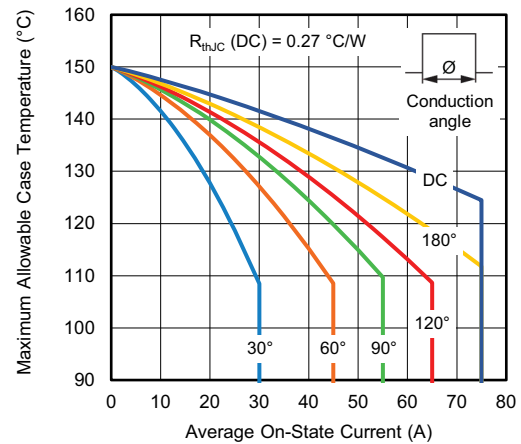


Fig. 2 - Current Rating Characteristics

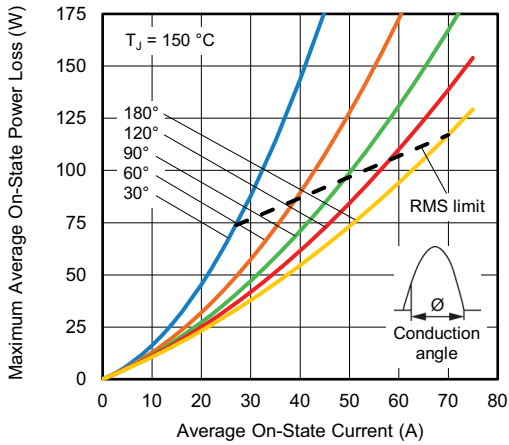


Fig. 3 - On-State Power Loss Characteristics

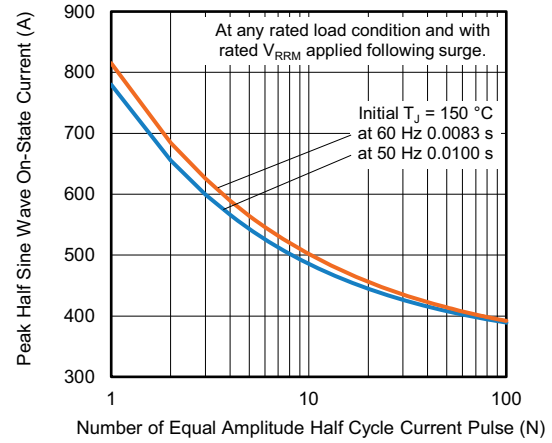


Fig. 5 - Maximum Non-Repetitive Surge Current

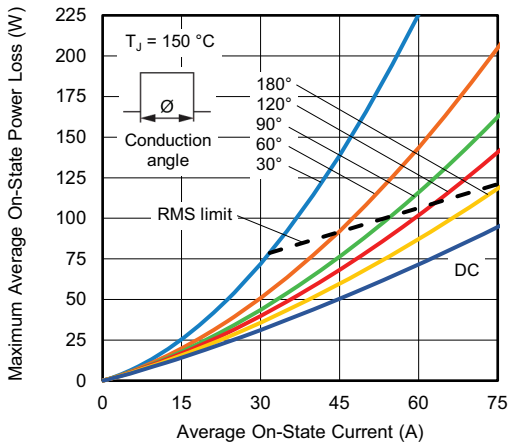


Fig. 4 - On-State Power Loss Characteristic

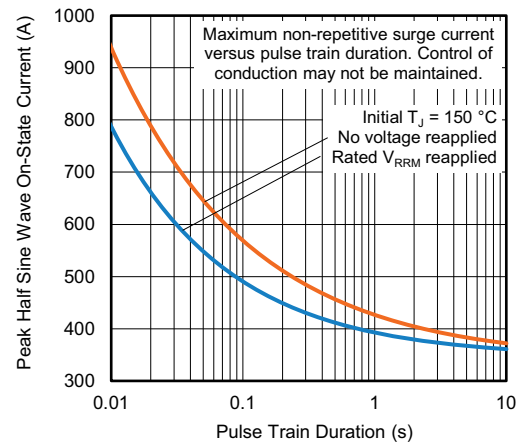


Fig. 6 - Maximum Non-Repetitive Surge Current

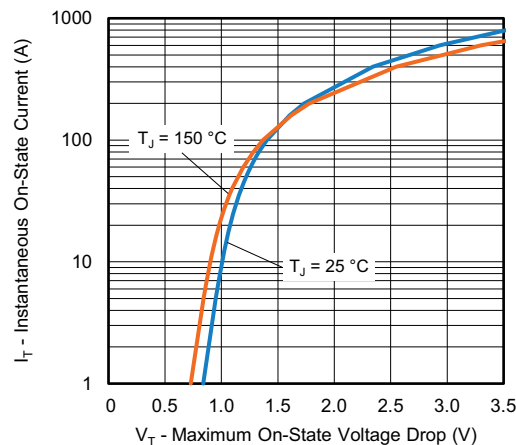


Fig. 7 - On-State Voltage Drop Characteristics

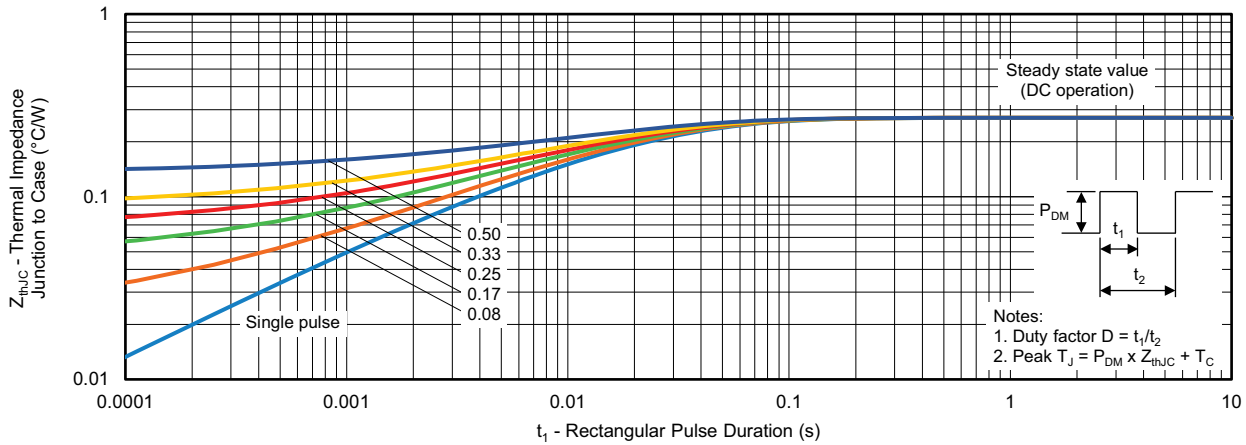


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

ORDERING INFORMATION TABLE

Device code	VS-	70	T	P	S	16	-M3						
	①	②	③	④	⑤	⑥	⑦						
	1	-	Vishay Semiconductors product										
	2	-	Current rating (70 = 70 A)										
	3	-	Circuit configuration: T = Thyristor										
	4	-	Package: P = Super TO-247										
	5	-	Type of silicon: S = Standard recovery rectifier										
	6	-	Voltage code x 100 = V_{RRM}		<table border="1"> <tr> <td>12</td> <td>=</td> <td>1200 V</td> </tr> <tr> <td>16</td> <td>=</td> <td>1600 V</td> </tr> </table>			12	=	1200 V	16	=	1600 V
12	=	1200 V											
16	=	1600 V											
	7	-	-M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free										

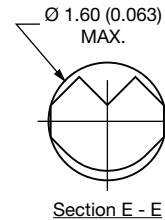
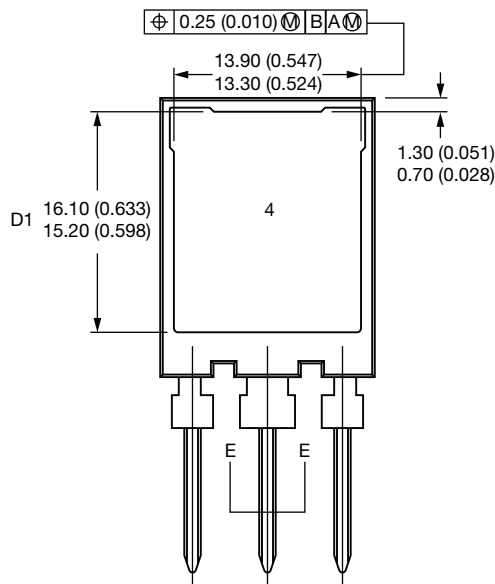
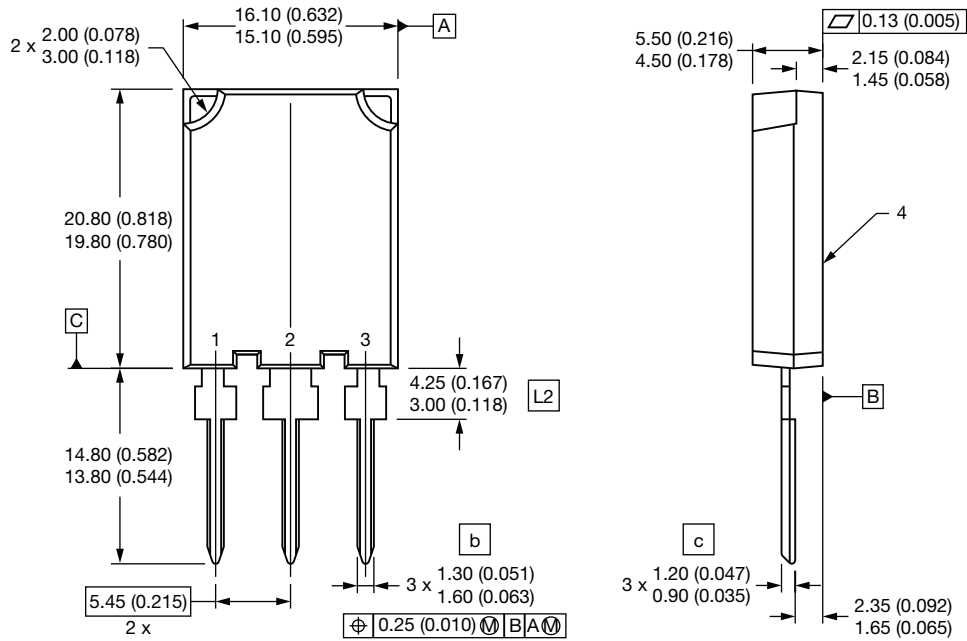
ORDERING INFORMATION (example)			
PREFERRED P/N	QUANTITY PER TUBE	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-70TPS12-M3	25	500	Antistatic plastic tube
VS-70TPS16-M3	25	500	Antistatic plastic tube

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?97136
Part marking information	www.vishay.com/doc?95683



Super TO-247

DIMENSIONS in millimeters (inches)



Lead assignments

SCR

- 1 - Cathode
- 2 - Anode
- 3 - Gate
- 4 - Anode

Notes

- (1) Dimension and tolerancing per ASME Y14.5M-1994
- (2) Controlling dimension: millimeter
- (3) Outline conforms to JEDEC® outline TO-274AA, except D1, b min., c min., L2 min.



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