ADD-A-PAK Generation VII
Power Modules Schottky Rectifier, 400 A

ADD-A-PAK

FEATURES

- 175 °C T_J operation
- Low forward voltage drop
- High frequency operation
- Low thermal resistance
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- High surge capability
- Easy mounting on heatsink

PRODUCT SUMMARY	
$I_{F(AV)}$	400 A
V_R	100 V
Package	ADD-A-PAK
Circuit	Two diodes common cathodes

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

ELECTRICAL DESCRIPTION

The VS-VSKCS403.. Schottky rectifier common cathode has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature.
Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	400	A
V_{RRM}		100	V
I_{FSM}	t_p = 5 µs sine	20 000	A
V_F	200 A_{pk}, T_J = 125 °C	0.83	V
T_J	Range	-55 to 175	°C

VOLTAGE RATINGS			
PARAMETER	SYMBOL	VS-VSKCS403/100	UNITS
Maximum DC reverse voltage	V_R	100	V
Maximum working peak reverse voltage	V_{RWM}		

ABSOLUTE MAXIMUM RATINGS						
PARAMETER		SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	per module	$I_{F(AV)}$	50 % duty cycle at T_C = 111 °C, rectangular waveform		400	A
	per leg				200	
Maximum peak one cycle non-repetitive surge current		I_{FSM}	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with rated V_{RRM} applied	20 000	
			10 ms sine or 6 ms rect. pulse		2300	
Non-repetitive avalanche energy		E_{AS}	T_J = 25 °C, I_{AS} = 5.5 A, L = 1 mH		15	mJ
Repetitive avalanche current		I_{AR}	Current decaying linearly to zero in 1 µs Frequency limited by T_J maximum V_A = 1.5 x V_R typical		1	A

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop	V_{FM}	200 A	T_J = 25 °C	0.99	V
		400 A		1.3	
		200 A	T_J = 125 °C	0.83	
		400 A		1.09	
Maximum reverse leakage current	I_{RM}	T_J = 25 °C	V_R = Rated V_R	6	mA
		T_J = 125 °C		80	
Maximum junction capacitance	C_T	V_R = 5 V_{DC} (test signal range 100 kHz to 1 MHz), 25 °C		5500	pF
Typical series inductance	L_S	Measured lead to lead 5 mm from package body		5.0	nH
Maximum voltage rate of change	dV/dt	Rated V_R		10 000	V/µs
Maximum RMS insulation voltage	V_{INS}	50 Hz		3000 (1 min) 3600 (1 s)	V

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		-55 to 175	°C
Maximum thermal resistance, junction to case per leg	R_{thJC}	DC operation	0.26	°C/W
Typical thermal resistance, case to heatsink per module	R_{thCS}		0.1	
Approximate weight			75	g
			2.7	oz.
Mounting torque ± 10 % to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the spread of the compound.	4	Nm
busbar			3	
Case style		JEDEC®	TO-240AA compatible	

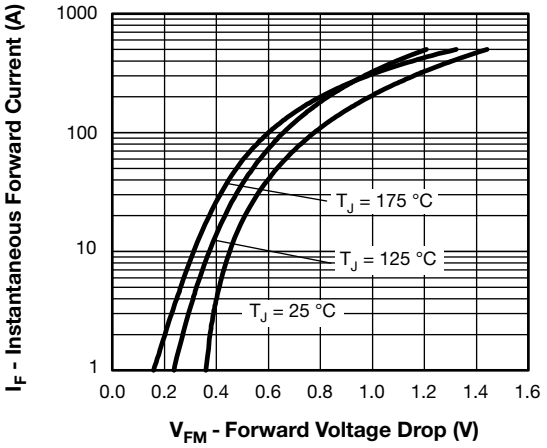


Fig. 1 - Maximum Forward Voltage Drop Characteristics

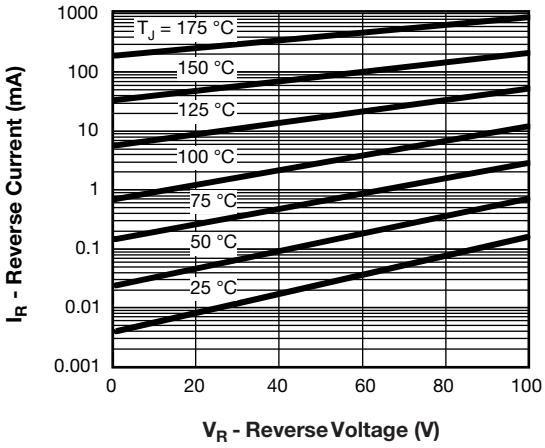


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

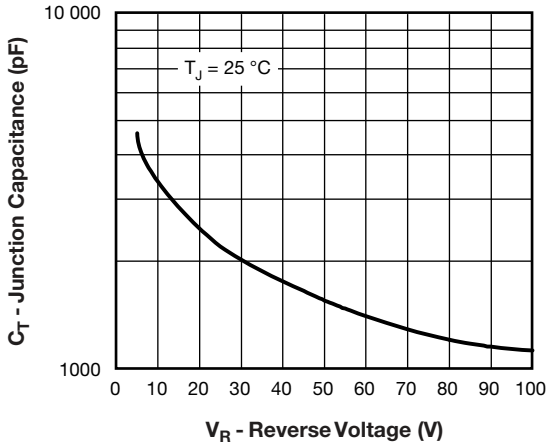


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

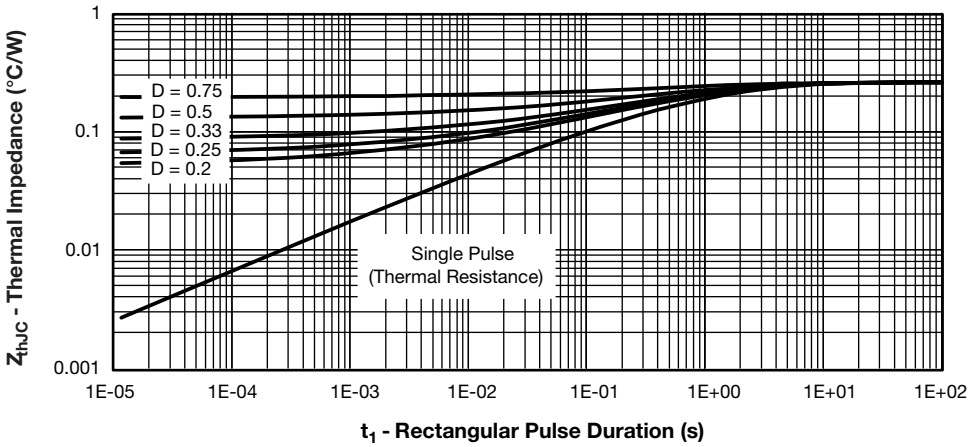


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

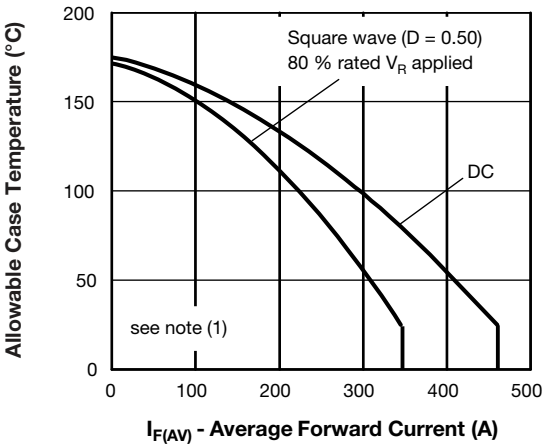


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

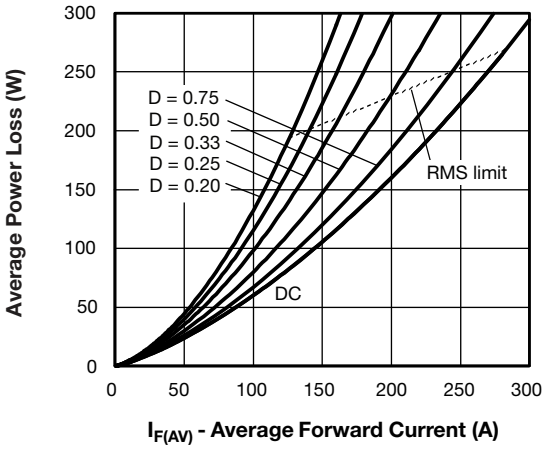


Fig. 6 - Forward Power Loss Characteristics

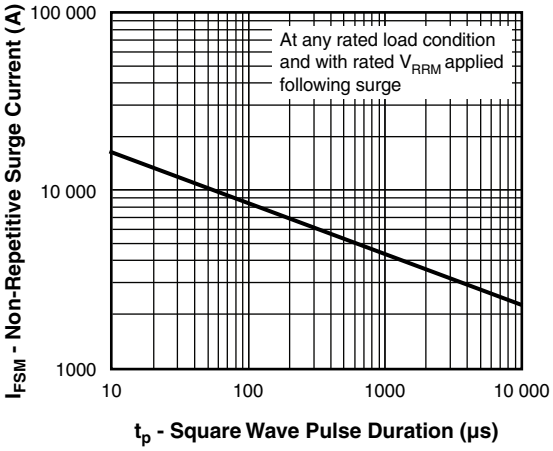


Fig. 7 - Maximum Non-Repetitive Surge Current

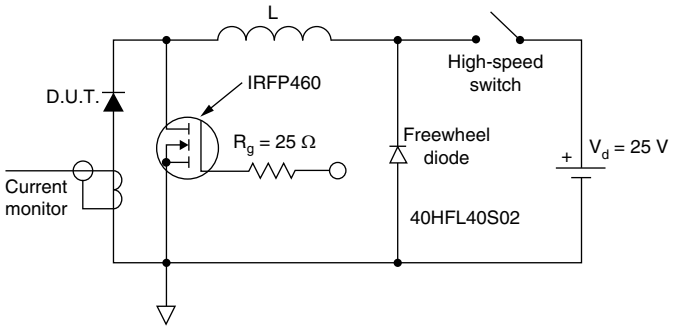


Fig. 8 - Unclamped Inductive Test Circuit

Note

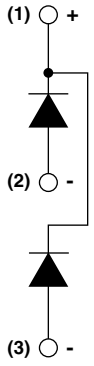
(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$;
Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}$/D) (see fig. 6);
Pd_{REV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at V_{R1} = 80 % rated V_R

ORDERING INFORMATION TABLE

Device code	VS-VS	KC	S	40	3	/	100
	1	2	3	4	5		6

- 1 - VS-VS = Vishay Semiconductors product
- 2 - Circuit configuration:
  KC = ADD-A-PAK - 2 diodes/common cathode
- 3 - S = Schottky diode
- 4 - Average rating (x 10)
- 5 - Product silicon identification
- 6 - Voltage rating (100 = 100 V)

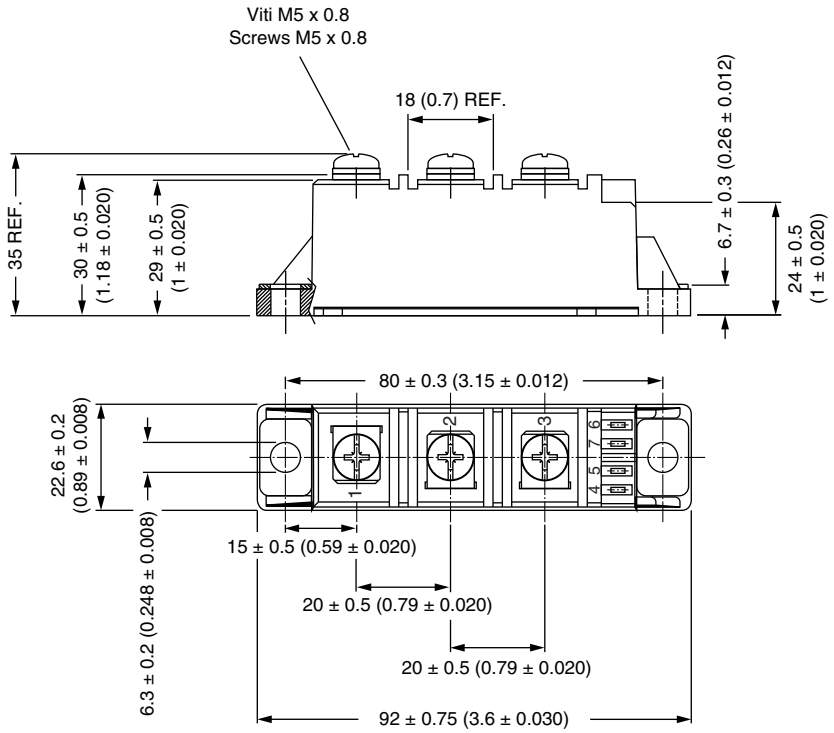
CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95369

ADD-A-PAK Generation VII - Diode

DIMENSIONS in millimeters (inches)



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