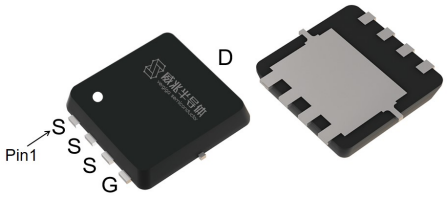
## Features

- Enhancement mode
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested,100% Rg Tested

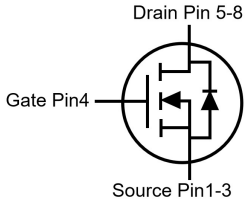
| | | |
|---|---|---|
| $V_{DS}$ | 100 | V |
| $R_{DS(on),TYP}$@ $V_{GS}$=10 V | 100 | mΩ |
| $R_{DS(on),TYP}$@ $V_{GS}$=4.5 V | 140 | mΩ |
| $I_{D(Silicon\ Limited)}$ | 7.4 | A |

Pb-Free RoHS HF Halogen-Free

**PDFN3333**




| Part ID | Package Type | Marking | Packing |
|---|---|---|---|
| VS1850GE | PDFN3333 | 1850GE | 5000PCS/Reel |




## Maximum ratings, at $T_A$ =25°C, unless otherwise specified

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source breakdown voltage | | 100 | V |
| $V_{GS}$ | Gate-Source voltage | | ±20 | V |
| $I_S$ | Diode continuous forward current (Silicon limited) | $T_C$ = 25°C | 7.4 | A |
| $I_D$ | Continuous drain current @VGS=10V (Silicon limited) | $T_C$ = 25°C | 7.4 | A |
| $I_D$ | Continuous drain current @VGS=10V (Silicon limited) | $T_C$ = 100°C | 4.7 | A |
| $I_{DM}$ | Pulse drain current tested ① | $T_C$ = 25°C | 19 | A |
| $I_{DSM}$ | Continuous drain current @VGS=10V | $T_A$ = 25°C | 3 | A |
| | | $T_A$ = 70°C | 2.4 | A |
| EAS | Maximum Avalanche energy, single pulsed ② | | 0.64 | mJ |
| $P_D$ | Maximum power dissipation ③ | $T_C$ = 25°C | 14 | W |
| | | $T_C$ = 100°C | 5.4 | W |
| $P_{DSM}$ | Maximum power dissipation ④ | $T_A$ = 25°C | 2.3 | W |
| | | $T_A$ = 70°C | 1.5 | W |
| $T_J$,$T_{STG}$ | Operating Junction and Storage Temperature Range | | -55 to 150 | °C |

## Thermal Characteristics

| Symbol | Parameter | Typical | Max | Unit |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case ⑤ | 7.7 | 9.2 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient ⑥ | 46 | 55 | °C/W |

## Electrical Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Electrical Characteristics @ $T_j$=25°C (unless otherwise stated)** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250uA | 100 | -- | -- | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current($T_j$=25℃) | $V_{DS}$=100V,$V_{GS}$=0V | -- | -- | 1 | μA |
| | Zero Gate Voltage Drain Current($T_j$=125℃)⑦ | $V_{DS}$=100V,$V_{GS}$=0V | -- | -- | 100 | μA |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$=±20V,$V_{DS}$=0V | -- | -- | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 1.3 | 1.8 | 2.4 | V |
| $R_{DS(on)}$ | Drain-Source On-State Resistance ⑧ | $V_{GS}$=10V, $I_D$=5A | -- | 100 | 130 | mΩ |
| | | ($T_j$=100℃)⑦ | -- | 150 | -- | mΩ |
| $R_{DS(on)}$ | Drain-Source On-State Resistance ⑧ | $V_{GS}$=4.5V, $I_D$=2A | -- | 140 | 180 | mΩ |
| **Dynamic Electrical Characteristics @ $T_j$ = 25°C (unless otherwise stated)** | | | | | | |
| Ciss | Input Capacitance ⑦ | $V_{DS}$=50V,$V_{GS}$=0V, f=100KHz | -- | 160 | -- | pF |
| Coss | Output Capacitance ⑦ | | -- | 45 | -- | pF |
| Crss | Reverse Transfer Capacitance ⑦ | | -- | 5 | -- | pF |
| Rg | Gate Resistance | f=1MHz | -- | 1.9 | -- | Ω |
| Qg(10V) | Total Gate Charge ⑦ | $V_{DS}$=50V,$I_D$=5A, $V_{GS}$=10V | -- | 3.9 | -- | nC |
| Qg(4.5V) | Total Gate Charge ⑦ | | -- | 2 | -- | nC |
| Qgs | Gate-Source Charge ⑦ | | -- | 0.9 | -- | nC |
| Qgd | Gate-Drain Charge ⑦ | | -- | 1 | -- | nC |
| **Switching Characteristics** ⑦ | | | | | | |
| Td(on) | Turn-on Delay Time | $V_{DD}$=50V, $I_D$=5A, $R_G$=3Ω, $V_{GS}$=10V | -- | 3.2 | -- | ns |
| Tr | Turn-on Rise Time | | -- | 2.8 | -- | ns |
| Td(off) | Turn-Off Delay Time | | -- | 6.4 | -- | ns |
| Tf | Turn-Off Fall Time | | -- | 1.6 | -- | ns |
| **Source- Drain Diode Characteristics@ $T_j$= 25°C (unless otherwise stated)** | | | | | | |
| $V_{SD}$ | Forward on voltage | $I_{SD}$=5A,$V_{GS}$=0V | -- | 0.95 | 1.2 | V |
| Trr | Reverse Recovery Time ⑦ | $V_{DD}$=50V, $I_{sd}$=5A, $V_{GS}$=0V di/dt=100A/μs | -- | 39 | -- | ns |
| Qrr | Reverse Recovery Charge ⑦ | | -- | 18 | -- | nC |

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This maximum value is based on starting $T_J$ = 25°C, L = 0.5mH, $R_G$ = 25Ω, $I_{AS}$ = 1.6A, $V_{GS}$ =10V； 100% FT tested at L = 0.5mH, $I_{AS}$ = 1.1A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ These tests are performed respectively with the device mounted on a 1 in2 pad and a minimum pad of 2oz. Copper FR-4 board in a still air environment with TA=25°C, using Transient Dual Interface method to acquire RθJC.

⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

## Typical Characteristics

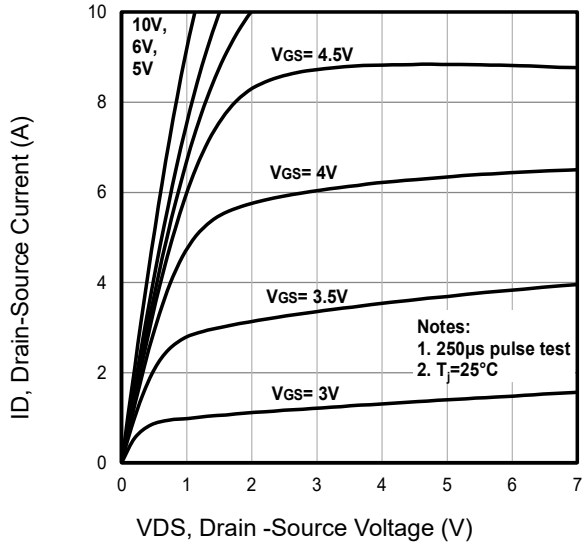



**Fig1.** Typical Output Characteristics

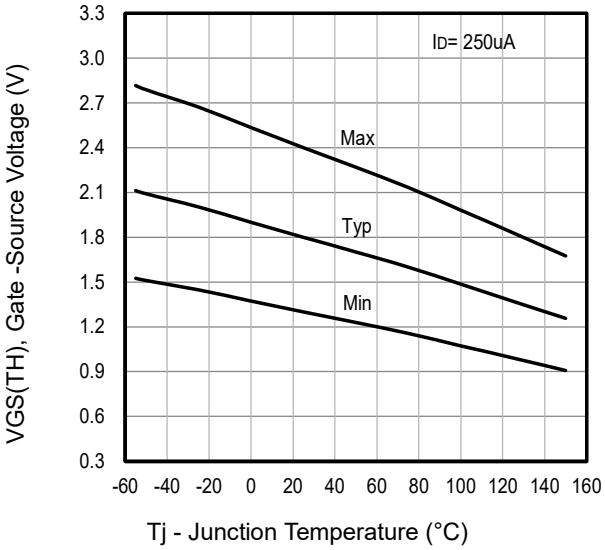



**Fig2.** Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

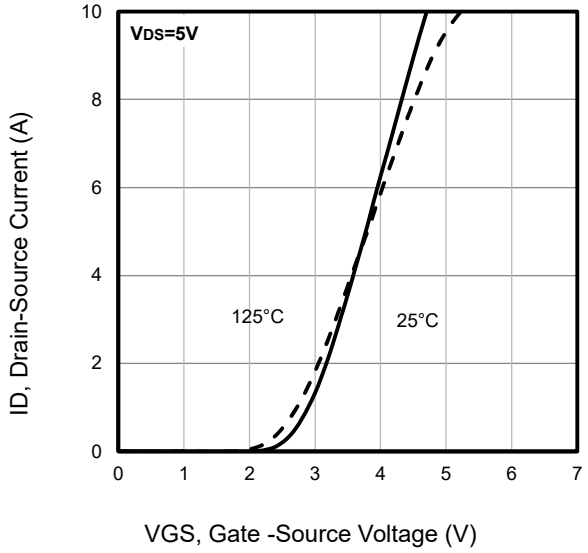



**Fig3.** Typical Transfer Characteristics

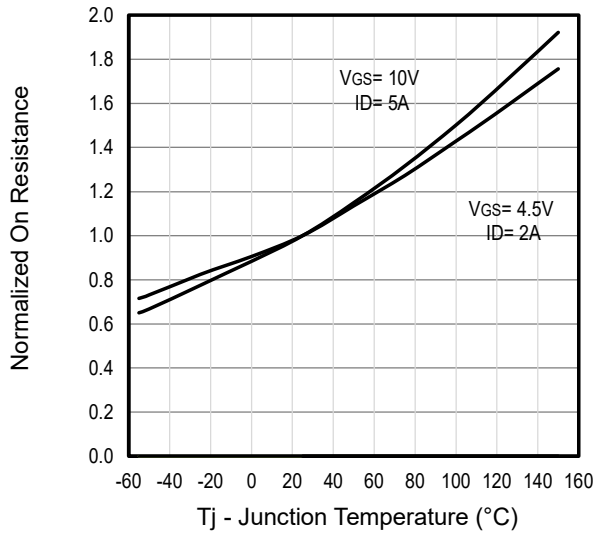



**Fig4.** Typical Normalized On-Resistance Vs. Tj

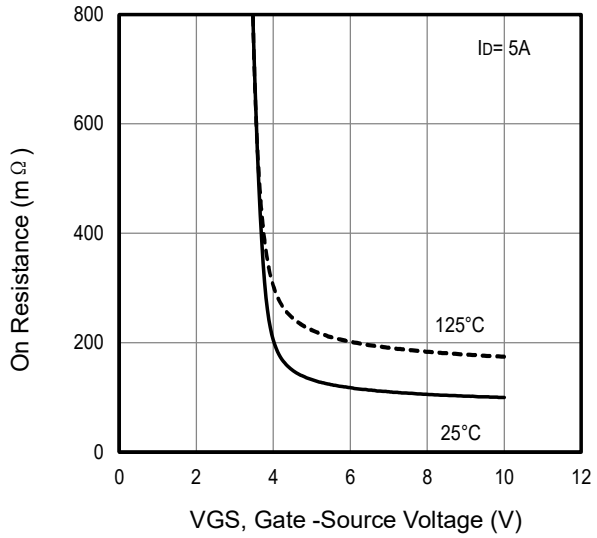



**Fig5.** Typical On Resistance Vs Gate -Source Voltage

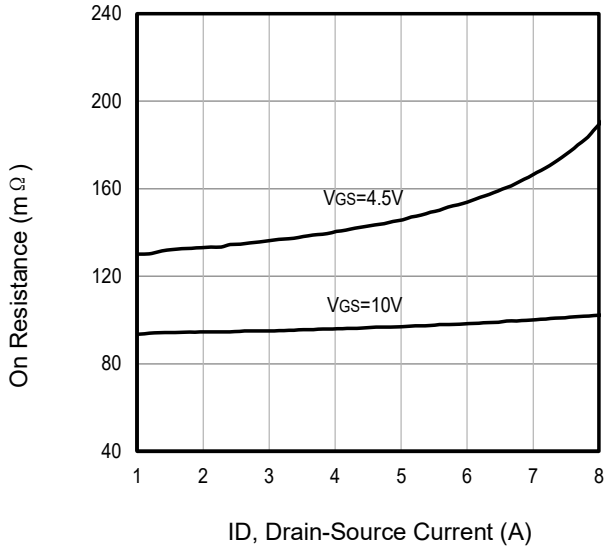



**Fig6.** Typical On Resistance Vs Drain Current

## Typical Characteristics

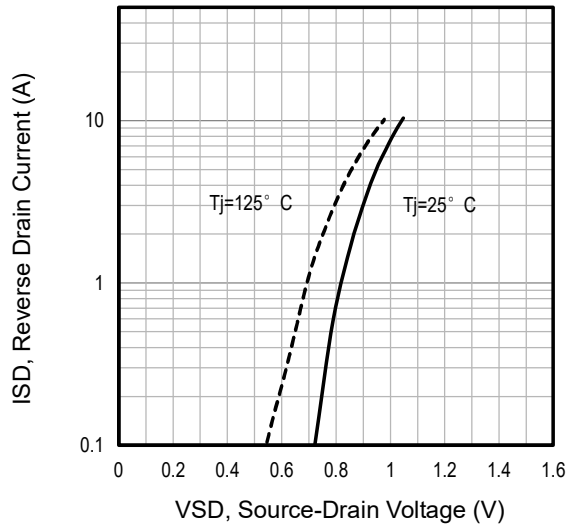



**Fig7.** Typical Source-Drain Diode Forward Voltage

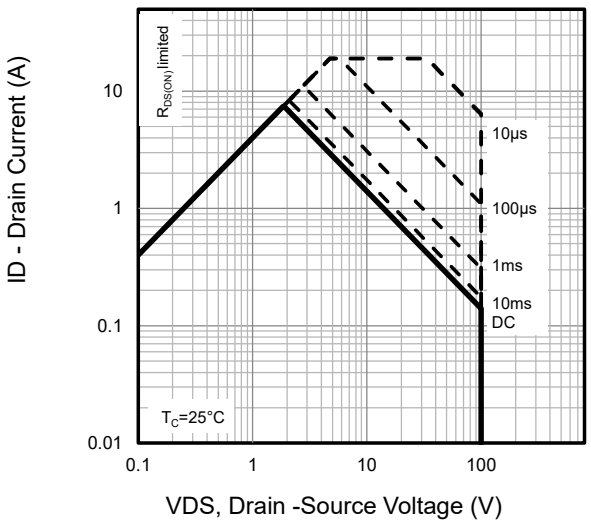



**Fig8.** Maximum Safe Operating Area

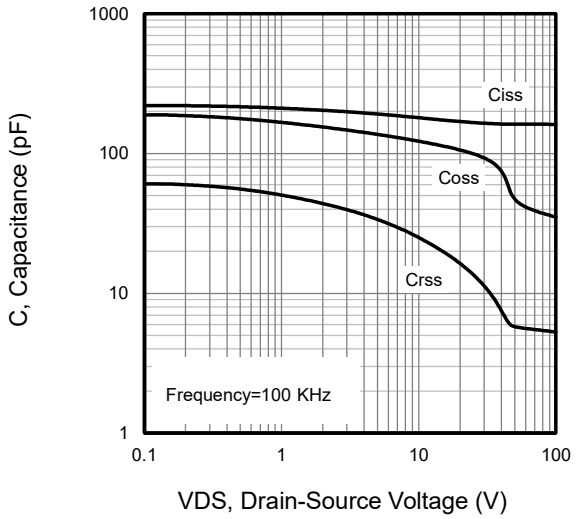



**Fig9.** Typical Capacitance Vs. Drain-Source Voltage

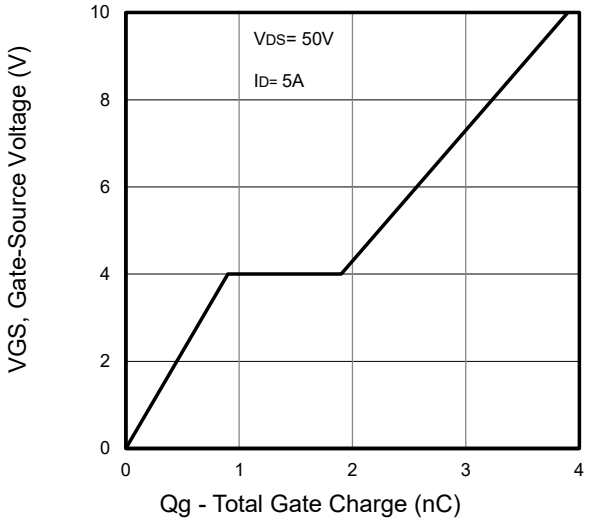



**Fig10.** Typical Gate Charge Vs. Gate-Source Voltage

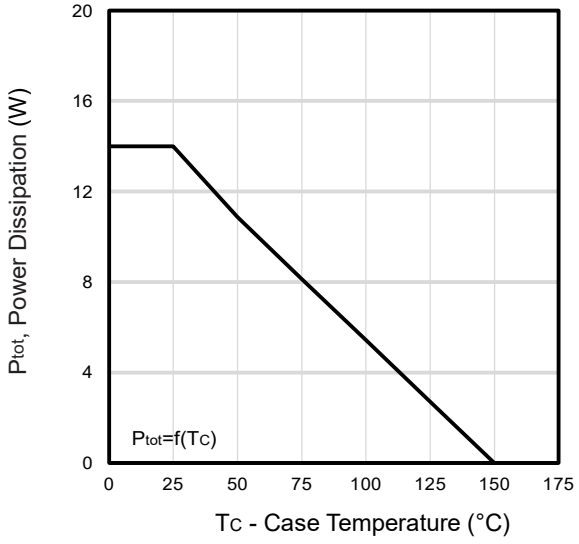



**Fig11.** Power Dissipation Vs. Case Temperature

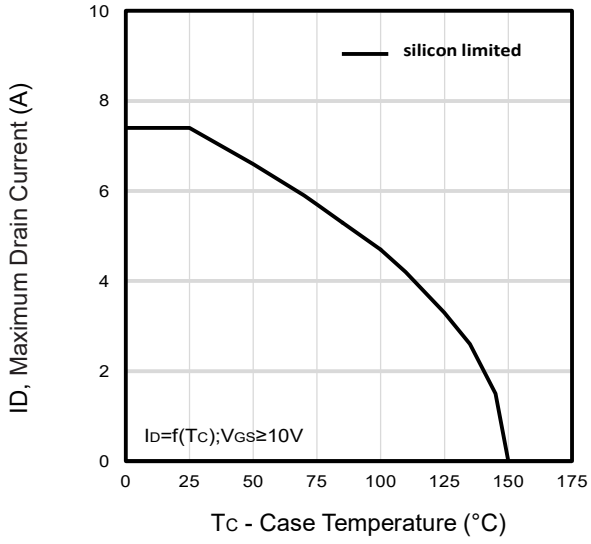



**Fig12.** Maximum Drain Current Vs. Case Temperature

## Typical Characteristics

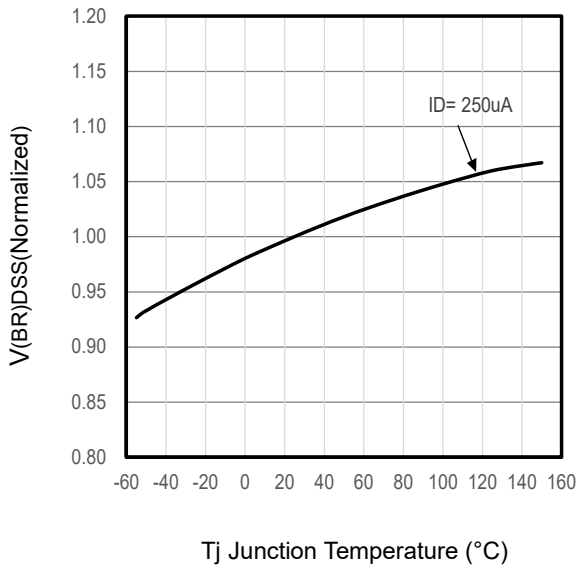



**Fig13.** Typical $V_{(BR)DSS}$ Vs Tj

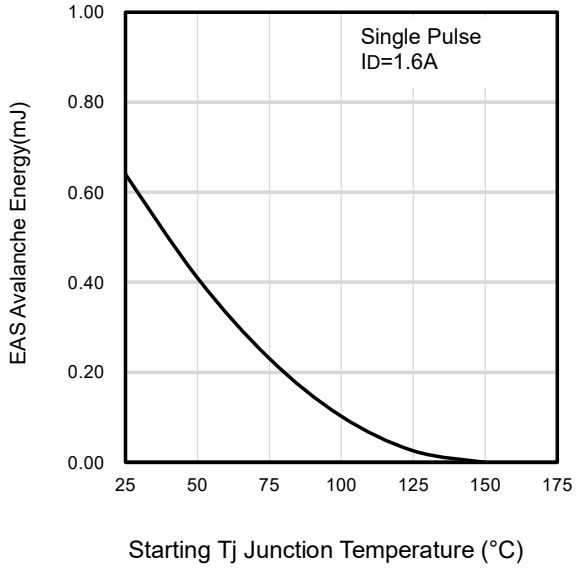



**Fig14.** Maximum Avalanche Energy vs Temperature (°C)

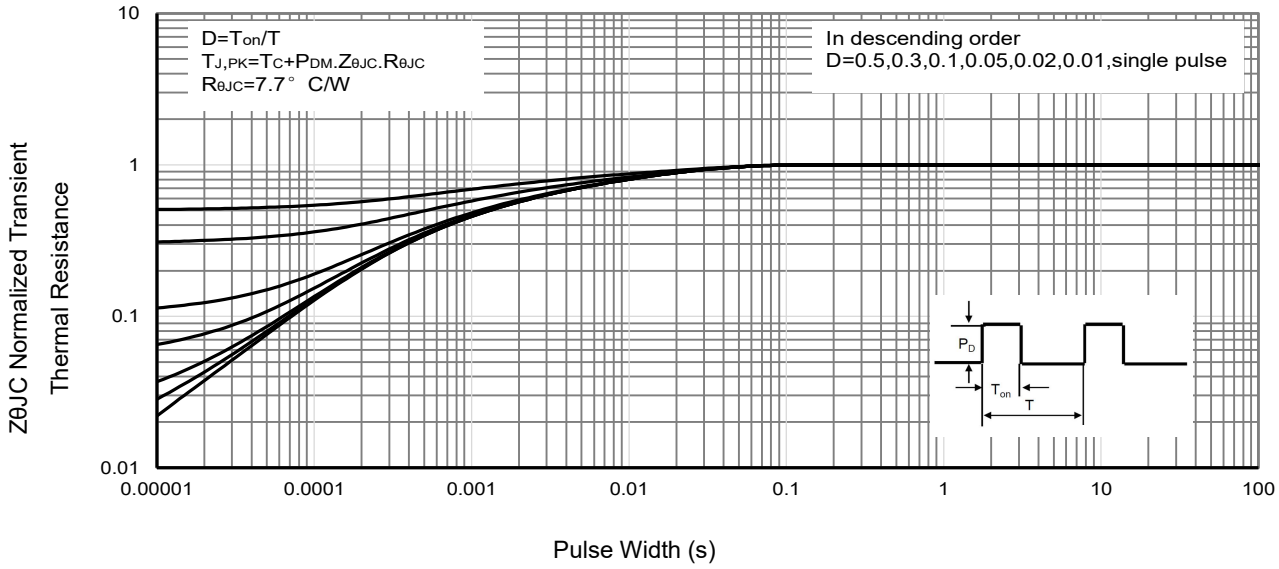



**Fig15 .** Normalized Maximum Transient Thermal Impedance

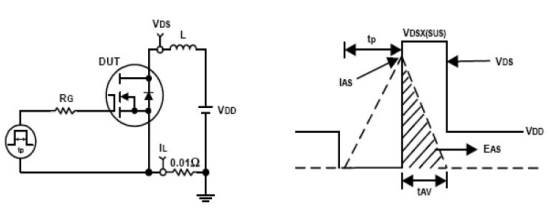



**Fig16.** Unclamped Inductive Test Circuit and waveforms

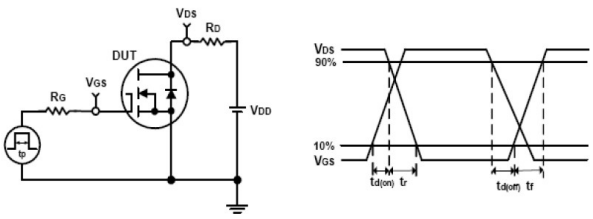
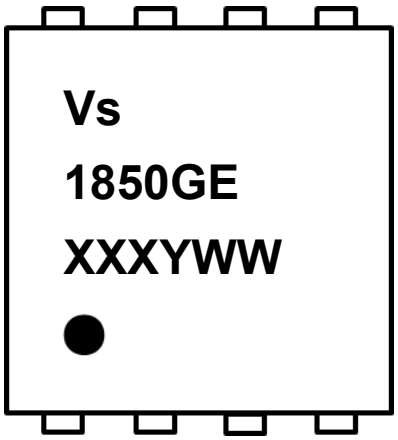



**Fig17.** Switching Time Test Circuit and waveforms

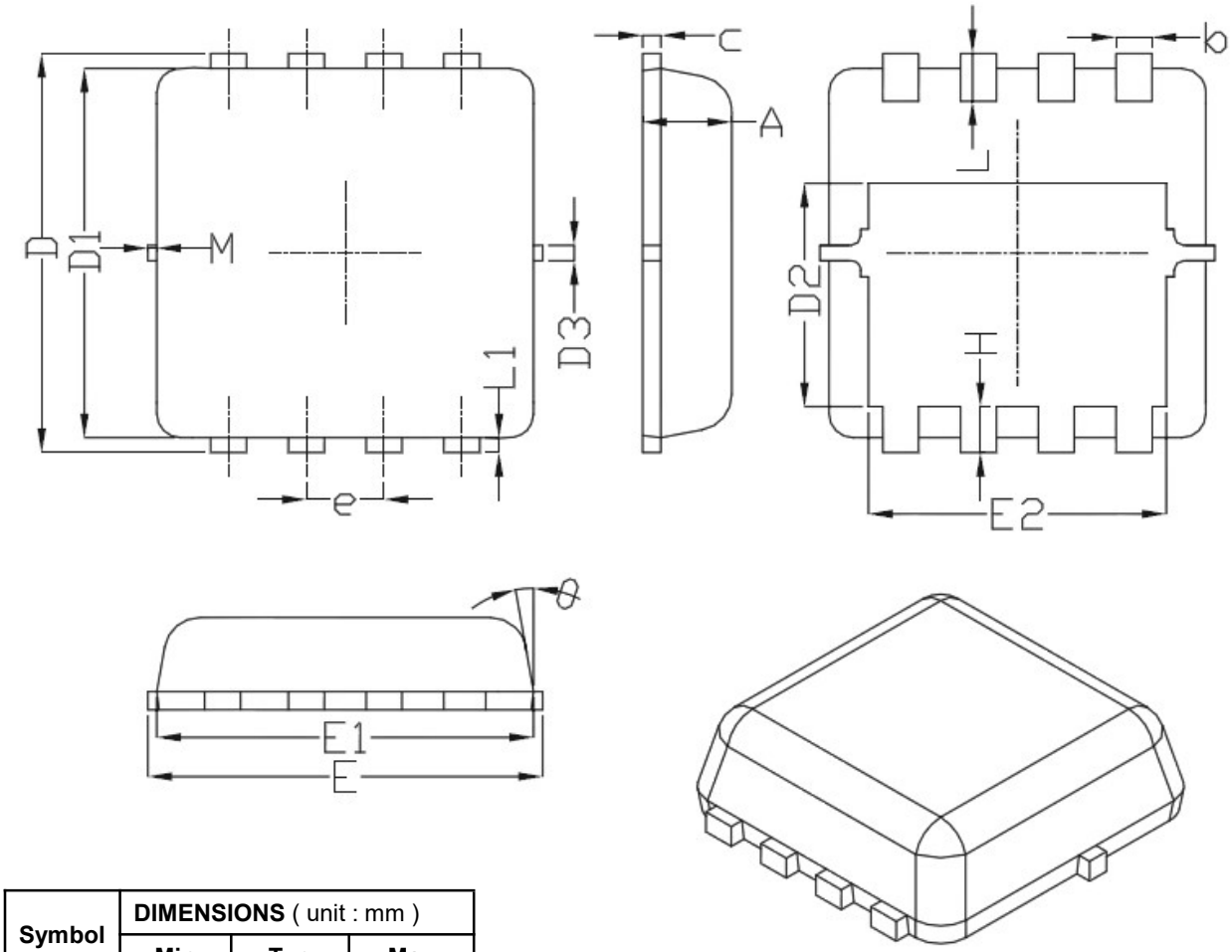
## Marking Information




1st line: Vergiga Code（Vs）
2nd line: Part Number（1850GE）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

| Code | C | D | E | F | G | H | J | K | L | M | N | P | Q | R | S | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Year | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 |

## PDFN3333 Package Outline Data




| Symbol | DIMENSIONS ( unit : mm ) | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.25 | 0.30 | 0.35 |
| C | 0.10 | 0.15 | 0.25 |
| D | 3.25 | 3.35 | 3.45 |
| D1 | 3.00 | 3.10 | 3.20 |
| D2 | 1.78 | 1.88 | 1.98 |
| D3 | -- | 0.13 | -- |
| E | 3.00 | 3.20 | 3.40 |
| E1 | 3.00 | 3.10 | 3.20 |
| E2 | 2.39 | 2.49 | 2.59 |
| e | 0.65 BSC | | |
| H | 0.30 | 0.39 | 0.50 |
| L | 0.30 | 0.40 | 0.50 |
| L1 | -- | 0.13 | -- |
| θ | -- | 10° | 12° |
| M | * | * | 0.15 |
| * Not specified | | | |

Notes:

1. Follow JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.