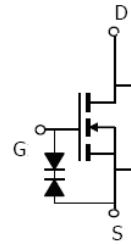
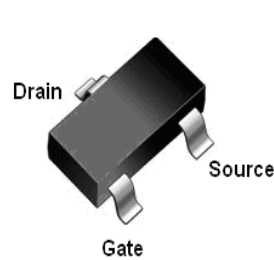


Features

- N-Channel, 2.5V Logic Level Control
- Enhancement mode
- Low on-resistance @ $V_{GS}=2.5\text{ V}$
- Fast Switching
- ESD Protection HBM 2.5KV
- Pb-free lead plating; RoHS compliant

V_{DS}	20	V
$R_{DS(on),typ} @ V_{GS}=4.5\text{ V}$	17	m Ω
$R_{DS(on),typ} @ V_{GS}=2.5\text{ V}$	23	m Ω
I_D	6.5	A

SOT23



Part ID	Package Type	Marking	Tape and reel information
VS3416AC	SOT23	V26	3000pcs/reel

Maximum ratings, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	20	V
I_S	Diode continuous forward current	$T_C=25^\circ\text{C}$ 1.3	A
I_D	Continuous drain current @ $V_{GS}=4.5\text{V}$	$T_C=25^\circ\text{C}$ 6.5	A
		$T_C=70^\circ\text{C}$ 5.2	A
I_{DM}	Pulse drain current tested ①	$T_C=25^\circ\text{C}$ 26	A
P_D	Maximum power dissipation	$T_C=25^\circ\text{C}$ 1	W
V_{GS}	Gate-Source voltage	± 8	V
ESD	HBM	2.5	KV
$T_{STG} T_J$	Storage and operating temperature range	-55 to 150	$^\circ\text{C}$
Thermal Characteristics			
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	80	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	125	$^\circ\text{C/W}$

Typical Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current (T _c =25°C)	V _{DS} =20V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _c =125°C)	V _{DS} =20V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±4.5V, V _{DS} =0V	--	--	±1	μA
		V _{GS} =±8V, V _{DS} =0V	--	--	±10	μA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.4	0.8	1.2	V
R _{DS(ON)}	Drain-Source On-State Resistance ②	V _{GS} =4.5V, I _D =6A	--	17	21	mΩ
		V _{GS} =2.5V, I _D =5A	--	23	28	mΩ
		V _{GS} =1.8V, I _D =2A	--	35	41	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1MHz	--	450	--	pF
C _{oss}	Output Capacitance		--	110	--	pF
C _{rss}	Reverse Transfer Capacitance		--	100	--	pF
Q _g	Total Gate Charge	V _{DS} =10V, I _D =6A, V _{GS} =4.5V	--	8.2	--	nC
Q _{gs}	Gate-Source Charge		--	2.4	--	nC
Q _{gd}	Gate-Drain Charge		--	3.3	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =10V, I _D =6A, R _G =3Ω, V _{GS} =4.5V, R _L =2Ω,	--	6.5	--	ns
t _r	Turn-on Rise Time		--	8	--	ns
t _{d(off)}	Turn-Off Delay Time		--	35	--	ns
t _f	Turn-Off Fall Time		--	9.1	--	ns
Source- Drain Diode Characteristics						
V _{SD}	Forward on voltage	T _J =25°C, I _{SD} =1.6A, V _{GS} =0V	--	0.76	1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} =6A, dI/dt=100A/μs	--	15	--	ns
Q _{rr}	Reverse Recovery Charge		--	5.5	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 ② Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

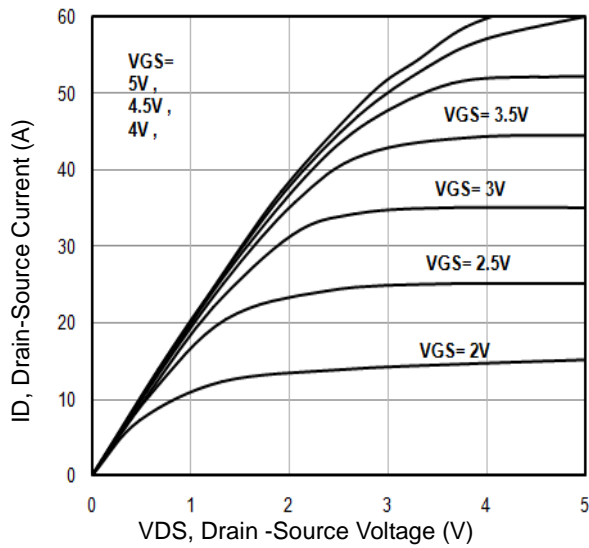


Fig1. Typical Output Characteristics

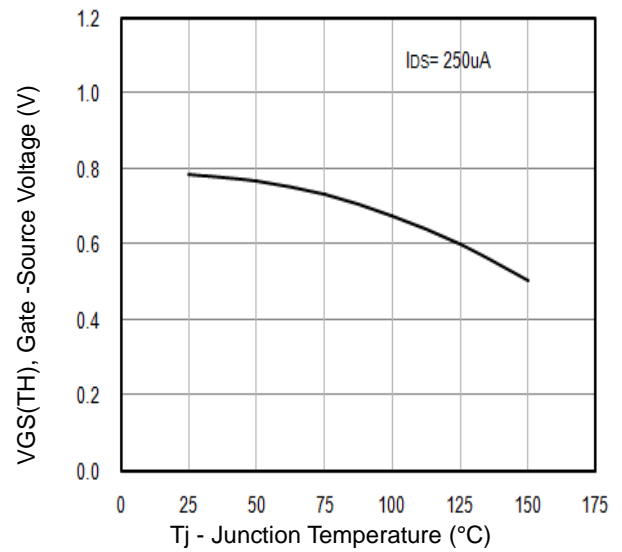


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

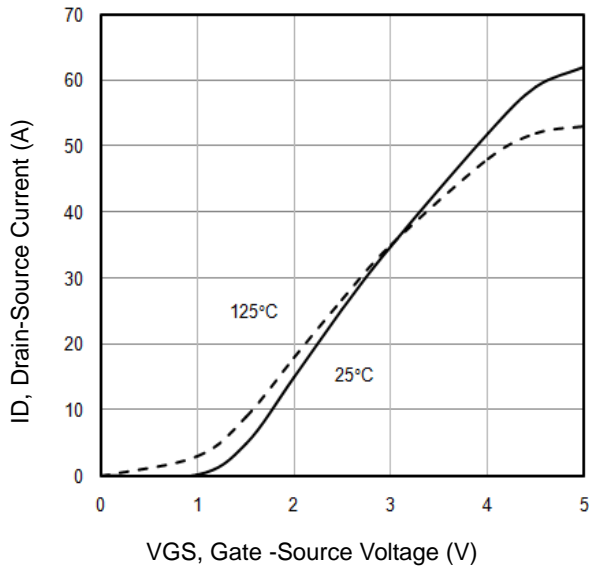


Fig3. Typical Transfer Characteristics

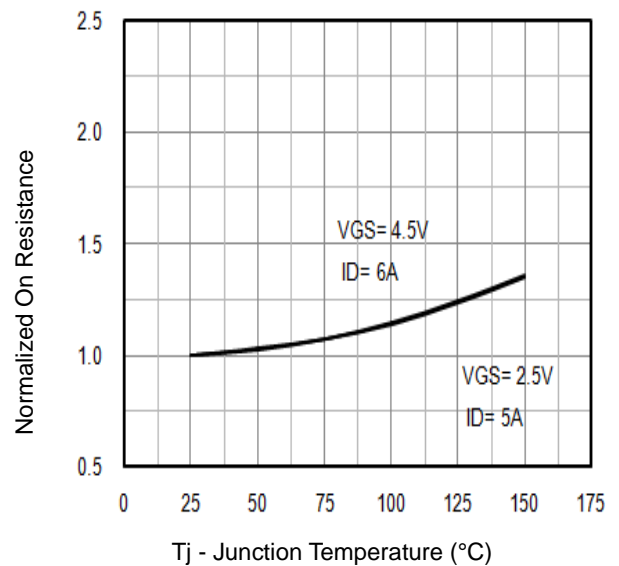


Fig4. Normalized On-Resistance Vs. Temperature

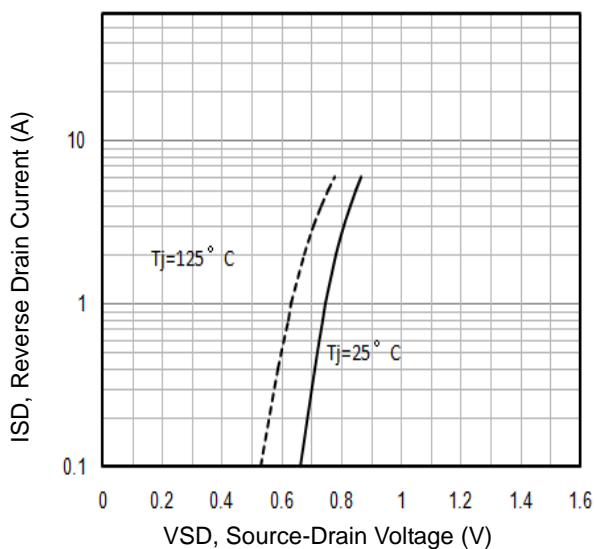


Fig5. Typical Source-Drain Diode Forward Voltage

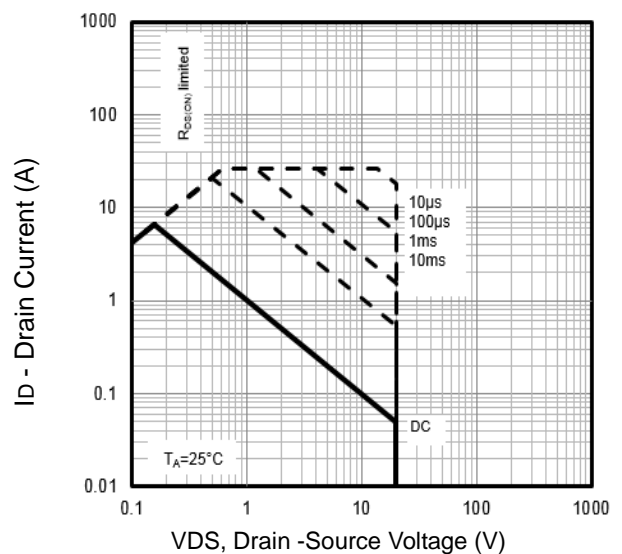


Fig6. Maximum Safe Operating Area

Typical Characteristics

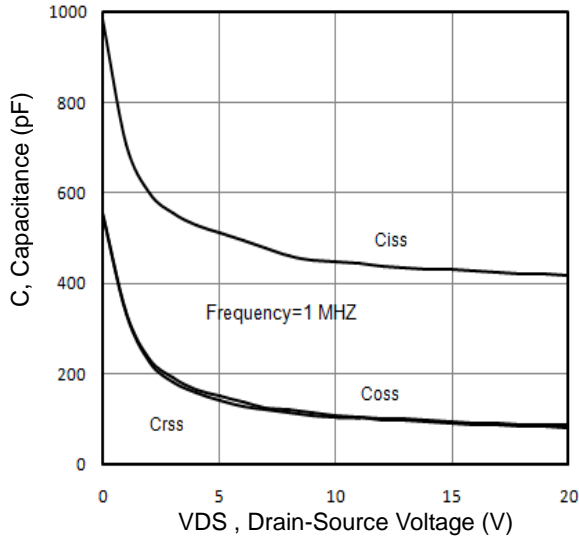


Fig7. Typical Capacitance Vs.Drain-Source Voltage

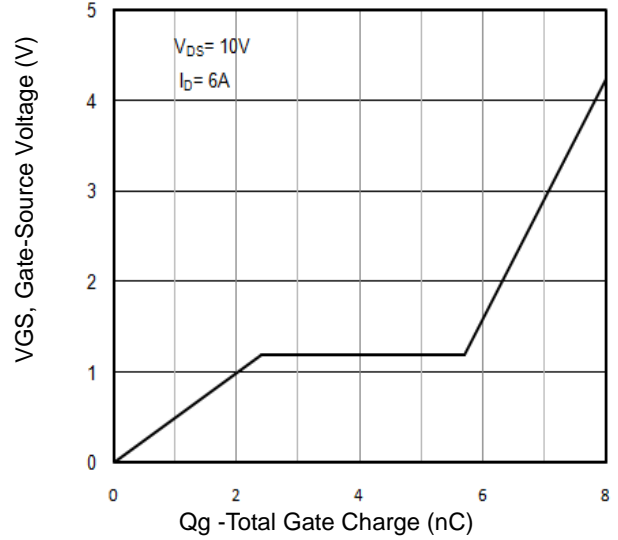


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

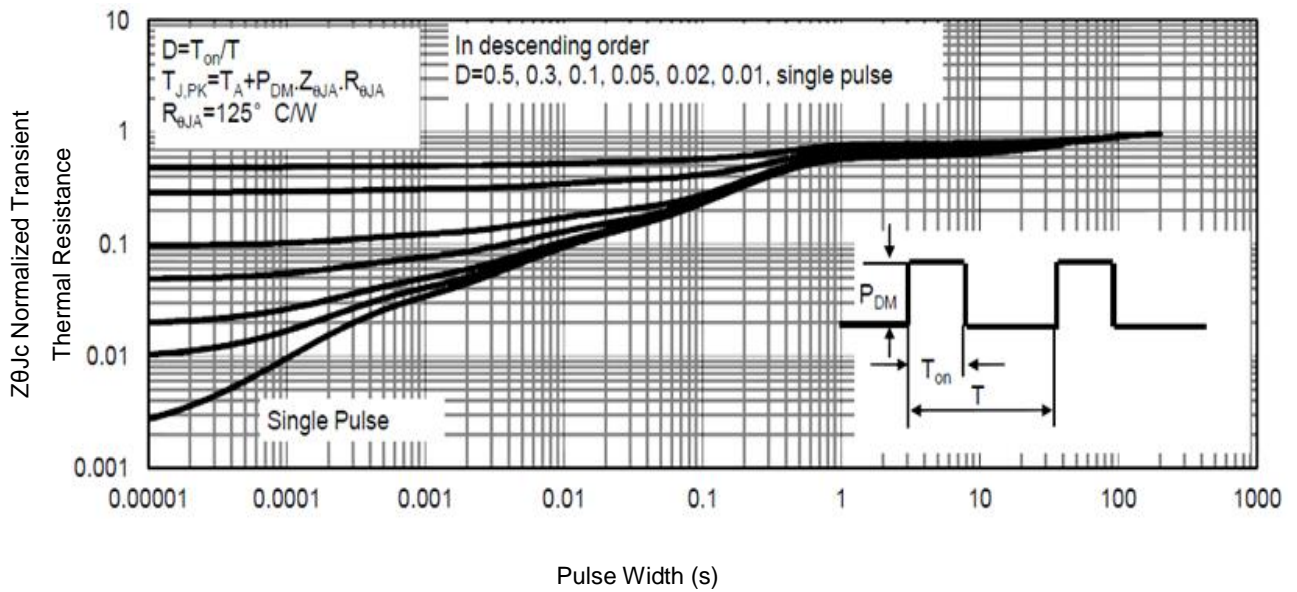


Fig9 . Normalized Maximum Transient Thermal Impedance

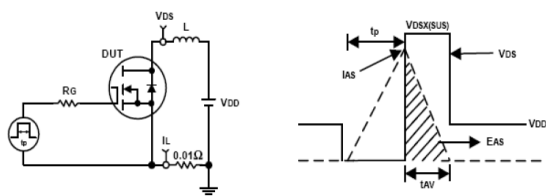


Fig10. Unclamped Inductive Test Circuit and waveforms

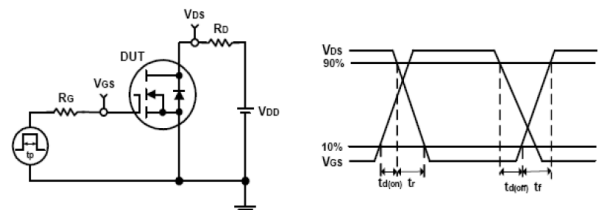
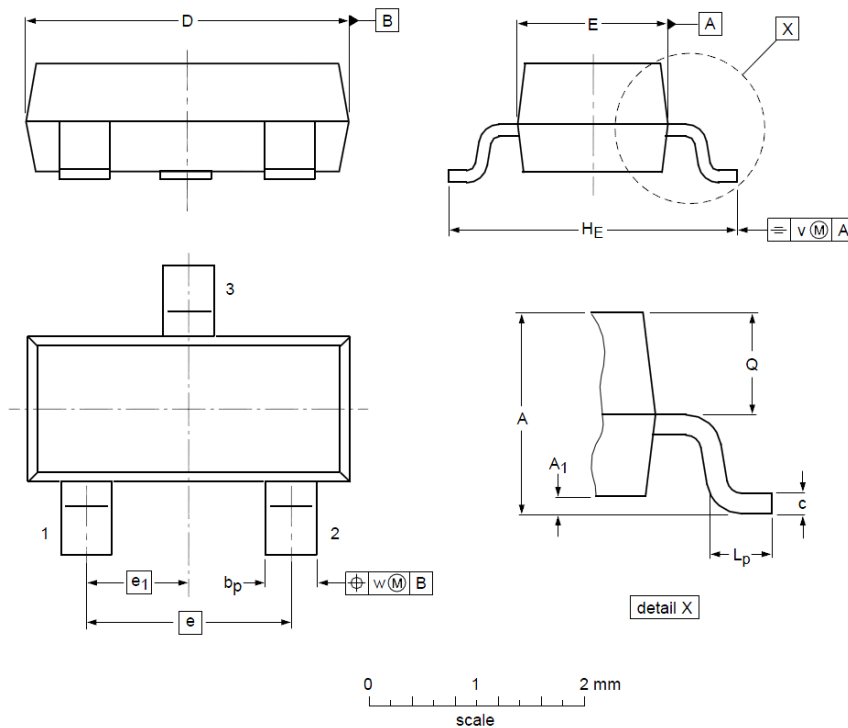


Fig11. Switching Time Test Circuit and waveforms

SOT23 Package Outline Data



Label	DIMENSIONS (unit: mm)		
	Min	Typ	Max
A	0.90	1.03	1.10
A₁	0.01	0.05	0.10
b_p	0.38	0.42	0.48
c	0.09	0.13	0.15
D	2.80	2.92	3.00
E	1.20	1.33	1.40
e	--	1.90	--
e₁	--	0.95	--
H_E	2.10	2.40	2.50
L_p	0.40	0.50	0.60
Q	0.45	0.49	0.55
v	--	0.20	--
w	--	0.10	--

Notes:

1. Follow JEDEC TO-236, variation AB.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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