Vanguard
Semiconductor

VS3506AP

-30V/-75A P-Channel Advanced Power MOSFET

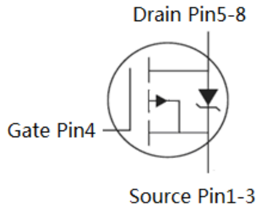
Features

- P-Channel，-5V Logic Level Control
- Low on-resistance RDS(on) @ V_{GS}=-4.5 V
- Fast Switching
- Enhancement mode
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant

Pb-Free RoHS HF Halogen-Free

V_{DS}	-30	V
$R_{DS(on),TYP}$@ V_{GS}=-10 V	5.3	mΩ
$R_{DS(on),TYP}$@ V_{GS}=-4.5V	8.4	mΩ
I_D	-75	A

PDFN5x6



Part ID	Package Type	Marking	Tape and reel information
VS3506AP	PDFN5x6	3506AP	3000pcs/reel

Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	**Parameter**		**Rating**	**Unit**
$V_{(BR)DSS}$	Drain-Source breakdown voltage		-30	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C=25°C	-75	A
I_D	Continuous drain current @VGS=-10V	T_C=25°C	-75	A
		T_C=100°C	-47	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	-300	A
I_{DM}	Pulse drain current tested	T_A=25°C	-23	A
		T_A=70°C	-18	A
EAS	Avalanche energy, single pulsed ②		122	mJ
P_D	Maximum power dissipation	T_C=25°C	45	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	4.2	W
T_{STG} T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	**Parameter**	**Typical**	**Unit**
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.8	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	30	°C/W

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ TJ = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V, ID=-250μA	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	VDS=-30V,VGS=0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(Tc=125℃)	VDS=-30V,VGS=0V	--	--	-100	μA
I_{GSS}	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-1.2	-1.6	-2.3	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ④	VGS=-10V, ID=-20A	--	5.3	8	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance ④	VGS=-4.5V, ID=-20A	--	8.4	13	mΩ
Dynamic Electrical Characteristics @ TJ = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	VDS=-15V,VGS=0V, f=1MHz	3000	3770	4500	pF
C_{oss}	Output Capacitance		300	545	750	pF
C_{rss}	Reverse Transfer Capacitance		250	395	550	pF
R_g	Gate Resistance	f=1MHz	--	5.6	--	Ω
Q_g	Total Gate Charge	VDS=-15V,ID=-20A, VGS=-10V	--	65	--	nC
Q_{gs}	Gate-Source Charge		--	16.1	--	nC
Q_{gd}	Gate-Drain Charge		--	18.1	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	VDD=-15V, ID=-20A, RG=3Ω, VGS=-10V	--	14.4	--	nS
t_r	Turn-on Rise Time		--	11.2	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	99.5	--	nS
t_f	Turn-Off Fall Time		--	47.5	--	nS
Source- Drain Diode Characteristics @ TJ = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	ISD=-20A,VGS=0V	--	-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	Tj=25℃,Isd=-20A, VGS=0V di/dt=-100A/μs	--	37	--	nS
Q_{rr}	Reverse Recovery Charge			35		nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -18A, V_{GS} =-10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

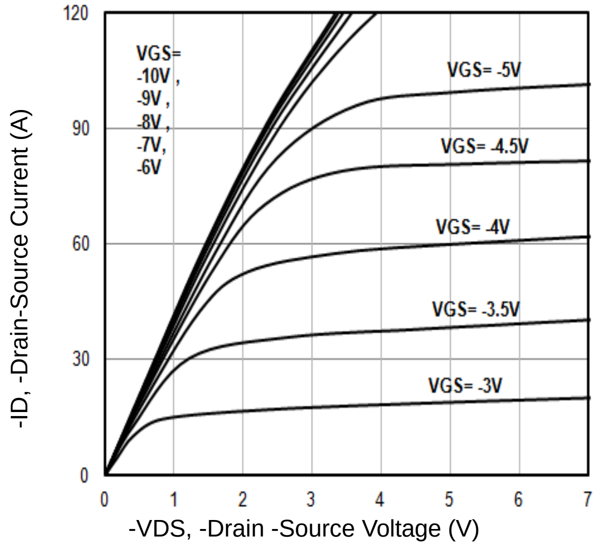


Fig1. Typical Output Characteristics

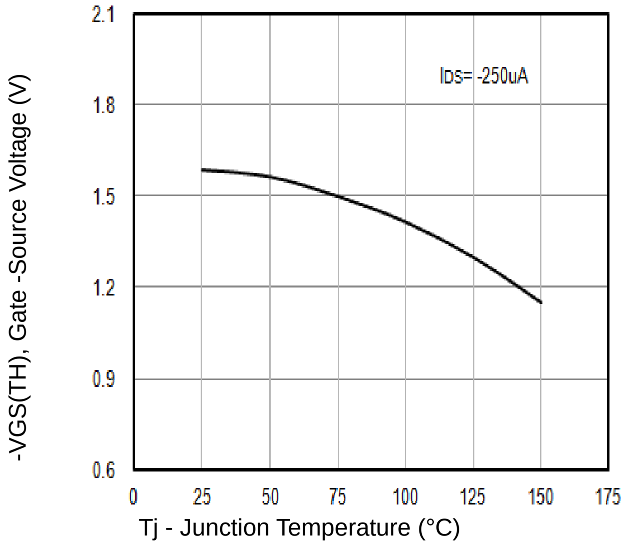


Fig2. -$V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

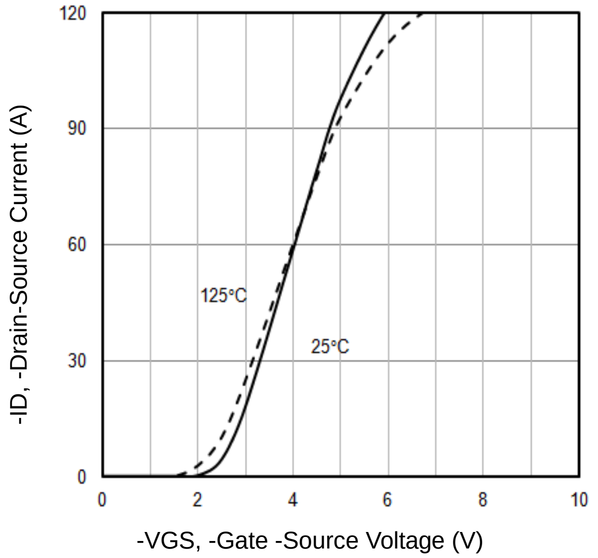


Fig3. Typical Transfer Characteristics

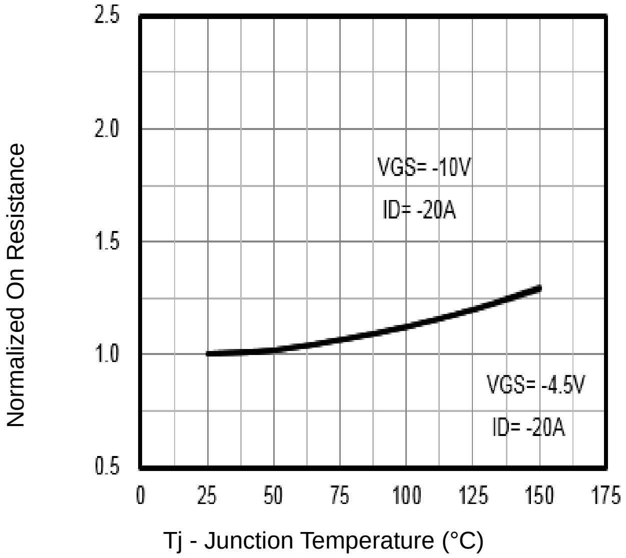


Fig4. Normalized On-Resistance Vs. Tj

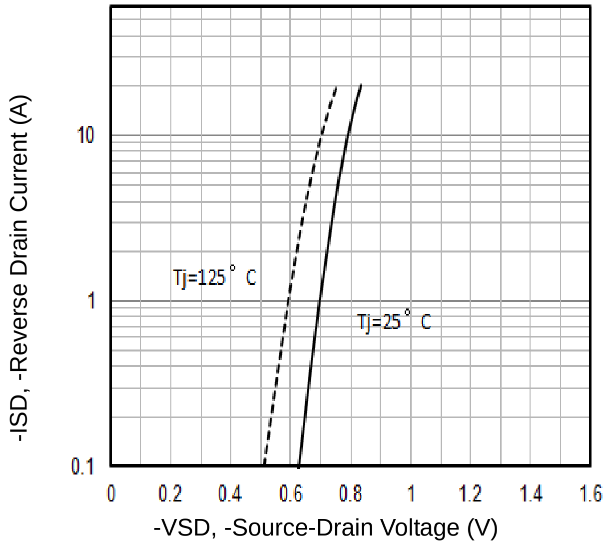


Fig5. Typical Source-Drain Diode Forward Voltage

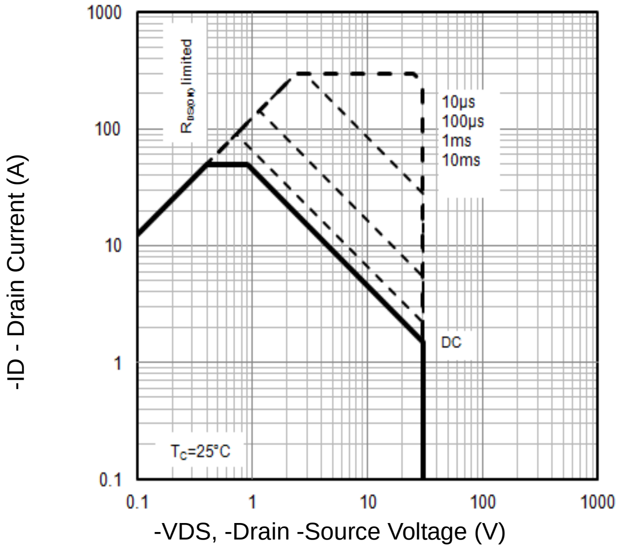


Fig6. Maximum Safe Operating Area

Typical Characteristics

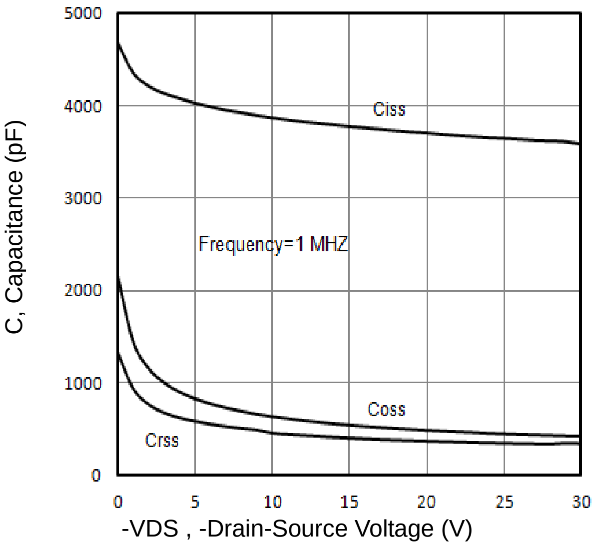


Fig7. Typical Capacitance Vs.Drain-Source Voltage

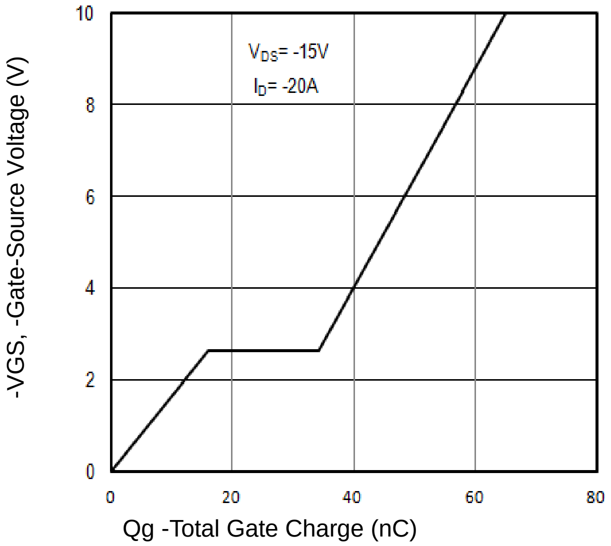


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

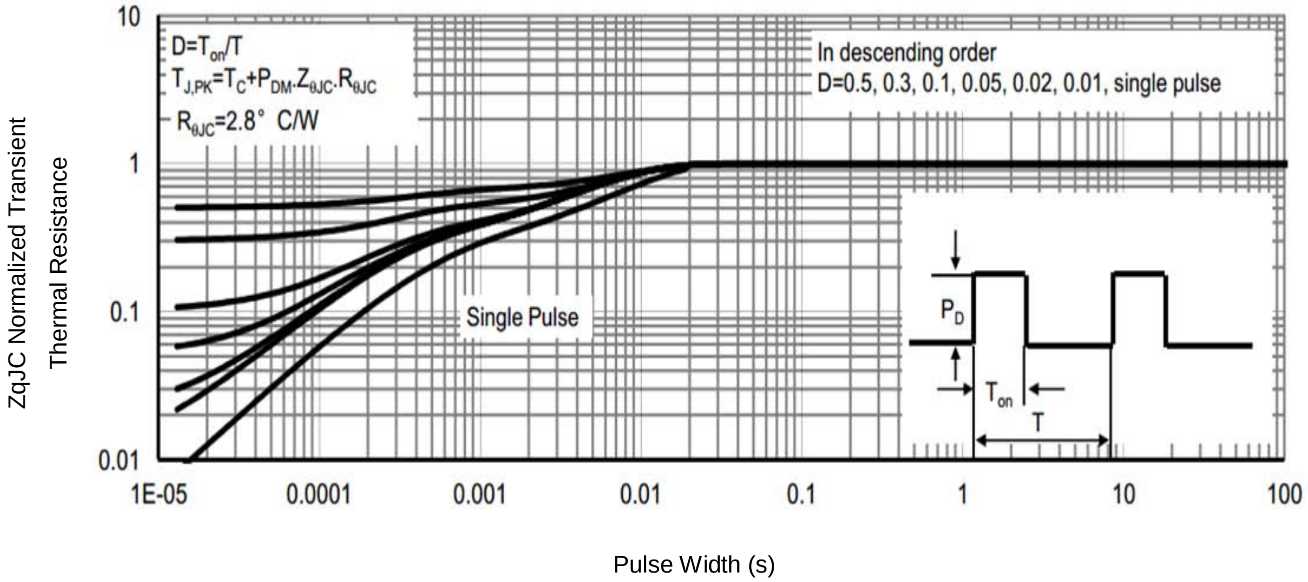


Fig9. Normalized Maximum Transient Thermal Impedance

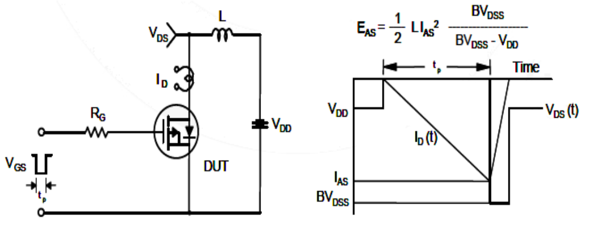


Fig10. Unclamped Inductive Test Circuit and Waveforms

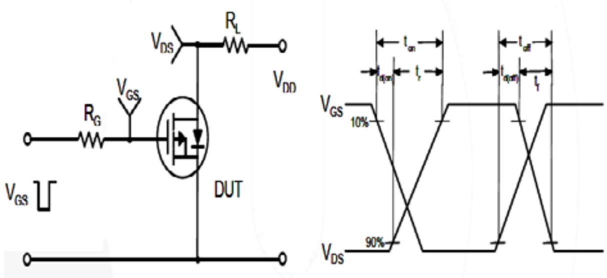
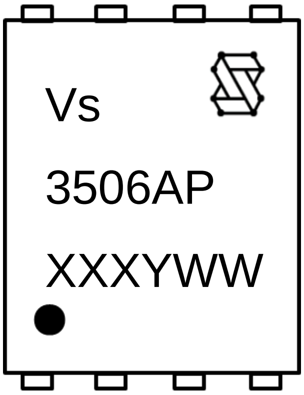


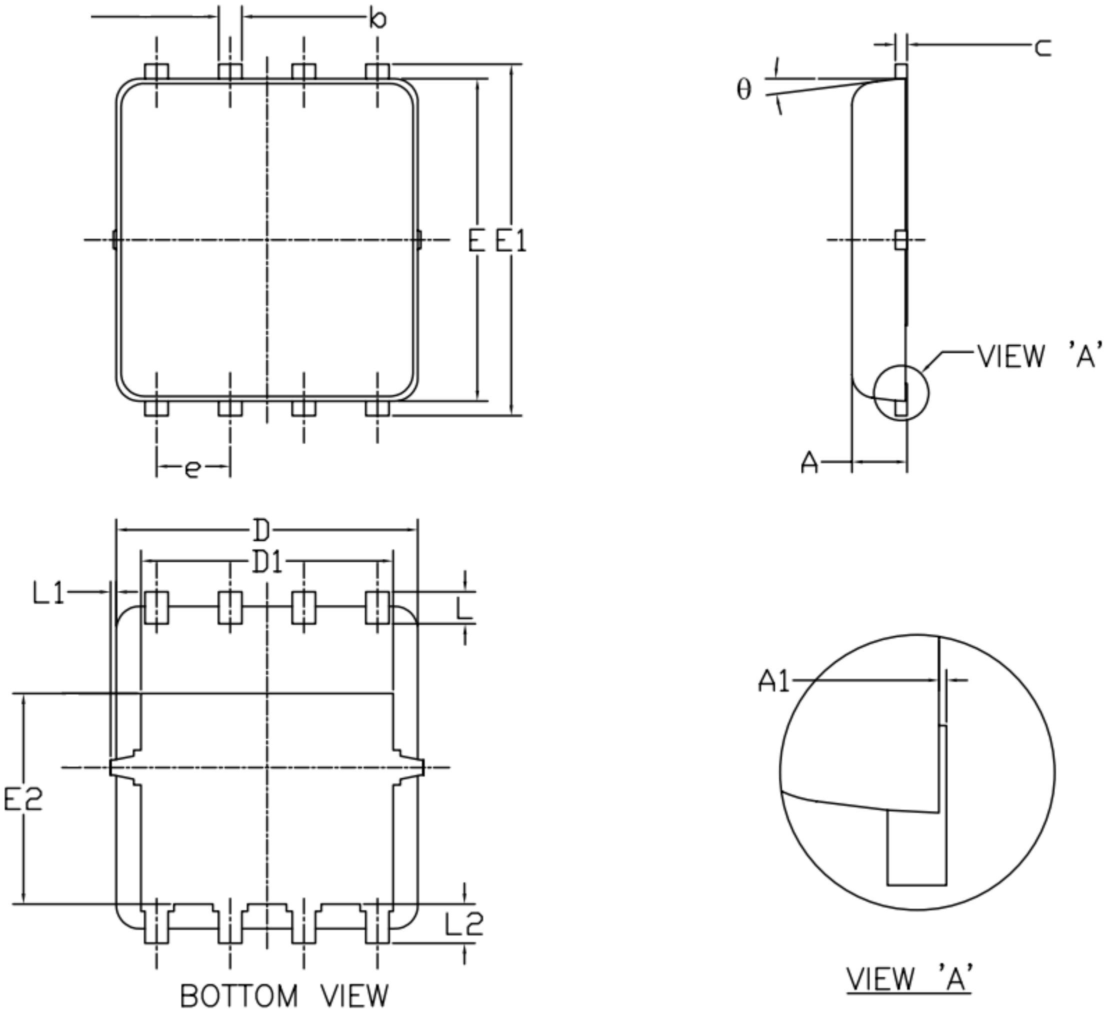
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line： Company Code（Vs）， Company Logo
2nd line： Part Number（3506AP）
3rd line： Date code （XXXYWW）
XXX： Wafer Lot Number
Y： Year Code， e.g. E means 2017
WW： Week Code

PDFN5x6 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	**Typ**	**Max**
A	0.90	1.00	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.51
c	0.20	0.25	0.33
D	4.80	4.90	5.40
D1	3.61	4.00	4.25
E	5.65	5.80	6.06
E1	5.90	6.10	6.35
E2	3.38	3.58	3.92
e	1.27 BSC		
L	0.51	0.61	0.71
L1	--	--	0.15
L2	0.41	0.51	0.61
θ	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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