

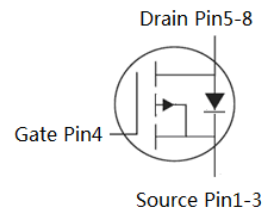
Features

- P-Channel, -5V Logic Level Control
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=-4.5V$
- Fast Switching
- Enhancement mode
- Pb-free lead plating; RoHS compliant


Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VS3508AS	SOP8	3508AS	3000pcs/Reel

V_{DS}	-30	V
$R_{DS(on),TYP@ V_{GS}=-10V}$	8.5	mΩ
$R_{DS(on),TYP@ V_{GS}=-4.5V}$	15	mΩ
I_D	-13	A



Maximum ratings, at $T_A=25^{\circ}C$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		-30	V
I_S	Diode continuous forward current	$T_A=25^{\circ}C$	-3	A
I_D	Continuous drain current@ $V_{GS}=-10V$	$T_A=25^{\circ}C$	-13	A
		$T_A=100^{\circ}C$	-8.5	A
I_{DM}	Pulse drain current tested ①	$T_A=25^{\circ}C$	-52	A
EAS	Avalanche energy, single pulsed ②		81	mJ
P_D	Maximum power dissipation	$T_A=25^{\circ}C$	3.1	W
V_{GS}	Gate-Source voltage		± 20	V
MSL			Level 3	
$T_{STG} T_J$	Storage and operating temperature range		-55 to 150	$^{\circ}C$

Thermal Characteristics

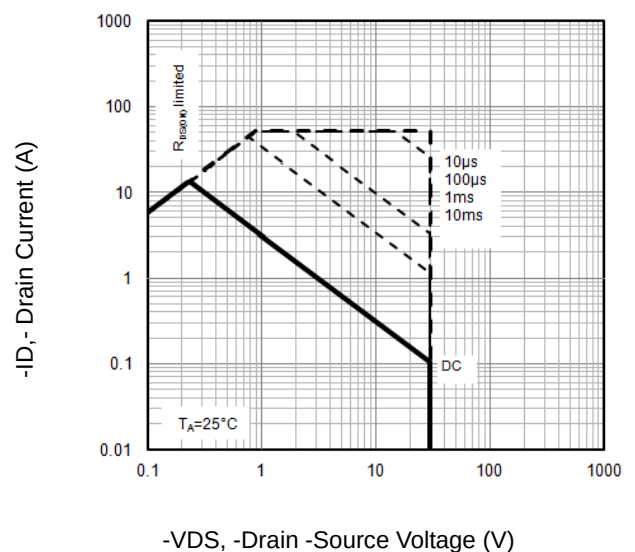
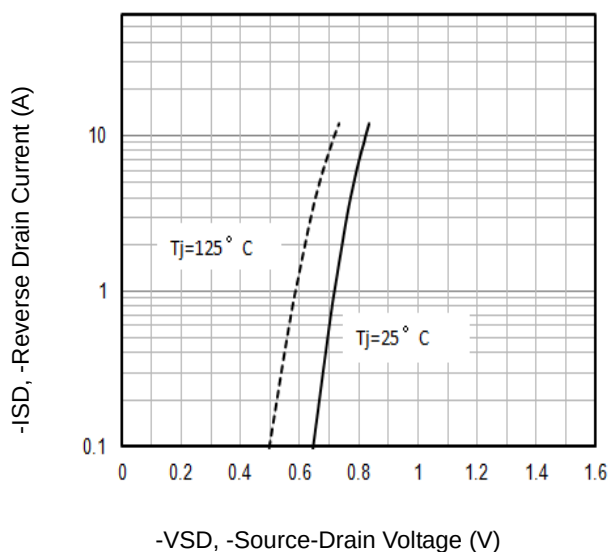
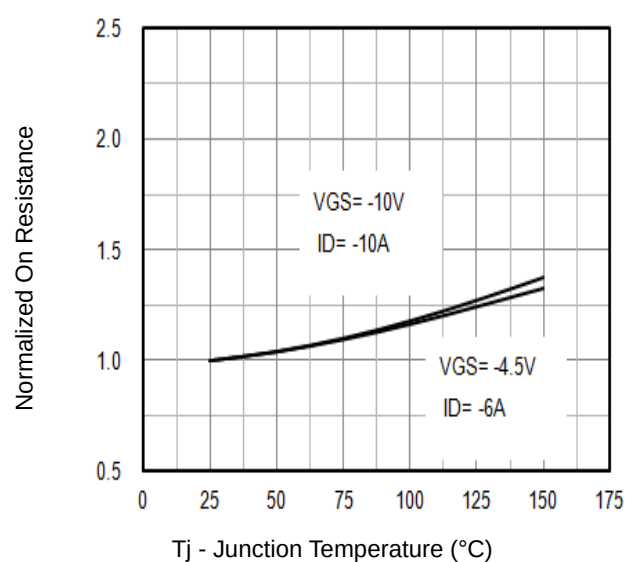
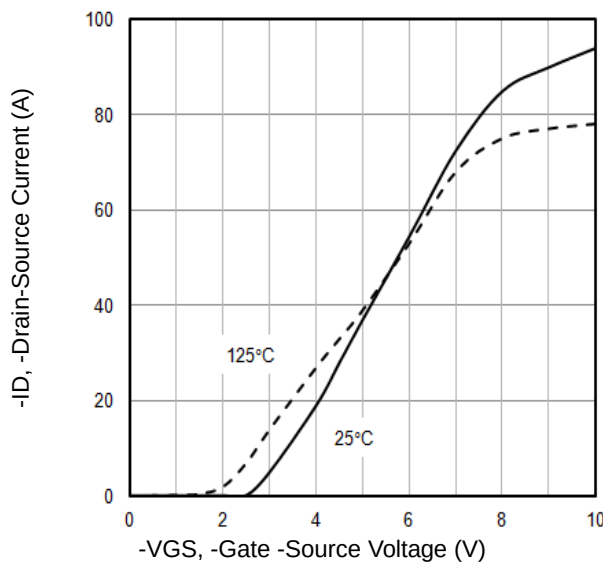
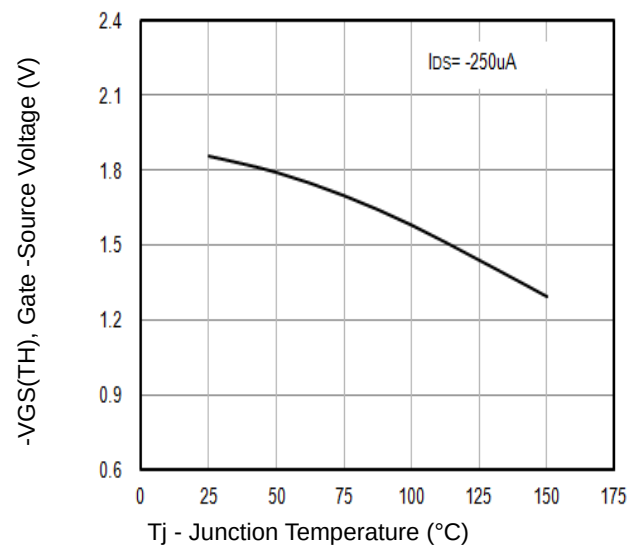
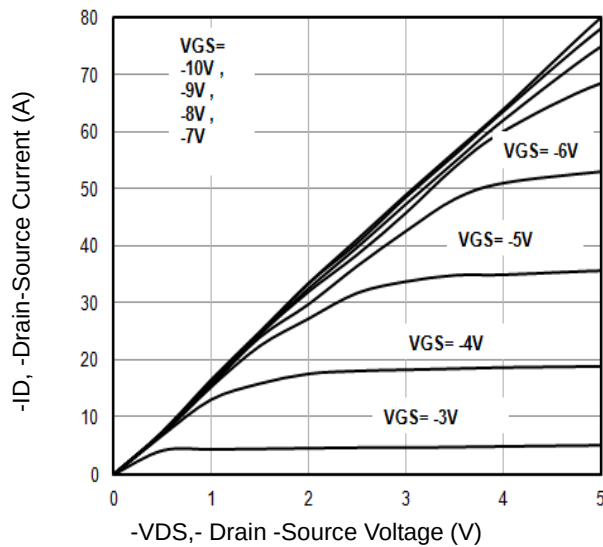
Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	24	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	40	$^{\circ}C/W$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =-250μA	-30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V,V _{GS} =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =-30V,V _{GS} =0V	--	--	-100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =-250μA	-1.0	-1.8	-2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ②	V _{GS} =-10V, I _D =-10A	--	8.5	10	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ②	V _{GS} =-4.5V, I _D =-6A	--	15	18	mΩ
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-15V,V _{GS} =0V, f=1MHz	--	3320	--	pF
C _{oss}	Output Capacitance		--	395	--	pF
C _{rss}	Reverse Transfer Capacitance		--	245	--	pF
R _g	Gate Resistance	f=1MHz	--	2.3	--	Ω
Q _g	Total Gate Charge	V _{DS} =-15V,I _D =-10A, V _{GS} =-10V	--	39	--	nC
Q _{gs}	Gate-Source Charge		--	7	--	nC
Q _{gd}	Gate-Drain Charge		--	11	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-15V, I _D =-10A, R _G =6.8Ω, V _{GS} =-10V	--	15	--	nS
t _r	Turn-on Rise Time		--	33	--	nS
t _{d(off)}	Turn-Off Delay Time		--	67	--	nS
t _f	Turn-Off Fall Time		--	21	--	nS
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =-10A,V _{GS} =0V	--	-0.83	-1.2	V
t _{rr}	Reverse Recovery Time	T _j =25 °C,I _{sd} =-10A, V _{GS} =0V	--	29	--	nS
Q _{rr}	Reverse Recovery Charge	di/dt=-100A/μs		144		nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{jmax}, starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -18A, V_{GS} = -10V. Part not recommended for use above this value
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics



Typical Characteristics

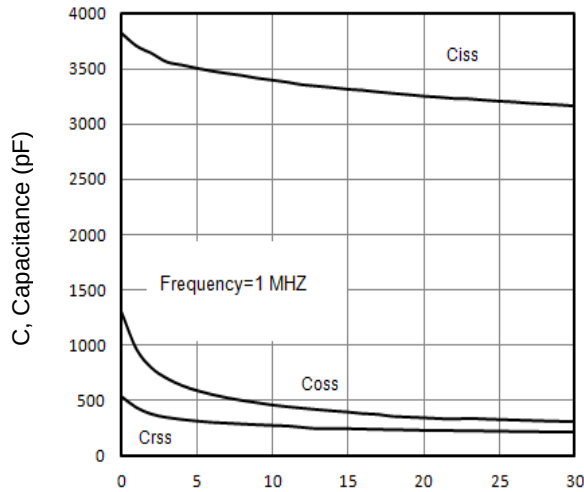


Fig7. Typical Capacitance Vs. Drain-Source Voltage

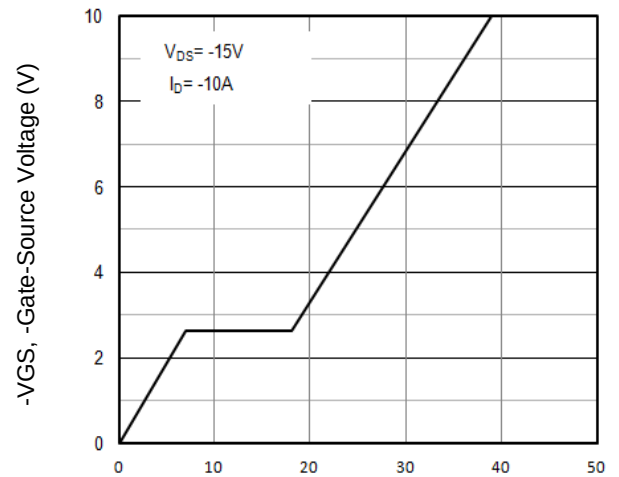


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

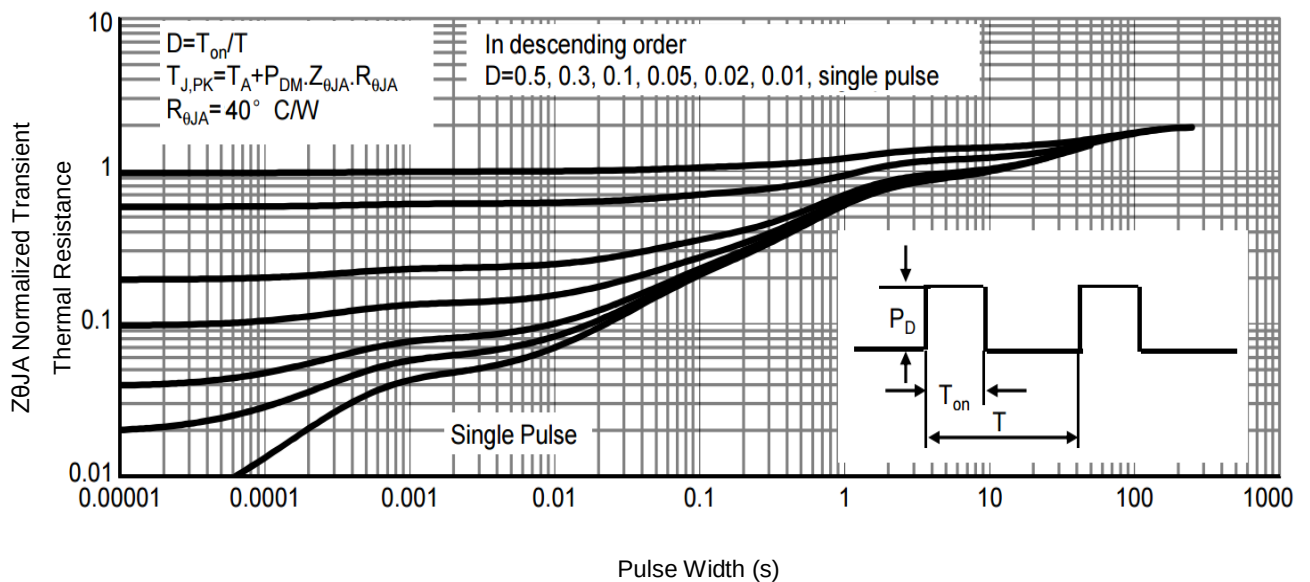


Fig9. Normalized Maximum Transient Thermal Impedance

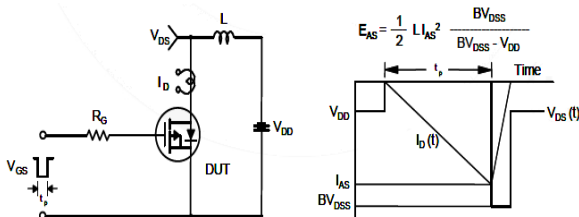


Fig10. Unclamped Inductive Test Circuit and Waveforms

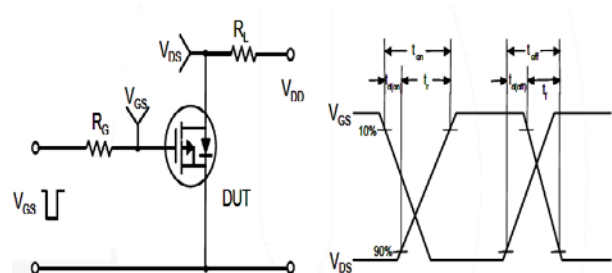
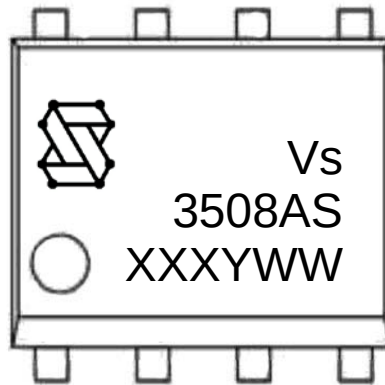


Fig11. Switching Time Test Circuit and waveforms

Marking Information

1st line: Company Code (Vs), Company Logo

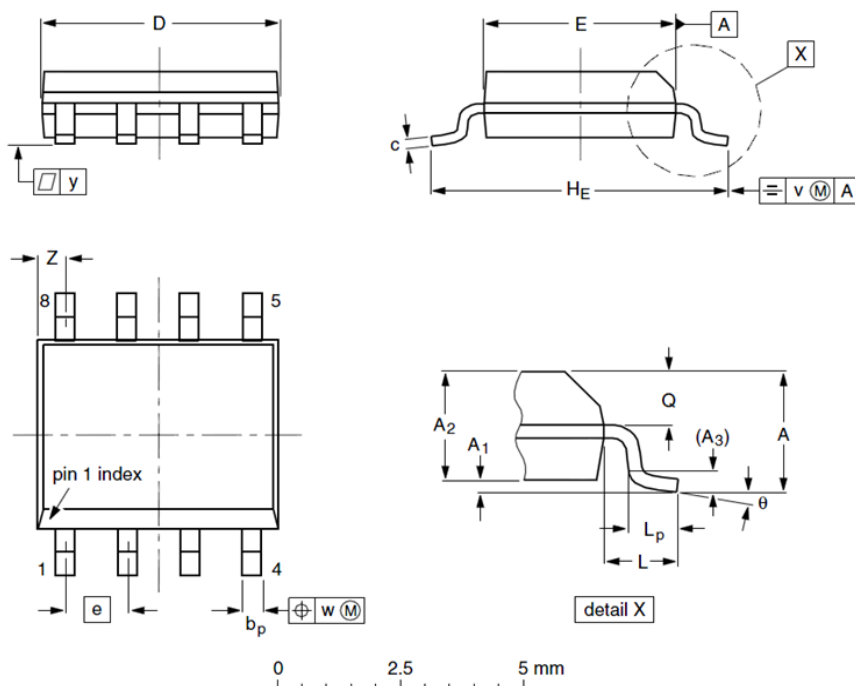
2nd line: Part Number (3508AS)

3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number

Y: Year Code, e.g. E means 2017

WW: Week Code

SOP8 Package Outline Data


Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A ₁	0.10	0.18	0.25
A ₂	1.25	1.35	1.50
A ₃	--	0.25	--
b _p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H _E	5.80	6.00	6.20
L	--	1.05	--
L _p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "b_p" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "b_p" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Customer Service
Sales and Service:
sales@vgsemi.com
Vanguard Semiconductor CO., LTD
TEL: (86-755) -26902410

FAX: (86-755) -26907027

WEB: www.vgsemi.com