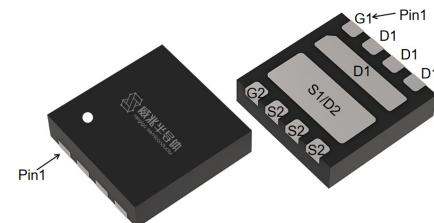


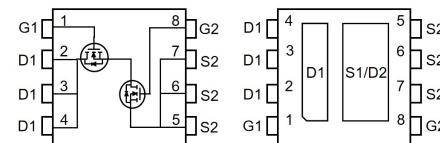
Features

- Dual Asymmetric N-Channel
- VitoMOS® II Technology
- 100% Avalanche Tested, 100% R_g Tested

V_{DS}	30	30	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	6.6	4.5	mΩ
$R_{DS(on),TYP} @ V_{GS}=4.5\text{ V}$	10	7	mΩ
I_D (Wire bond Limited)	24	36	A

DFN3x3

Halogen-Free

Part ID	Package Type	Marking	Packing
VS3625DB	DFN3x3	3625DB	5000pcs/Reel



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating		Unit
		Q1	Q2	
V(BR)DSS	Drain-Source breakdown voltage	30	30	V
V _{GS}	Gate-Source voltage	±20	±20	V
I _S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	8.3	A
I _D	Continuous drain current @ $V_{GS}=10\text{V}$ (Wire bond Limited)	$T_C = 25^\circ\text{C}$	24	A
	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon Limited)	$T_C = 100^\circ\text{C}$	17	A
I _{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	108	A
I _{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	12	A
		$T_A = 70^\circ\text{C}$	9	A
EAS	Avalanche energy, single pulsed ②	42	56	mJ
P _D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$	10	W
P _{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$	1.7	W
T _{STG,TJ}	Storage and Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical		Max		Unit
		Q1	Q2	Q1	Q2	
R _{θJC}	Thermal Resistance, Junction-to-Case ⑤	11	5.3	13	6.4	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient ⑥	60	50	72	60	°C/W

Q1-Channel Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	30	--	--	V
IDSS	Zero Gate Voltage Drain Current($T_J=25^\circ\text{C}$)	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_J=125^\circ\text{C}$) ^⑦	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$	--	--	100	μA
IGSS	Gate-Body Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	1.4	2.0	V
RDS(on)	Drain-Source On-State Resistance ^⑧	$V_{GS}=10\text{V}, I_D=13\text{A}$	--	6.6	8.6	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=10\text{A}$	--	10	13	$\text{m}\Omega$
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
Ciss	Input Capacitance ^⑦	$V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	--	605	--	pF
Coss	Output Capacitance ^⑦		--	495	--	pF
Crss	Reverse Transfer Capacitance ^⑦		--	60	--	pF
Rg	Gate Resistance	f=1MHz	--	1.8	--	Ω
Qg(10V)	Total Gate Charge ^⑦	$V_{DS}=15\text{V}, I_D=13\text{A}, V_{GS}=10\text{V}$	--	12	--	nC
Qg(4.5V)	Total Gate Charge ^⑦		--	6.2	--	nC
Qgs	Gate Source Charge ^⑦		--	1.7	--	nC
Qgd	Gate Drain Charge ^⑦		--	2.5	--	nC
Switching Characteristics ^⑦						
Td(on)	Turn on Delay Time	$V_{DD}=15\text{V}, I_D=13\text{A}, R_G=3\Omega, V_{GS}=10\text{V}$	--	5	--	ns
Tr	Turn on Rise Time		--	39	--	ns
Td(off)	Turn Off Delay Time		-	14	--	ns
Tf	Turn Off Fall Time		--	6.8	--	ns
Source Drain Diode Characteristics						
VSD	Forward on voltage	$I_{SD}=13\text{A}, V_{GS}=0\text{V}$	--	0.8	1.2	V
Trr	Reverse Recovery Time ^⑦	$V_{DD}=15\text{V}, I_{SD}=13\text{A}, V_{GS}=0\text{V}$ $di/dt=100\text{A}/\mu\text{s}$	--	16	--	ns
Qrr	Reverse Recovery Charge ^⑦		--	3.7	--	nC

NOTE:

- ① Single pulse; pulse width $\leq 100\mu\text{s}$.
- ② Q1: EAS of 42mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 13\text{A}$, $V_{GS}=10\text{V}$; 100% FT tested at $L = 0.5\text{mH}$, $I_{AS} = 7\text{A}$.
Q2: EAS of 56mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 15\text{A}$, $V_{GS}=10\text{V}$; 100% FT tested at $L = 0.5\text{mH}$, $I_{AS} = 8\text{A}$.
- ③ The power dissipation P_d is based on $T_{j(max)}$, using junction-to-case thermal resistance $R_{\theta JC}$.
- ④ The power dissipation P_{dsm} is based on $T_{j(max)}$, using junction-to-ambient thermal resistance $R_{\theta JA}$.
- ⑤ These tests are performed respectively with the device mounted on a 1 in2 pad and a minimum pad of 2oz. Copper FR-4 board in a still air environment with $TA=25^\circ\text{C}$, using Transient Dual Interface method to acquire $R_{\theta JC}$.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with $TA=25^\circ\text{C}$.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width $\leq 380\mu\text{s}$; duty cycles $\leq 2\%$.

Q2-Channel Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	--	--	V
IDSS	Zero Gate Voltage Drain Current $t(T_J=25^\circ\text{C})$	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1	μA
	Zero Gate Voltage Drain Current $t(T_J=125^\circ\text{C})$ ^⑦	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}$	--	--	100	μA
IGSS	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	--	--	± 100	nA
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0	1.5	2.1	V
RDS(on)	Drain-Source On-State Resistance ^⑧	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=15\text{A}$	--	4.5	5.9	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=10\text{A}$	--	7	9.1	$\text{m}\Omega$
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
Ciss	Input Capacitance ^⑦	$V_{\text{DS}}=15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	--	825	--	pF
Coss	Output Capacitance ^⑦		--	485	--	pF
Crss	Reverse Transfer Capacitance ^⑦		--	70	--	pF
Rg	Gate Resistance	f=1MHz	--	2.5	--	Ω
Qg(10V)	Total Gate Charge ^⑦	$V_{\text{DS}}=15\text{V}, I_{\text{D}}=15\text{A}, V_{\text{GS}}=10\text{V}$	--	16	--	nC
Qg(4.5V)	Total Gate Charge ^⑦		--	8	--	nC
Qgs	Gate Source Charge ^⑦		--	2.3	--	nC
Qgd	Gate Drain Charge ^⑦		--	3.2	--	nC
Switching Characteristics ^⑦						
Td(on)	Turn on Delay Time	$V_{\text{DD}}=15\text{V}, I_{\text{D}}=15\text{A}, R_{\text{G}}=3\Omega, V_{\text{GS}}=10\text{V}$	--	5.2	--	ns
Tr	Turn on Rise Time		--	44	--	ns
Td(off)	Turn Off Delay Time		-	17	--	ns
Tf	Turn Off Fall Time		--	11	--	ns
Source Drain Diode Characteristics						
VSD	Forward on voltage	$I_{\text{SD}}=15\text{A}, V_{\text{GS}}=0\text{V}$	--	0.8	1.2	V
Trr	Reverse Recovery Time ^⑦	$V_{\text{DD}}=15\text{V}, I_{\text{SD}}=15\text{A}, V_{\text{GS}}=0\text{V}$	--	16	--	ns
Qrr	Reverse Recovery Charge ^⑦		--	5.2	--	nC

NOTE:

① Single pulse; pulse width $\leq 100\mu\text{s}$.

② Q1: EAS of 42mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{\text{AS}} = 13\text{A}$, $V_{\text{GS}} = 10\text{V}$: 100% FT tested at $L = 0.5\text{mH}$, $I_{\text{AS}} = 7\text{A}$.

Q2: EAS of 56mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{\text{AS}} = 15\text{A}$, $V_{\text{GS}} = 10\text{V}$: 100% FT tested at $L = 0.5\text{mH}$, $I_{\text{AS}} = 8\text{A}$.

③ The power dissipation P_d is based on $T_{\text{j(max)}}$, using junction-to-case thermal resistance $R_{\theta\text{JC}}$.

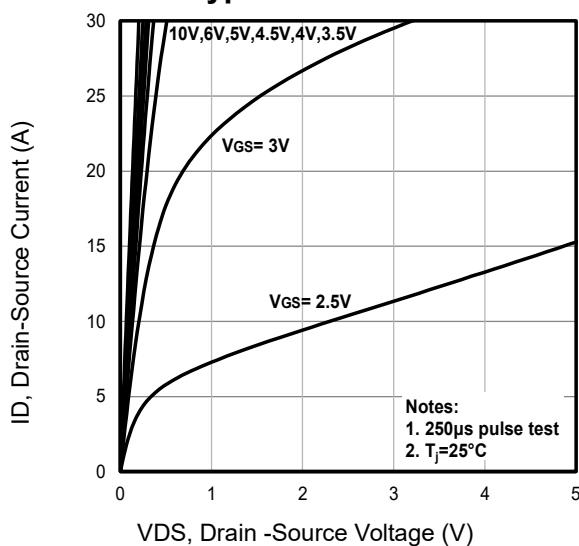
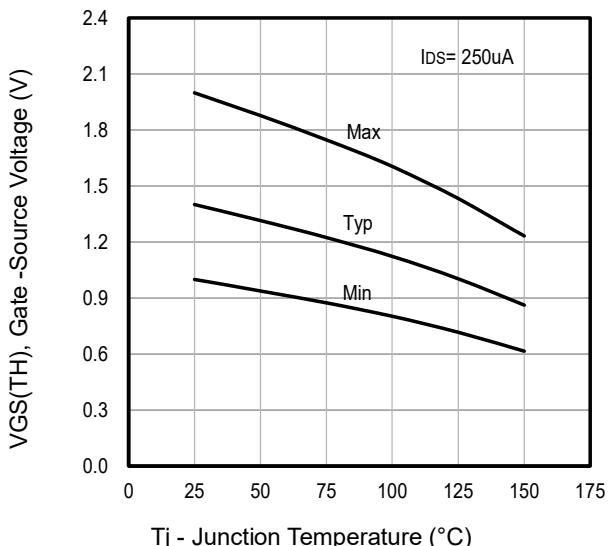
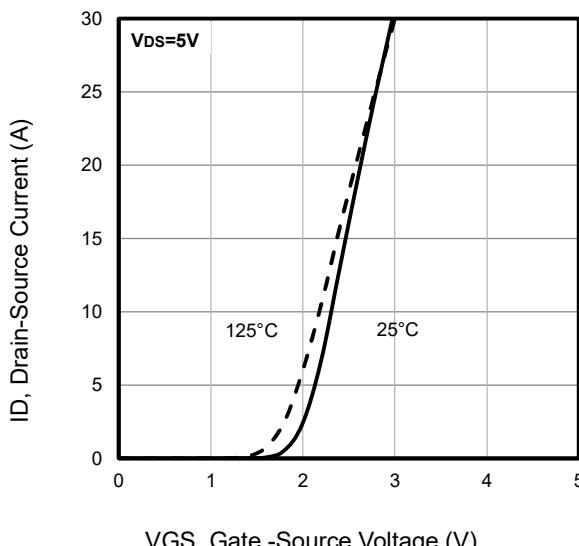
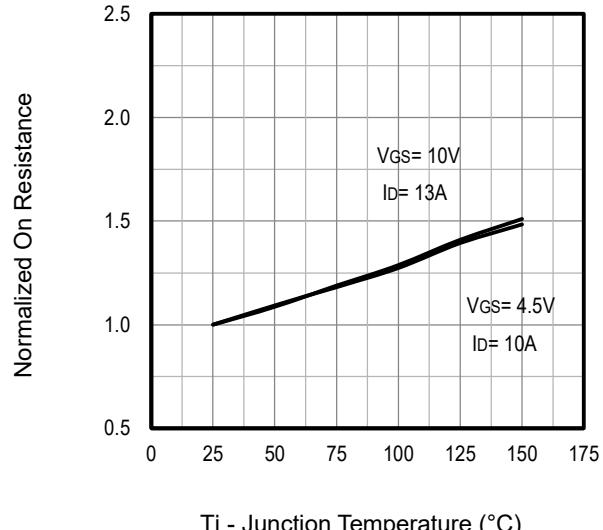
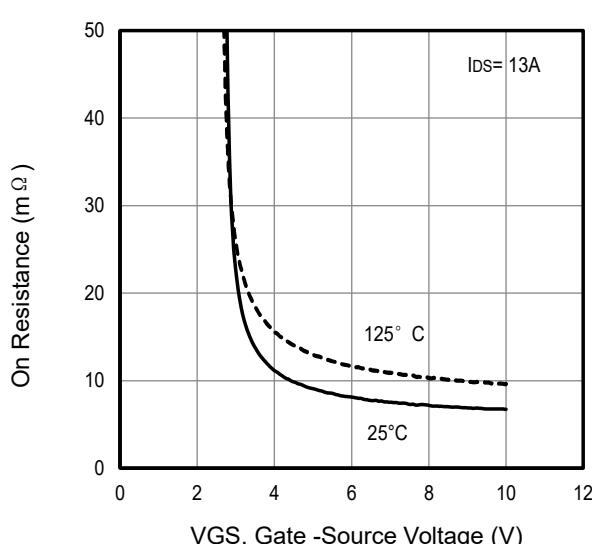
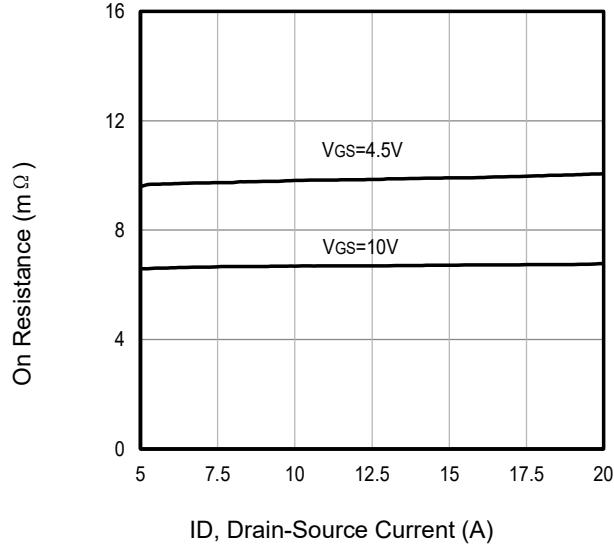
④ The power dissipation P_{dsm} is based on $T_{\text{j(max)}}$, using junction-to-ambient thermal resistance $R_{\theta\text{JA}}$.

⑤ These tests are performed respectively with the device mounted on a 1 in2 pad and a minimum pad of 2oz. Copper FR-4 board in a still air environment with $TA=25^\circ\text{C}$, using Transient Dual Interface method to acquire $R_{\theta\text{JC}}$.

⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with $TA=25^\circ\text{C}$.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width $\leq 380\mu\text{s}$; duty cycle $\leq 2\%$.

Q1-Channel Typical Characteristics

Fig1. Typical Output Characteristics

Fig2. Typical $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

Fig3. Typical Transfer Characteristics

Fig4. Typical Normalized On-Resistance Vs. T_j

Fig5. Typical On Resistance Vs Gate-Source Voltage

Fig6. Typical On Resistance Vs Drain Current

Q1-Channel Typical Characteristics

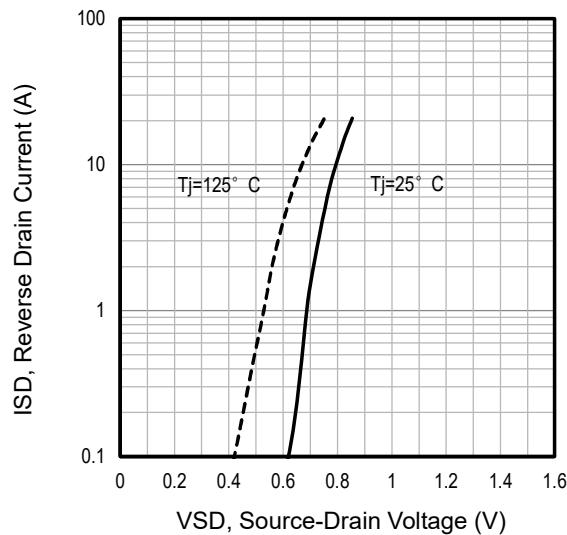


Fig7. Typical Source-Drain Diode Forward Voltage

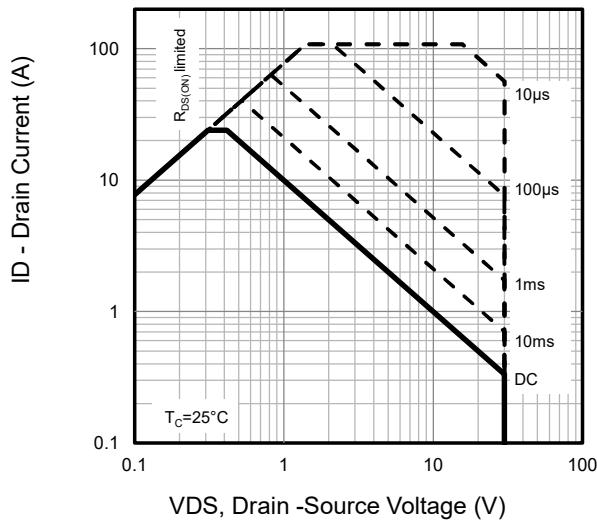


Fig8. Maximum Safe Operating Area

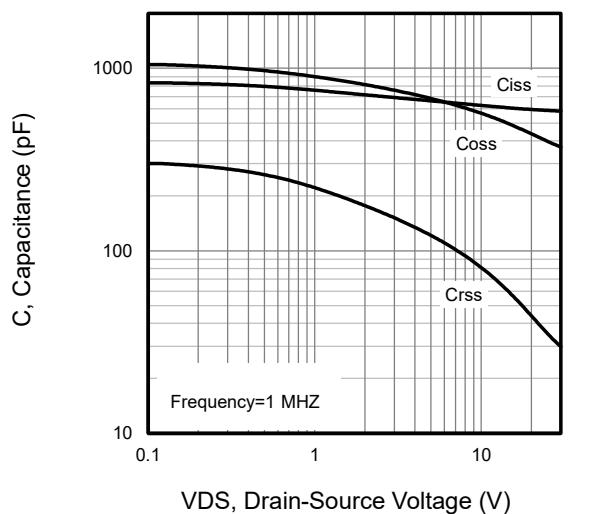


Fig9. Typical Capacitance Vs. Drain-Source Voltage

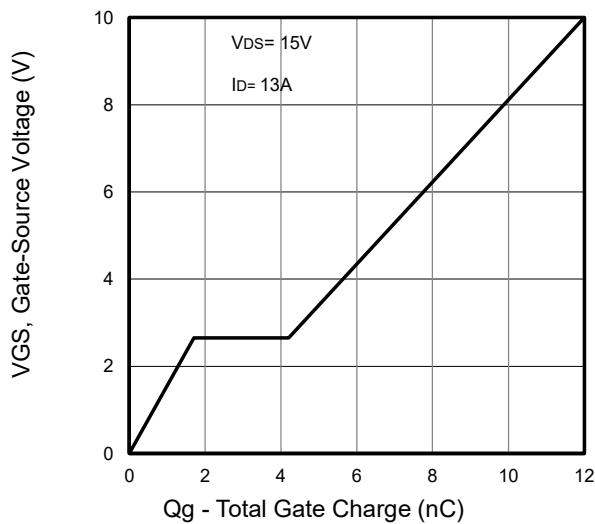


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

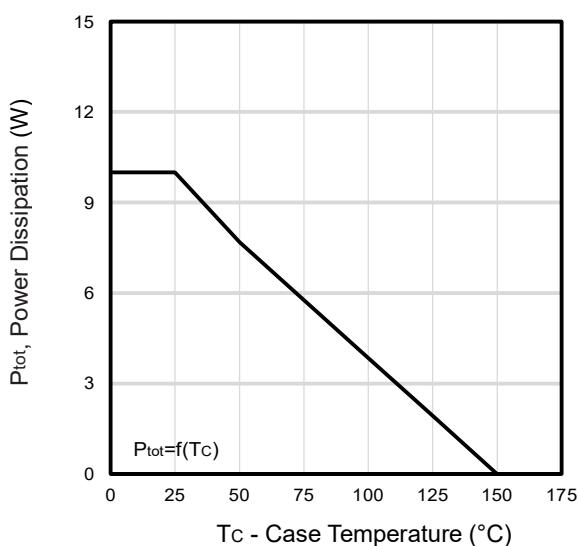


Fig11. Power Dissipation Vs. Case Temperature

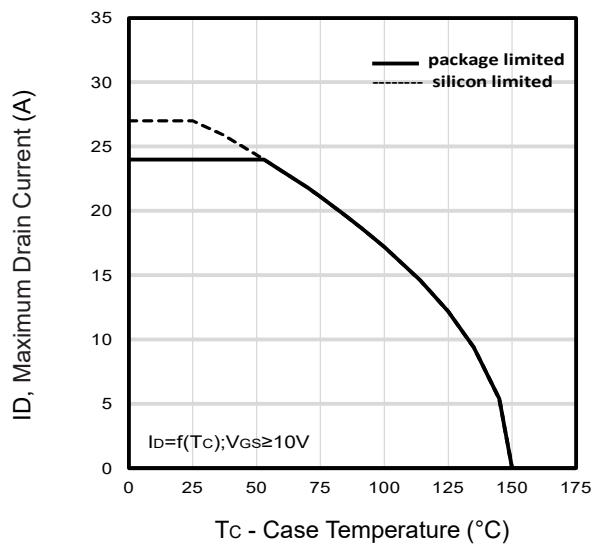


Fig12. Maximum Drain Current Vs. Case Temperature

Q1-Channel Typical Characteristics

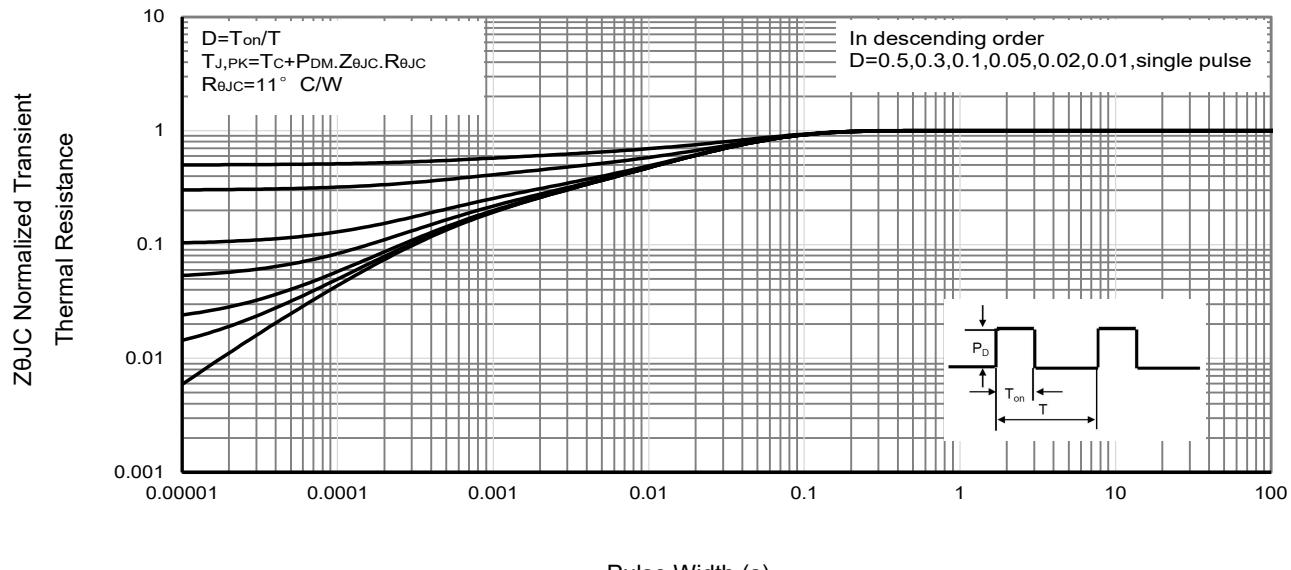


Fig13 . Normalized Maximum Transient Thermal Impedance

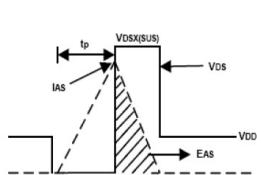
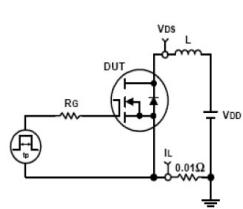


Fig14. Unclamped Inductive Test Circuit and waveforms

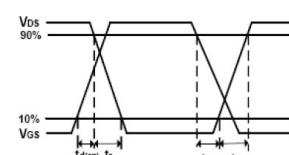
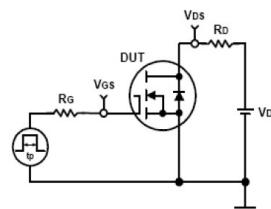
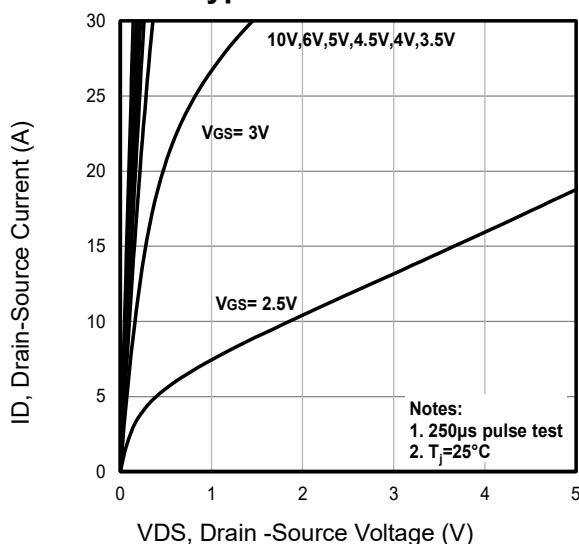
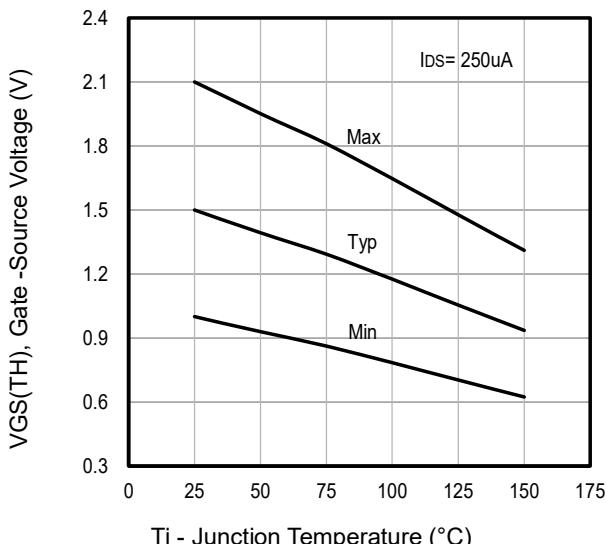
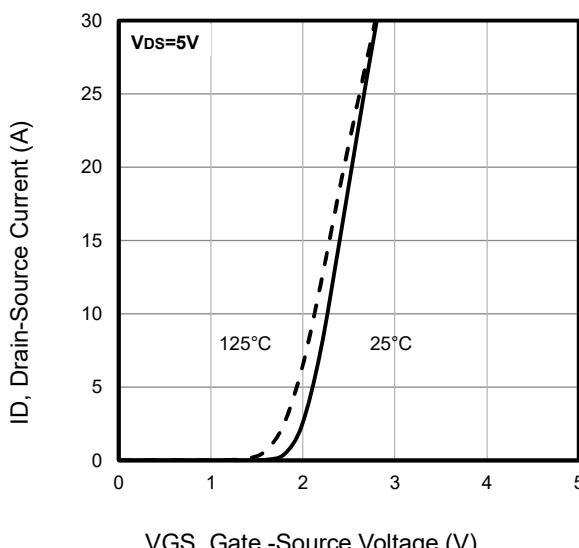
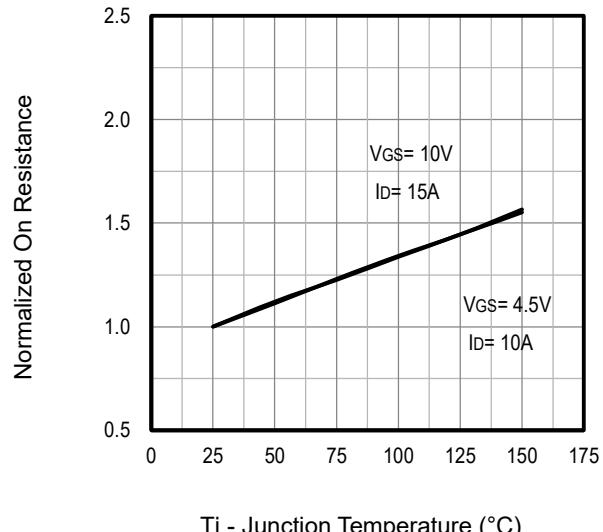
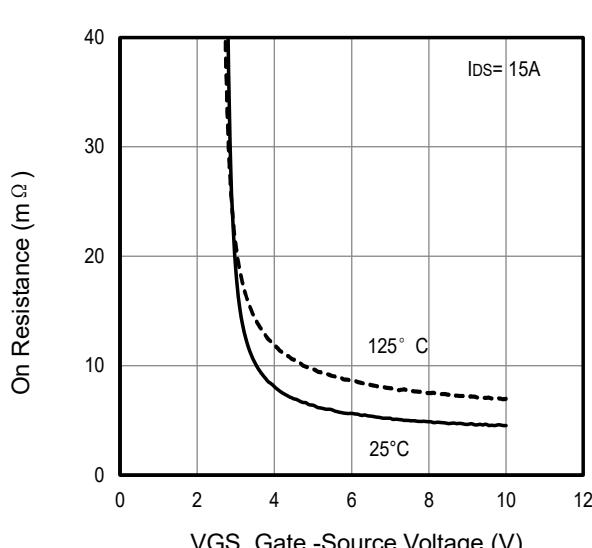
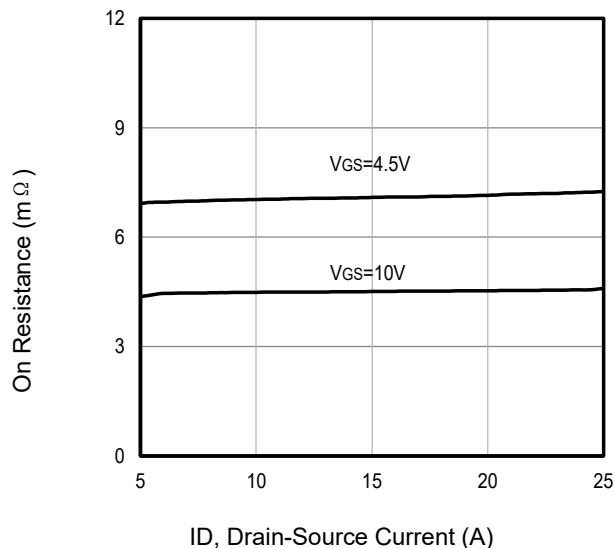


Fig15. Switching Time Test Circuit and waveforms

Q2-Channel Typical Characteristics

Fig1. Typical Output Characteristics

Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

Fig3. Typical Transfer Characteristics

Fig4. Typical Normalized On-Resistance Vs. T_j

Fig5. Typical On Resistance Vs Gate -Source Voltage

Fig6. Typical On Resistance Vs Drain Current

Q2-Channel Typical Characteristics

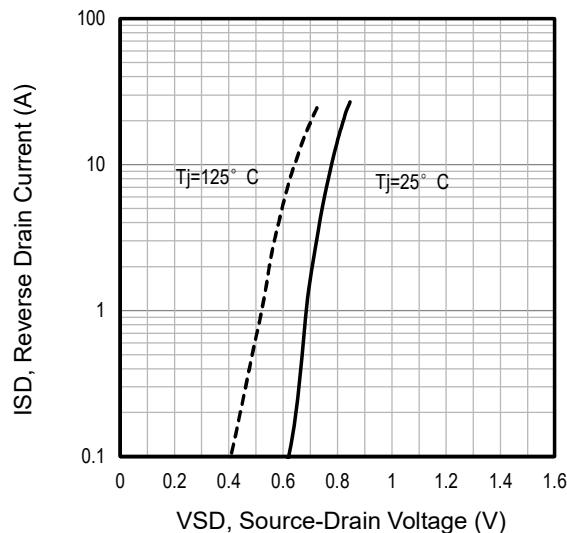


Fig7. Typical Source-Drain Diode Forward Voltage

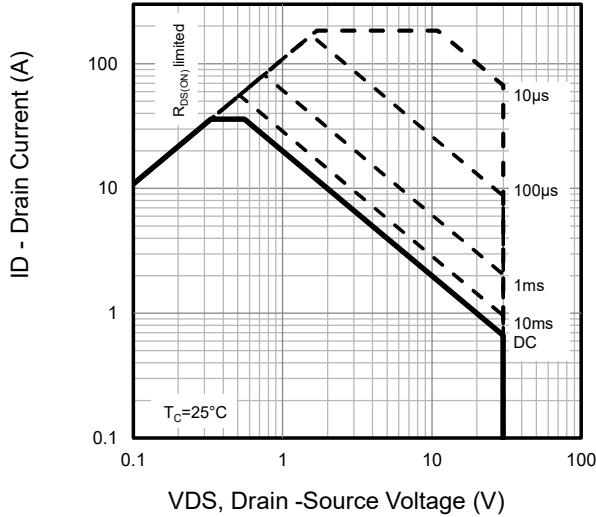


Fig8. Maximum Safe Operating Area

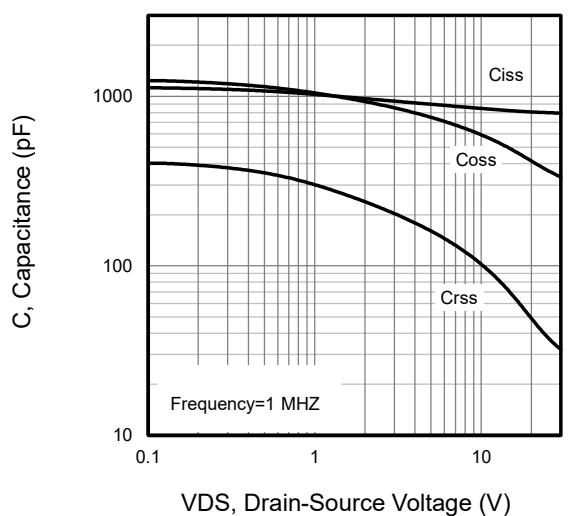


Fig9. Typical Capacitance Vs. Drain-Source Voltage

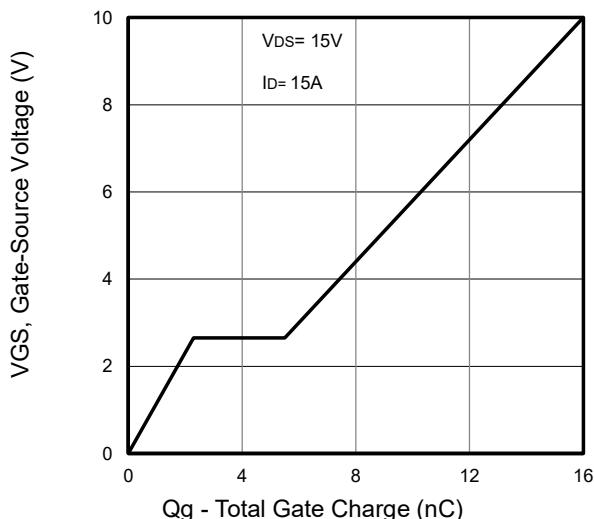


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

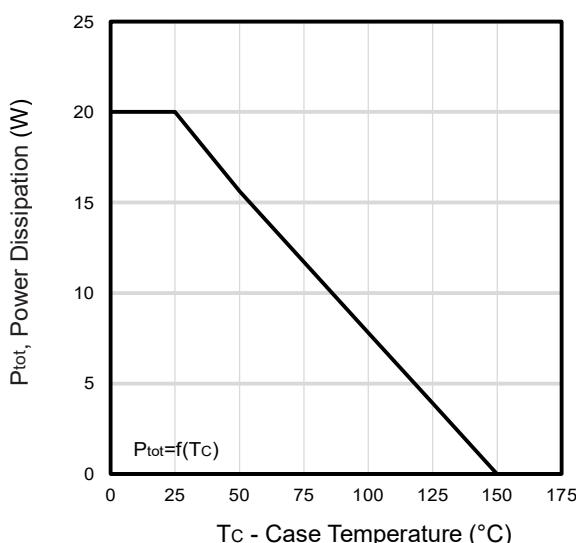


Fig11. Power Dissipation Vs. Case Temperature

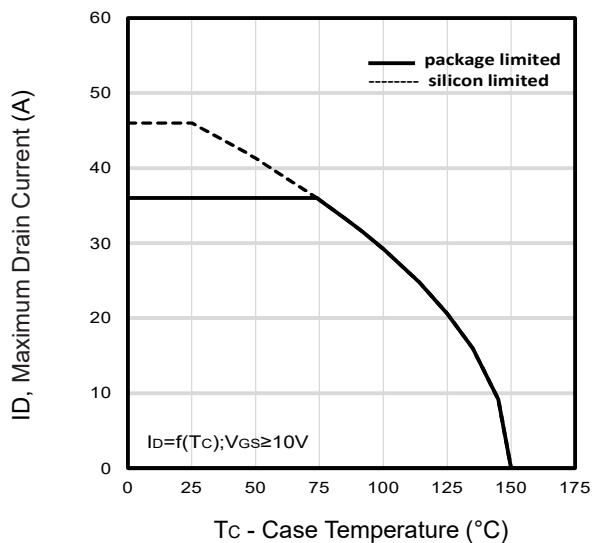


Fig12. Maximum Drain Current Vs. Case Temperature

Q2-Channel Typical Characteristics

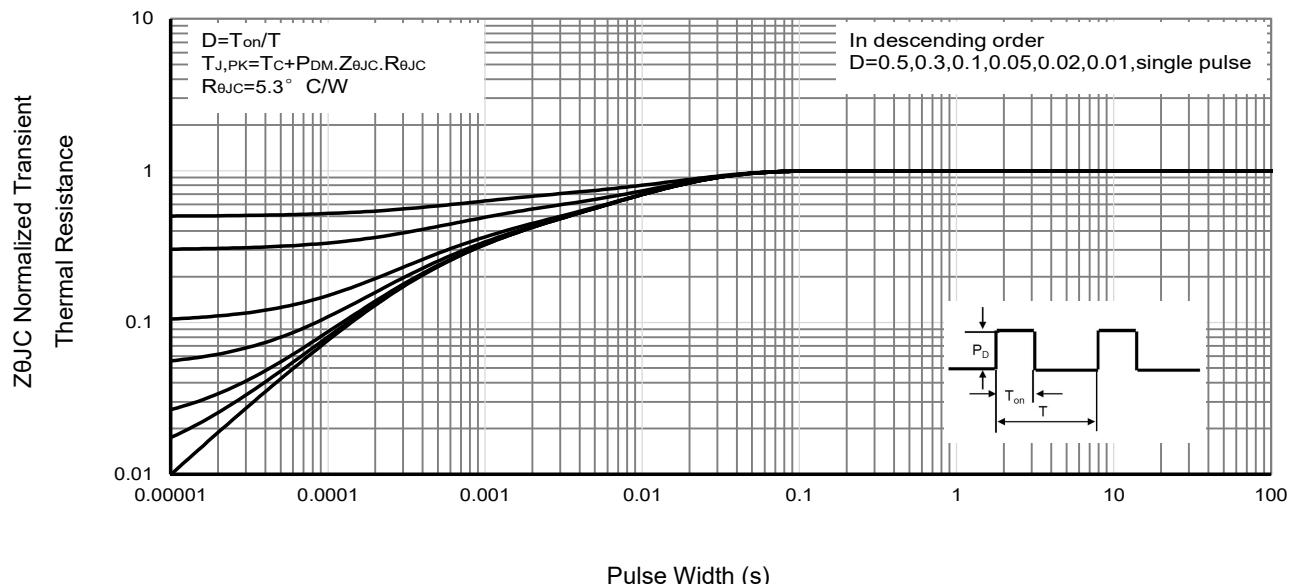


Fig13 . Normalized Maximum Transient Thermal Impedance

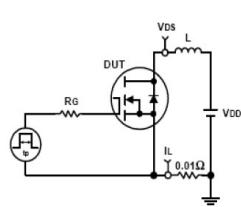


Fig14. Unclamped Inductive Test Circuit and waveforms

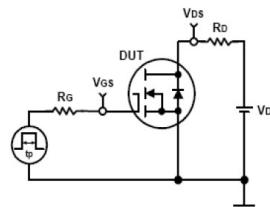
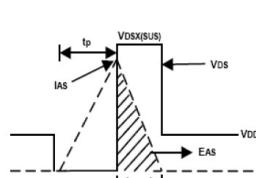


Fig15. Switching Time Test Circuit and waveforms

Marking Information

1st line: Vergiga Code (Vs)

2nd line: Part Number (3625DB)

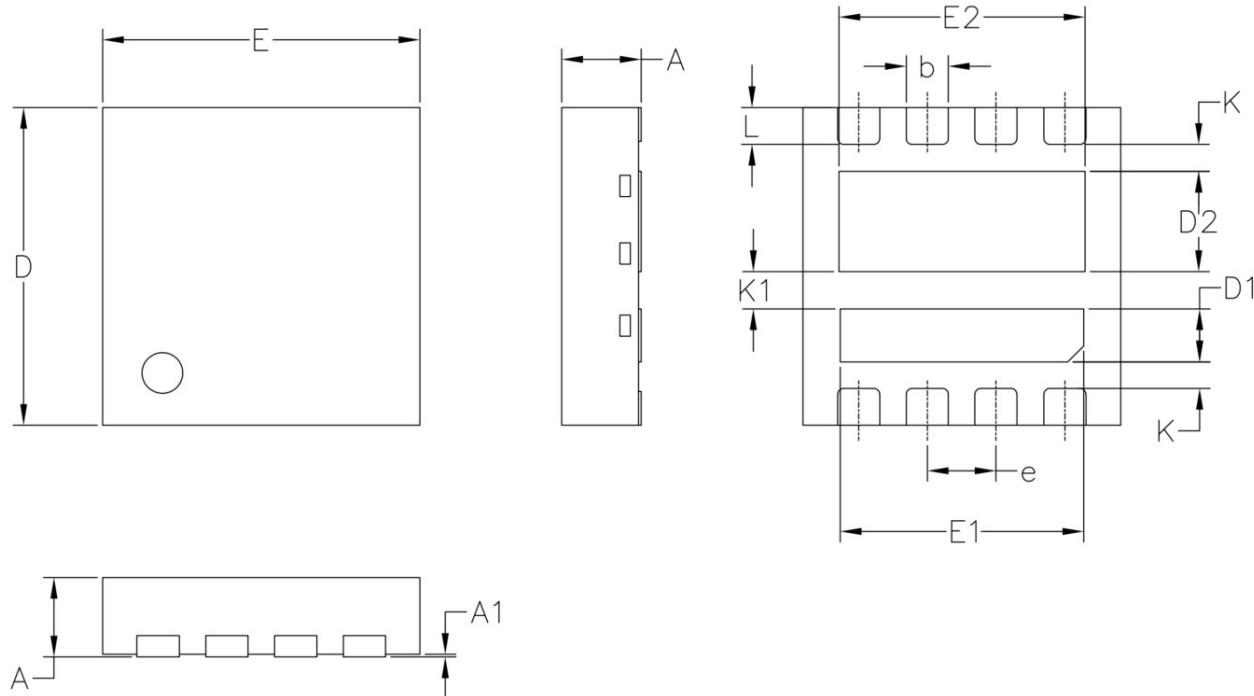
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

DFN3x3 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	--	0.05
b	0.35	0.40	0.45
D	2.90	3.00	3.10
D1	0.40	0.50	0.60
D2	0.85	0.95	1.05
E	2.90	3.00	3.10
E1	2.20	2.30	2.40
E2	2.20	2.325	2.45
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.25	0.35	0.45
L	0.27	--	0.40

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Vergiga Semiconductor CO., LTD
TEL: (86-755) -26902410

FAX: (86-755) -26907027

WEB: www.vergiga.com