

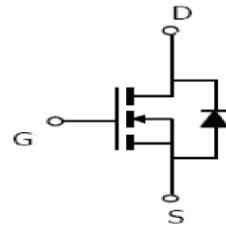
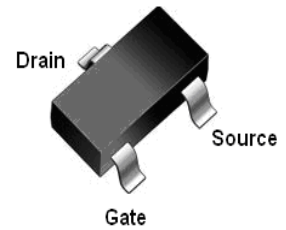
Features

- N-Channel, 2.5V Logic Level Control
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- Fast Switching
- Pb-free lead plating; RoHS compliant


Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VS3640BC	SOT23	VS06	3000pcs/reel

V_{DS}	30	V
$R_{DS(on),TYP} @ V_{GS}=4.5\text{ V}$	29	mΩ
$R_{DS(on),TYP} @ V_{GS}=2.5\text{ V}$	36	mΩ
I_D	5	A

SOT23


Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	30	V
I_S	Diode continuous forward current	$T_A=25\text{ °C}$ 0.8	A
I_D	Continuous drain current @ $V_{GS}=4.5\text{ V}$	$T_A=25\text{ °C}$ 5	A
		$T_A=100\text{ °C}$ 3	A
I_{DM}	Pulse drain current tested ①	$T_A=25\text{ °C}$ 20	A
P_D	Maximum power dissipation	$T_A=25\text{ °C}$ 1	W
V_{GS}	Gate-Source voltage	±12	V
$T_{STG} T_J$	Storage and operating temperature range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	80	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	125	°C/W



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V,V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =30V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±12V,V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	0.6	0.9	1.2	V
R _{DS(ON)}	Drain-Source On-State Resistance②	V _{GS} =4.5V, I _D =5A	--	29	38	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance②	V _{GS} =2.5V, I _D =3A	--	36	47	mΩ
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =15V,V _{GS} =0V, f=1MHz	700	770	850	pF
C _{oss}	Output Capacitance		40	50	60	pF
C _{rss}	Reverse Transfer Capacitance		35	45	55	pF
R _g	Gate Resistance	f=1MHz		3		Ω
Q _g	Total Gate Charge	V _{DS} =15V,I _D =5A, V _{GS} =4.5V	--	8.5	--	nC
Q _{gs}	Gate-Source Charge		--	1.8	--	nC
Q _{gd}	Gate-Drain Charge		--	2.1	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =15V, I _D =5A, R _G =3Ω, V _{GS} =4.5V	--	6.5	--	nS
t _r	Turn-on Rise Time		--	17	--	nS
t _{d(off)}	Turn-Off Delay Time		--	29	--	nS
t _f	Turn-Off Fall Time		--	5	--	nS
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =5A,V _{GS} =0V	--	0.9	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C,I _{sd} =5A, di/dt=100A/μs	--	10.5	--	nS
Q _{rr}	Reverse Recovery Charge			5		nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 ② Pulse width ≤ 300μs; duty cycles ≤ 2%.



Typical Characteristics

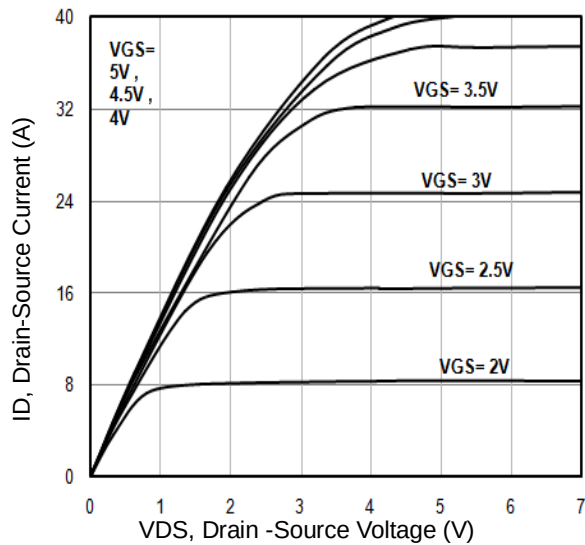


Fig1. Typical Output Characteristics

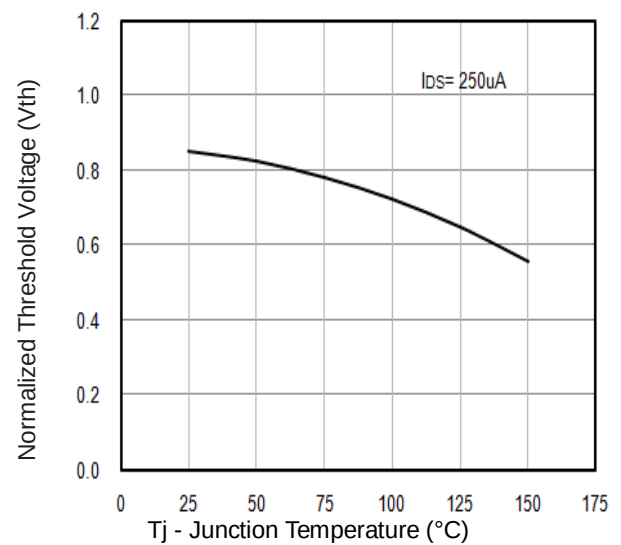


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_J

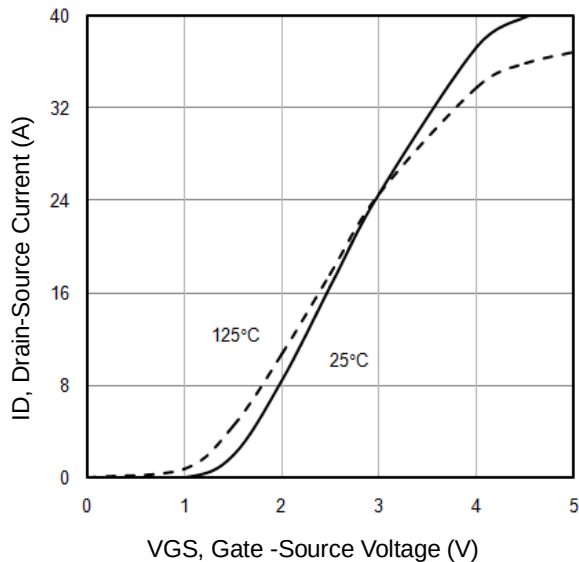


Fig3. Typical Transfer Characteristics

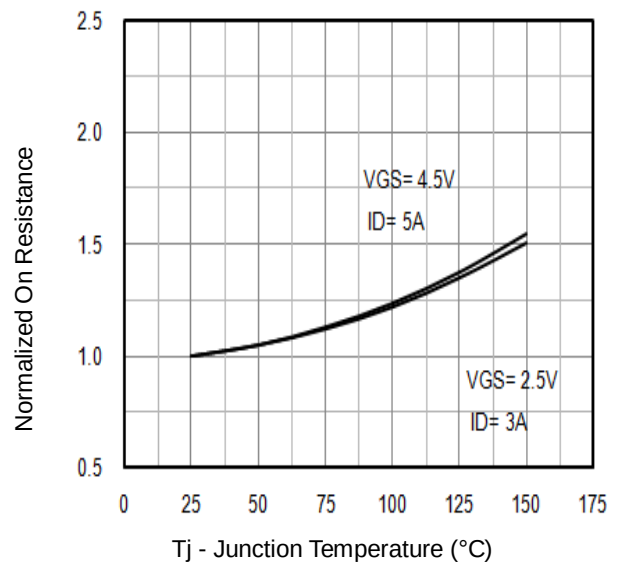


Fig4. Normalized On-Resistance Vs. T_J

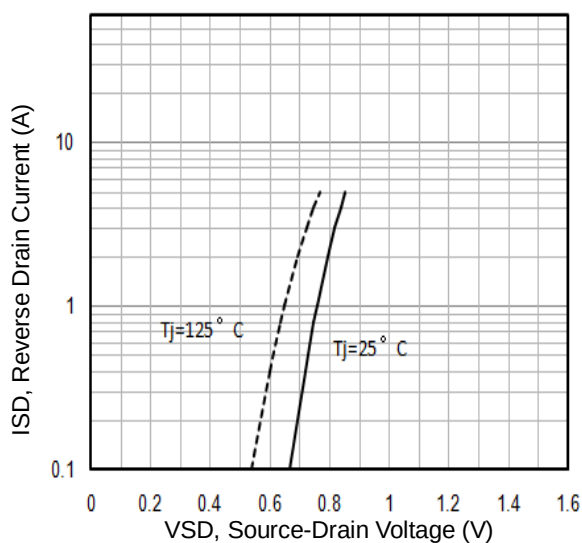


Fig5. Typical Source-Drain Diode Forward Voltage

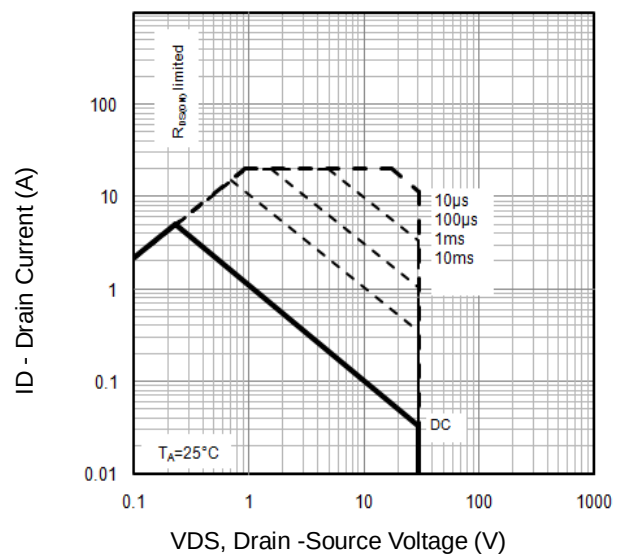


Fig6. Maximum Safe Operating Area

Typical Characteristics

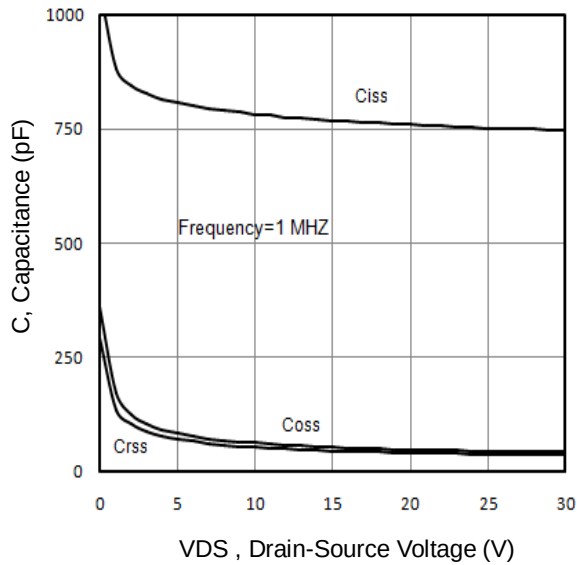


Fig7. Typical Capacitance Vs. Drain-Source Voltage

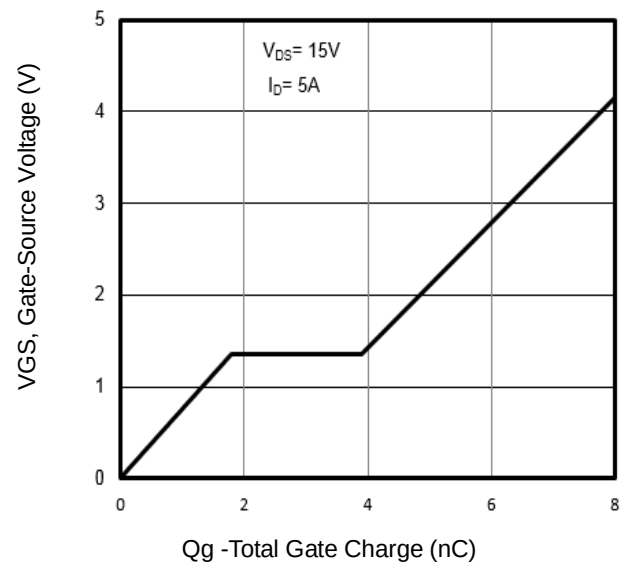


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

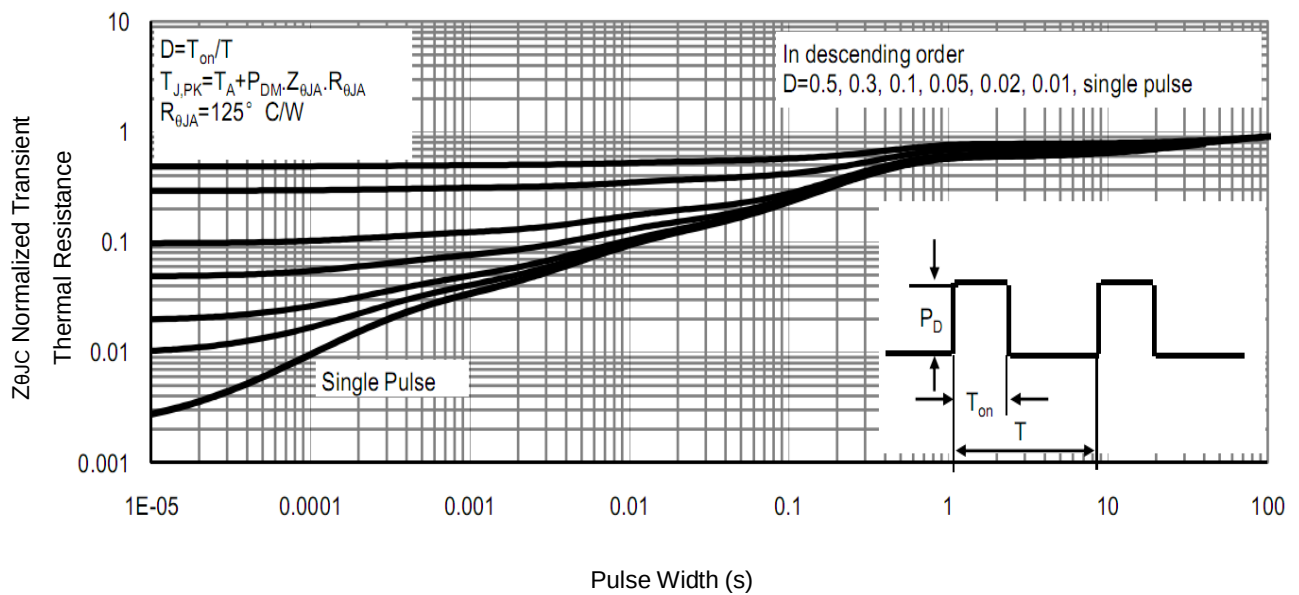


Fig9 . Normalized Maximum Transient Thermal Impedance

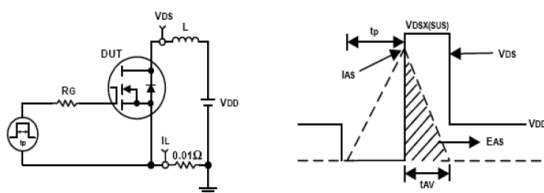


Fig10. Unclamped Inductive Test Circuit and waveforms

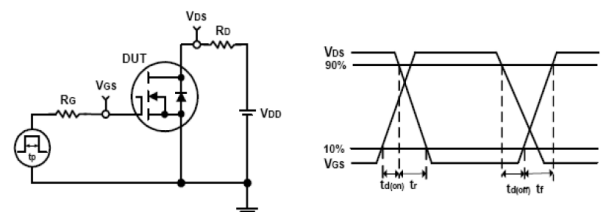
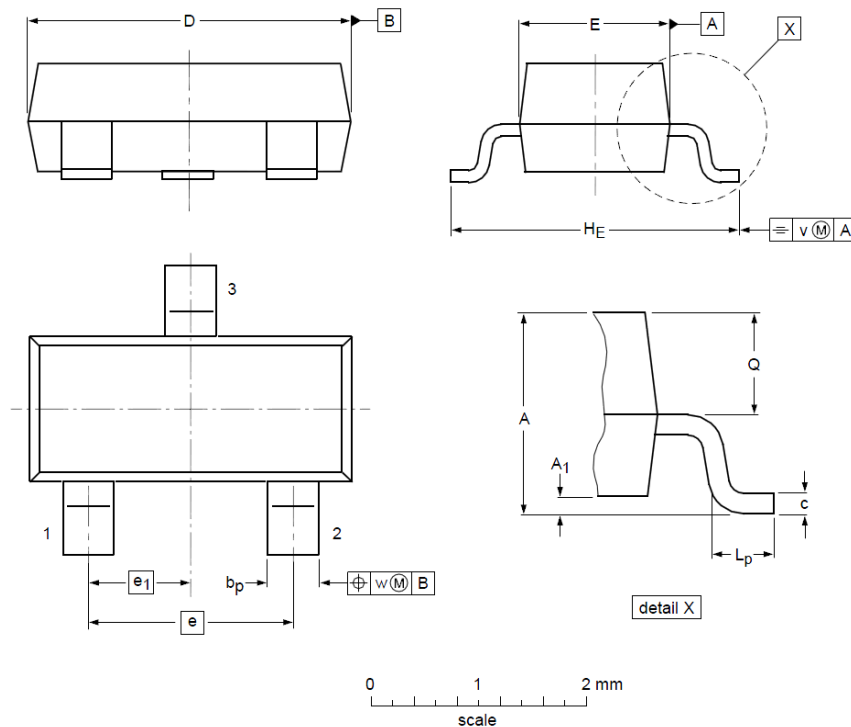


Fig11. Switching Time Test Circuit and waveforms

SOT23 Package Outline Data



Label	DIMENSIONS (unit: mm)		
	Min	Typ	Max
A	0.90	1.03	1.10
A₁	0.01	0.05	0.10
b_p	0.38	0.42	0.48
c	0.09	0.13	0.15
D	2.80	2.92	3.00
E	1.20	1.33	1.40
e	--	1.90	--
e₁	--	0.95	--
H_E	2.10	2.40	2.50
L_p	0.40	0.50	0.60
Q	0.45	0.49	0.55
v	--	0.20	--
w	--	0.10	--

Notes:

1. Follow JEDEC TO-236, variation AB.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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