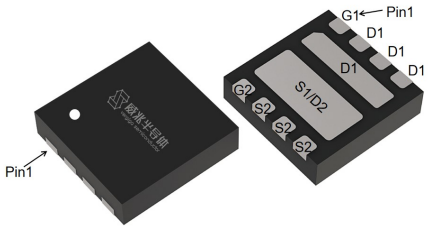
Features

- Dual Asymmetric N-Channel
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested,100% Rg Tested

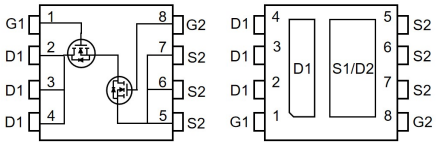
V_{DS}	30	30	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	8.2	4.9	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5V	12	7.7	mΩ
$I_{D(Wire\ bond\ Limited)}$	24	36	A

DFN3x3



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS3647DB	DFN3x3	3647DB	5000pcs/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating Q1	Rating Q2	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		30	30	V
V_{GS}	Gate-Source voltage		±20	±20	V
I_S	Diode continuous forward current	T_C =25°C	14	23	A
I_D	Continuous drain current @VGS=10V((Wire bond Limited)	T_C =25°C	24	36	A
	Continuous drain current @VGS=10V((Sillicon Limited)	T_C =100°C	20	32	A
I_{DM}	Pulse drain current tested ①	T_C =25°C	128	204	A
I_{DSM}	Continuous drain current @VGS=10V	T_A =25°C	10	14	A
		T_A =70°C	8	11	A
EAS	Avalanche energy, single pulsed ②		49	64	mJ
P_D	Maximum power dissipation ③	T_C =25°C	17	27	W
P_{DSM}	Maximum power dissipation ④	T_A =25°C	1.7	2.1	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical Q1	Typical Q2	Max Q1	Max Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	6.1	3.9	7.3	4.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	60	50	72	60	°C/W

Q1-Channel Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_j=25℃)	V_{DS}=30V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)⑦	V_{DS}=30V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.1	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=13A	--	8.2	11	mΩ
		V_{GS}=4.5V, I_D=10A	--	12	16	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V_{DS}=15V,V_{GS}=0V, f=1MHz	--	420	--	pF
Coss	Output Capacitance ⑦		--	315	--	pF
Crss	Reverse Transfer Capacitance ⑦		--	10	--	pF
Rg	Gate Resistance	f=1MHz	--	1.3	--	Ω
Qg(10V)	Total Gate Charge ⑦	V_{DS}=15V,I_D=13A, V_{GS}=10V	--	7.6	--	nC
Qg(4.5V)	Total Gate Charge ⑦		--	3.7	--	nC
Qgs	Gate Source Charge ⑦		--	1.5	--	nC
Qgd	Gate Drain Charge ⑦		--	1.2	--	nC
Switching Characteristics ⑦						
Td(on)	Turn on Delay Time	V_{DD}=15V, I_D=13A, R_G=3Ω, V_{GS}=10V	--	4.4	--	ns
Tr	Turn on Rise Time		--	39	--	ns
Td(off)	Turn Off Delay Time		-	10	--	ns
Tf	Turn Off Fall Time		--	2.2	--	ns
Source Drain Diode Characteristics						
V_{SD}	Forward on voltage	I_{SD}=13A,V_{GS}=0V	--	0.8	1.2	V
Trr	Reverse Recovery Time ⑦	V_{DD}=15V, I_{sd}=13A, V_{GS}=0V di/dt=100A/μs	--	14	--	ns
Qrr	Reverse Recovery Charge ⑦		--	3.5	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② Q1：EAS of 49mJ is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 14A, V_{GS} =10V； 100% FT tested at L = 0.5mH, I_{AS} = 8A.
Q2：EAS of 64mJ is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 16A, V_{GS} =10V； 100% FT tested at L = 0.5mH, I_{AS} = 9A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ These tests are performed respectively with the device mounted on a 1 in2 pad and a minimum pad of 2oz. Copper FR-4 board in a still air environment with TA=25°C, using Transient Dual Interface method to acquire RθJC.

⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Q2-Channel Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current t(T_j=25℃)	V_{DS}=30V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current t(T_j=125℃)⑦	V_{DS}=30V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.2	1.7	2.3	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=15A	--	4.9	6.4	mΩ
		V_{GS}=4.5V, I_D=10A	--	7.7	10	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	VDS=15V,VGS=0V, f=1MHz	--	835	--	pF
Coss	Output Capacitance ⑦		--	540	--	pF
Crss	Reverse Transfer Capacitance ⑦		--	60	--	pF
Rg	Gate Resistance	f=1MHz	--	1.9	--	Ω
Qg(10V)	Total Gate Charge ⑦	VDS=15V,ID=15A, VGS=10V	--	15	--	nC
Qg(4.5V)	Total Gate Charge ⑦		--	7.6	--	nC
Qgs	Gate Source Charge ⑦		--	2.7	--	nC
Qgd	Gate Drain Charge ⑦		--	3	--	nC
Switching Characteristics ⑦						
Td(on)	Turn on Delay Time	VDD=15V, ID=15A, RG=3Ω, VGS=10V	--	5.6	--	ns
Tr	Turn on Rise Time		--	44	--	ns
Td(off)	Turn Off Delay Time		-	15	--	ns
Tf	Turn Off Fall Time		--	7.2	--	ns
Source Drain Diode Characteristics						
V_{SD}	Forward on voltage	I_{SD}=15A,V_{GS}=0V	--	0.8	1.2	V
Trr	Reverse Recovery Time ⑦	V_{DD}=15V, Isd=15A, VGS=0V di/dt=100A/μs	--	19	--	ns
Qrr	Reverse Recovery Charge ⑦		--	5.3	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② Q1：EAS of 49mJ is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 14A, V_{GS} =10V；100% FT tested at L = 0.5mH, I_{AS} = 8A.
Q2：EAS of 64mJ is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 16A, V_{GS} =10V；100% FT tested at L = 0.5mH, I_{AS} = 9A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ These tests are performed respectively with the device mounted on a 1 in2 pad and a minimum pad of 2oz. Copper FR-4 board in a still air environment with TA=25°C, using Transient Dual Interface method to acquire RθJC.

⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Q1-Channel Typical Characteristics

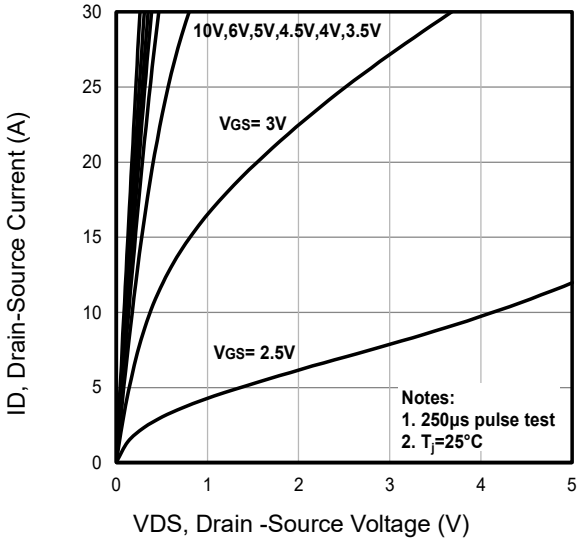


Fig1. Typical Output Characteristics

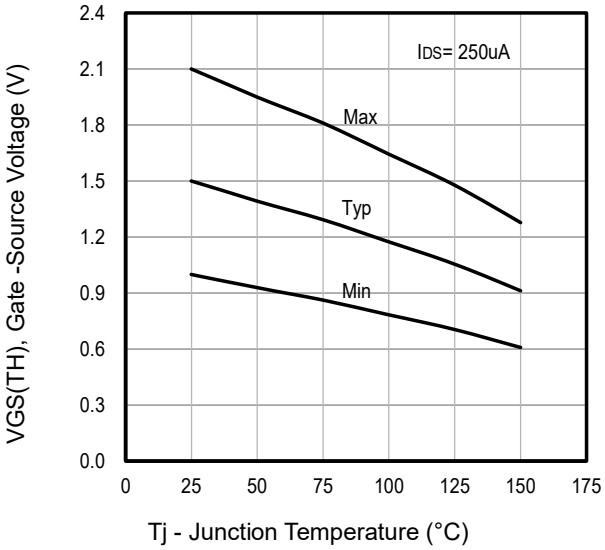


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

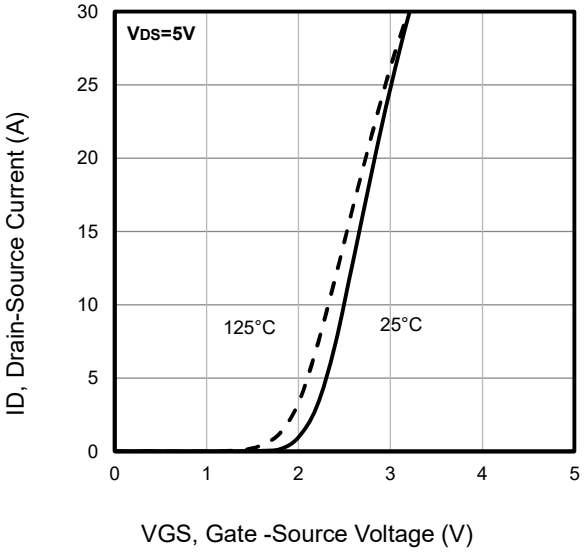


Fig3. Typical Transfer Characteristics

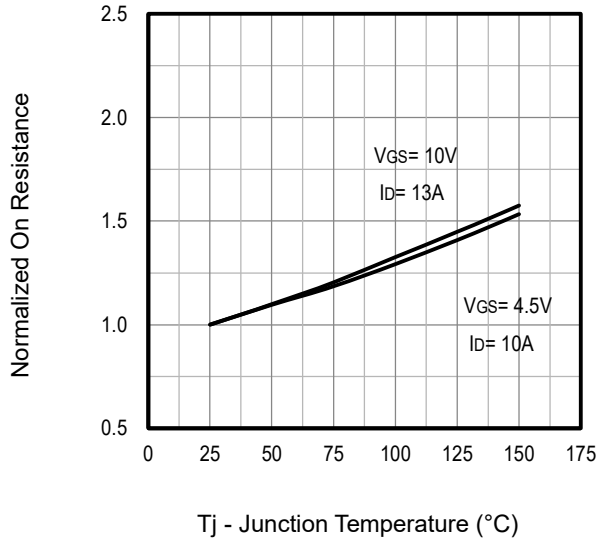


Fig4. Typical Normalized On-Resistance Vs. Tj

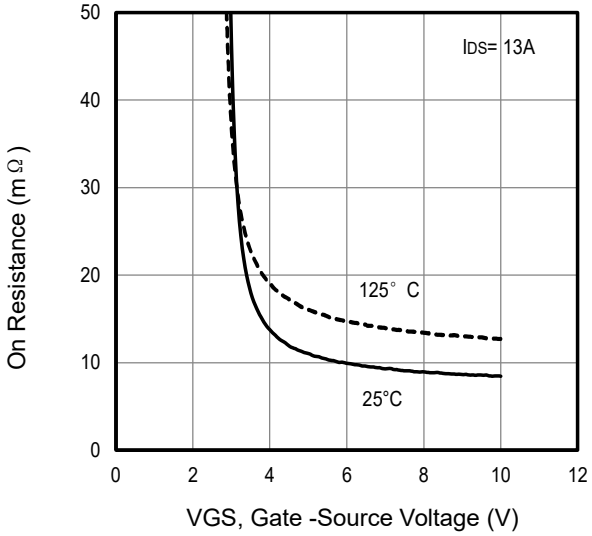


Fig5. Typical On Resistance Vs Gate -Source Voltage

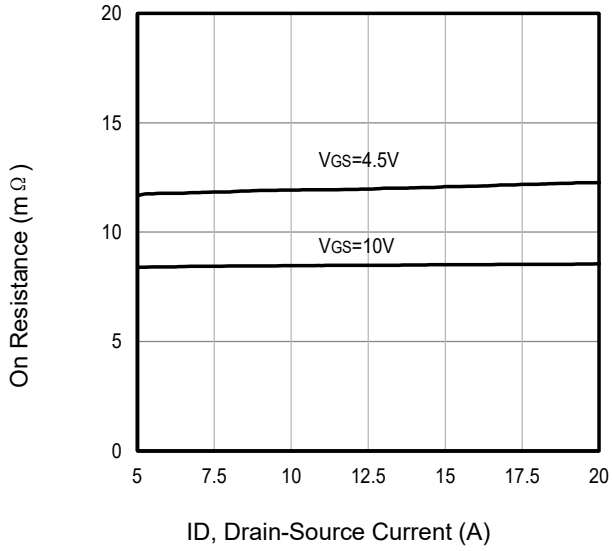


Fig6. Typical On Resistance Vs Drain Current

Q1-Channel Typical Characteristics

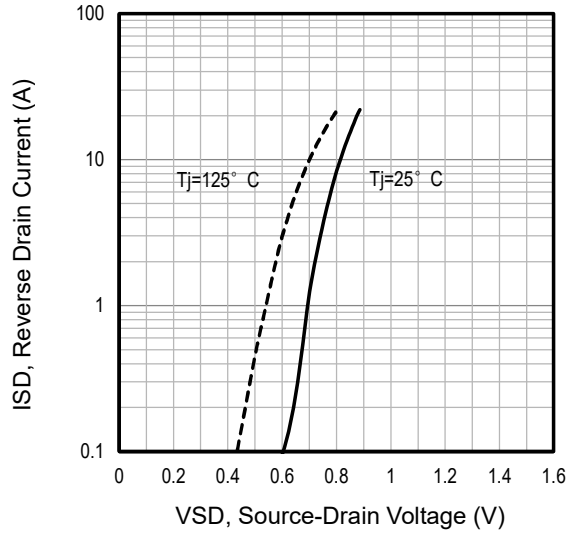


Fig7. Typical Source-Drain Diode Forward Voltage

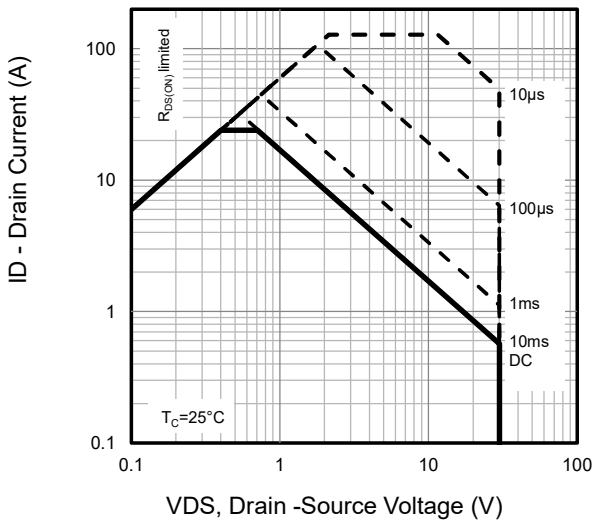


Fig8. Maximum Safe Operating Area

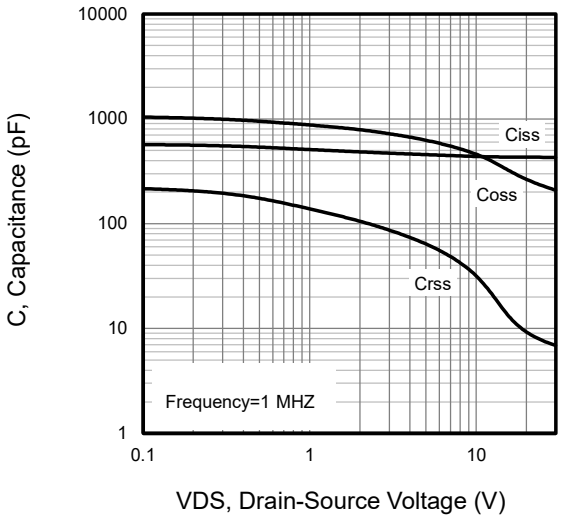


Fig9. Typical Capacitance Vs. Drain-Source Voltage

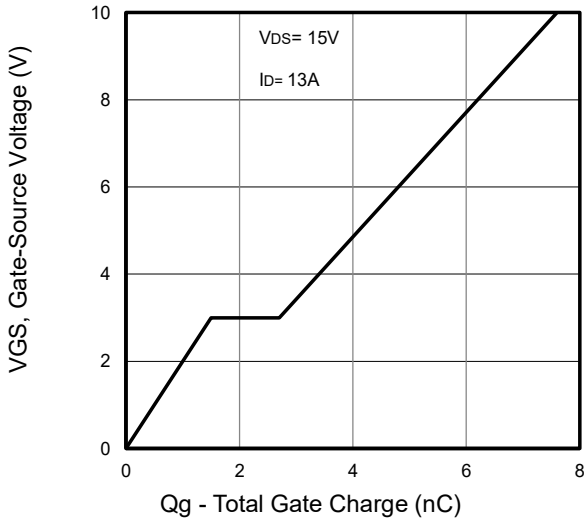


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

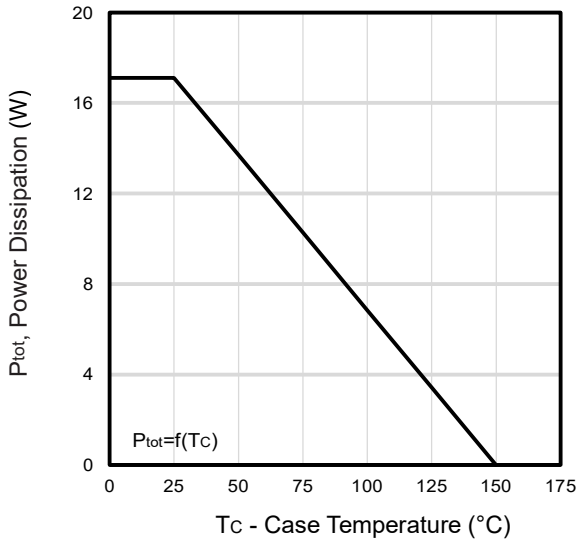


Fig11. Power Dissipation Vs. Case Temperature

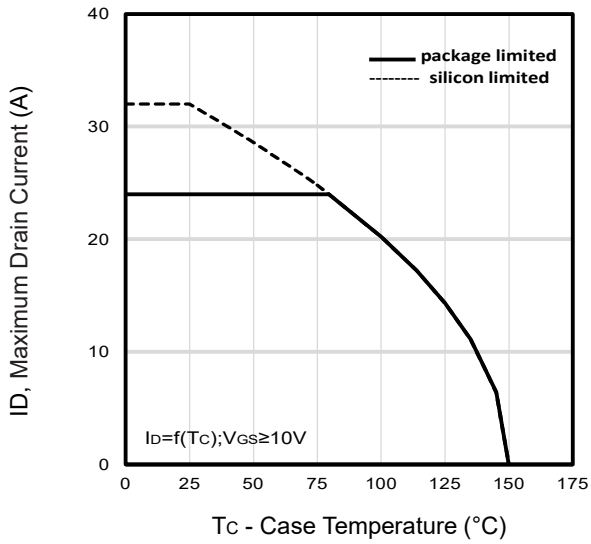


Fig12. Maximum Drain Current Vs. Case Temperature

Q1-Channel Typical Characteristics

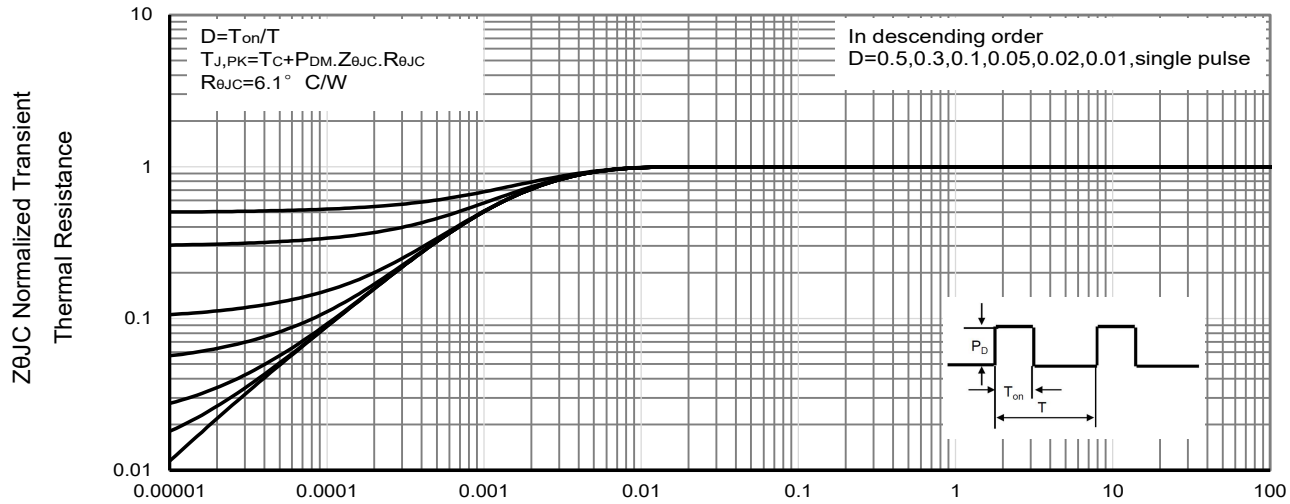


Fig13 . Normalized Maximum Transient Thermal Impedance

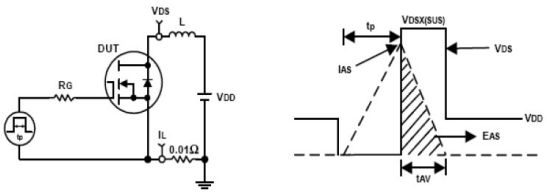


Fig14. Unclamped Inductive Test Circuit and waveforms

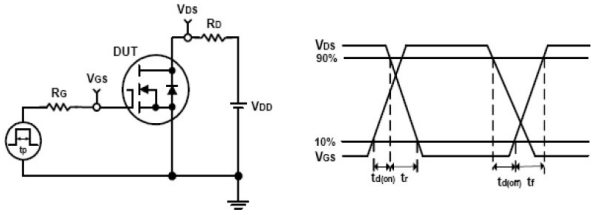


Fig15. Switching Time Test Circuit and waveforms

Q2-Channel Typical Characteristics

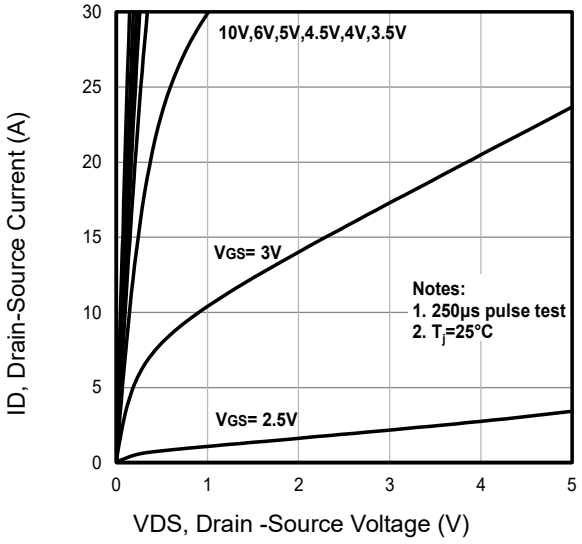


Fig1. Typical Output Characteristics

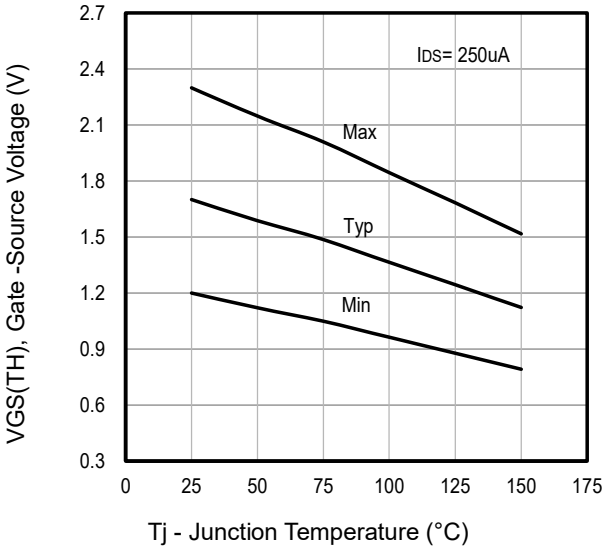


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

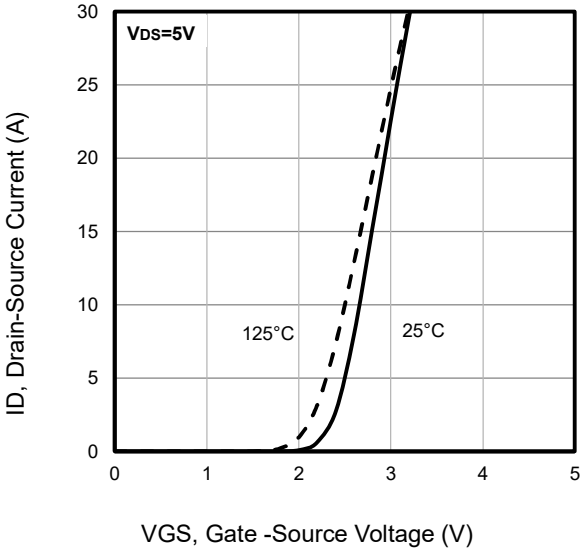


Fig3. Typical Transfer Characteristics

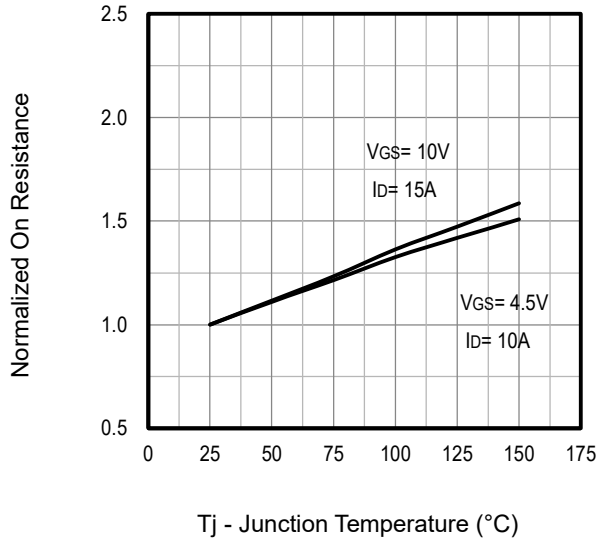


Fig4. Typical Normalized On-Resistance Vs. Tj

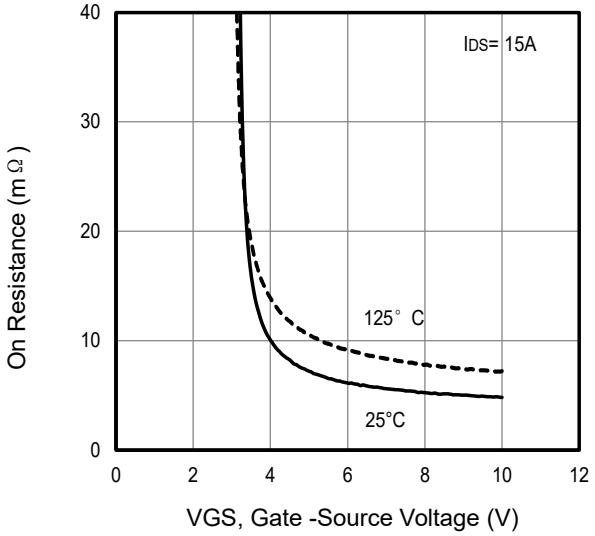


Fig5. Typical On Resistance Vs Gate -Source Voltage

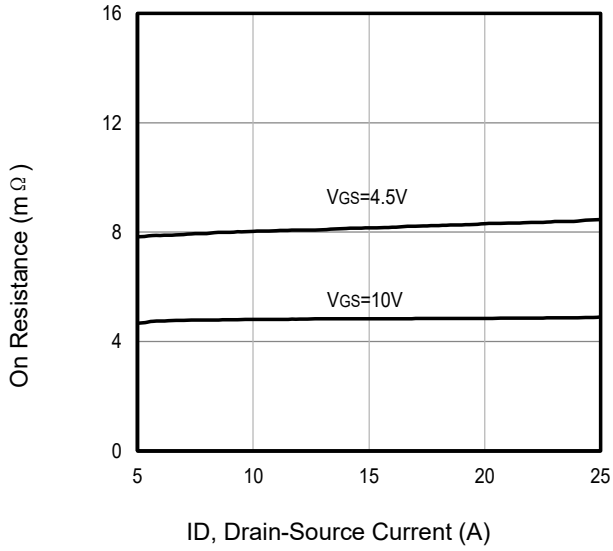


Fig6. Typical On Resistance Vs Drain Current

Q2-Channel Typical Characteristics

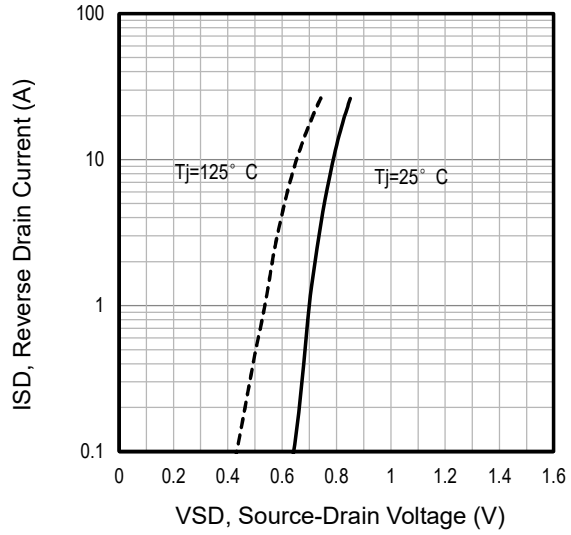


Fig7. Typical Source-Drain Diode Forward Voltage

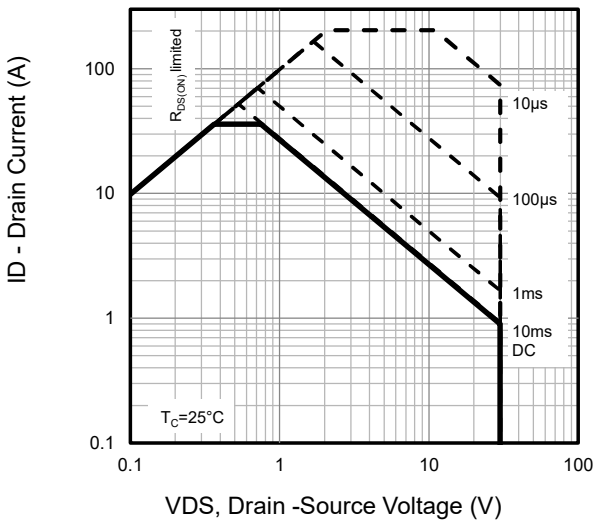


Fig8. Maximum Safe Operating Area

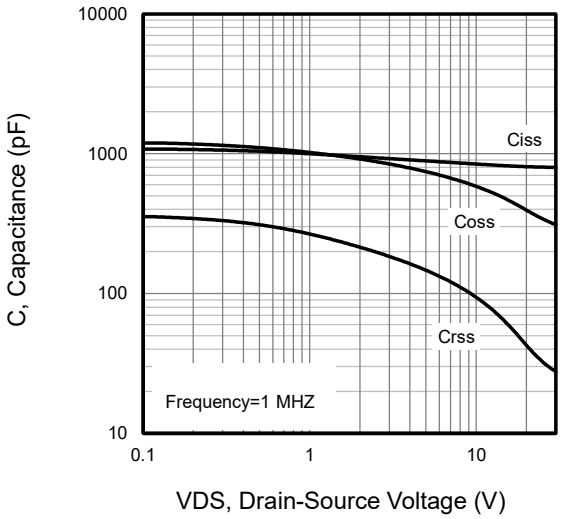


Fig9. Typical Capacitance Vs. Drain-Source Voltage

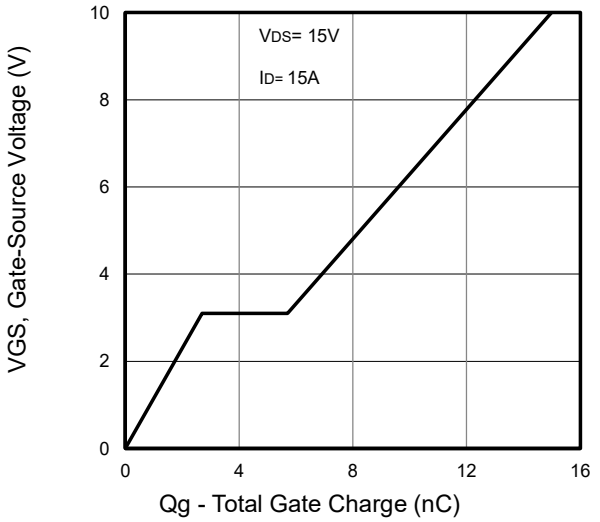


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

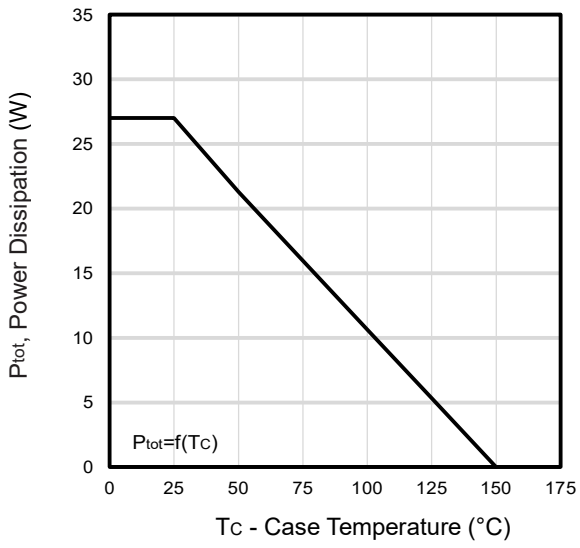


Fig11. Power Dissipation Vs. Case Temperature

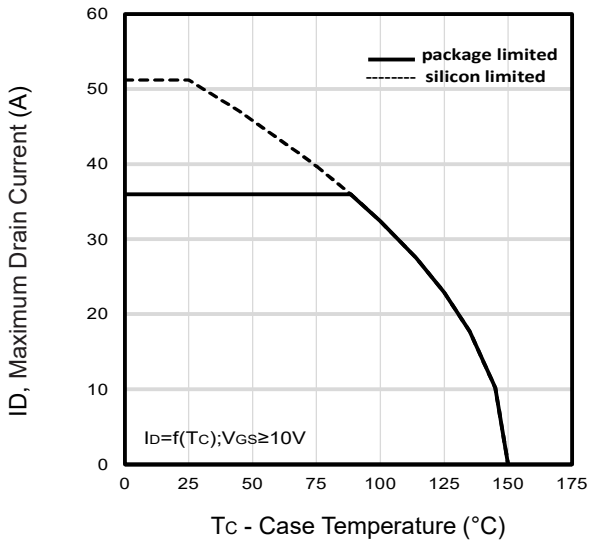


Fig12. Maximum Drain Current Vs. Case Temperature

Q2-Channel Typical Characteristics

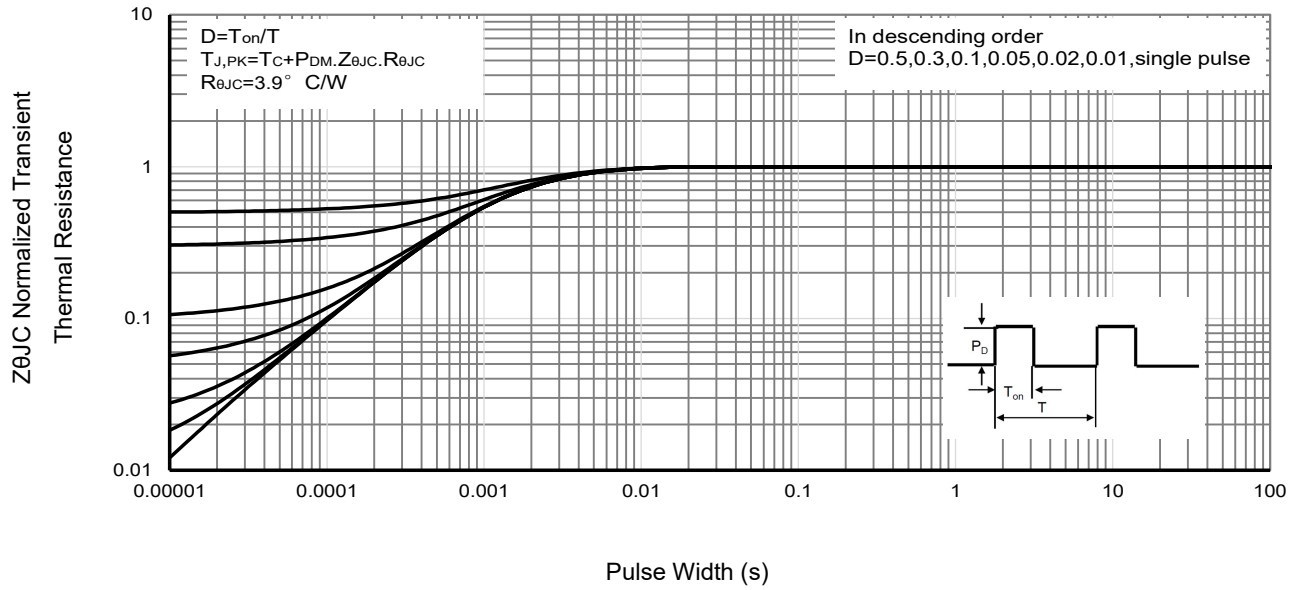


Fig13 . Normalized Maximum Transient Thermal Impedance

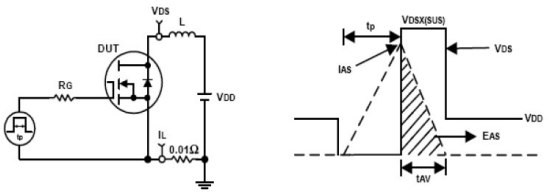


Fig14. Unclamped Inductive Test Circuit and waveforms

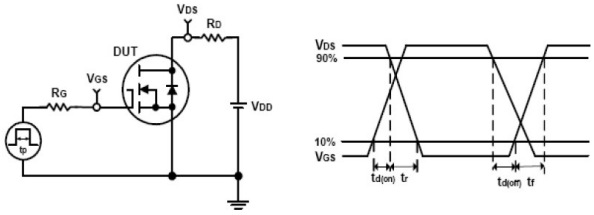
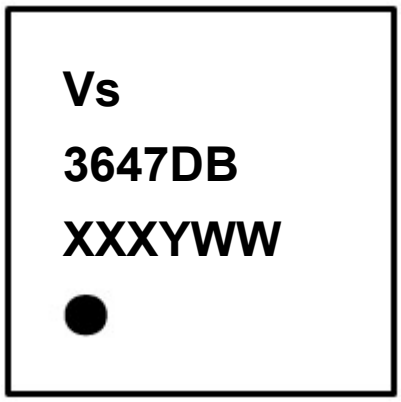


Fig15. Switching Time Test Circuit and waveforms

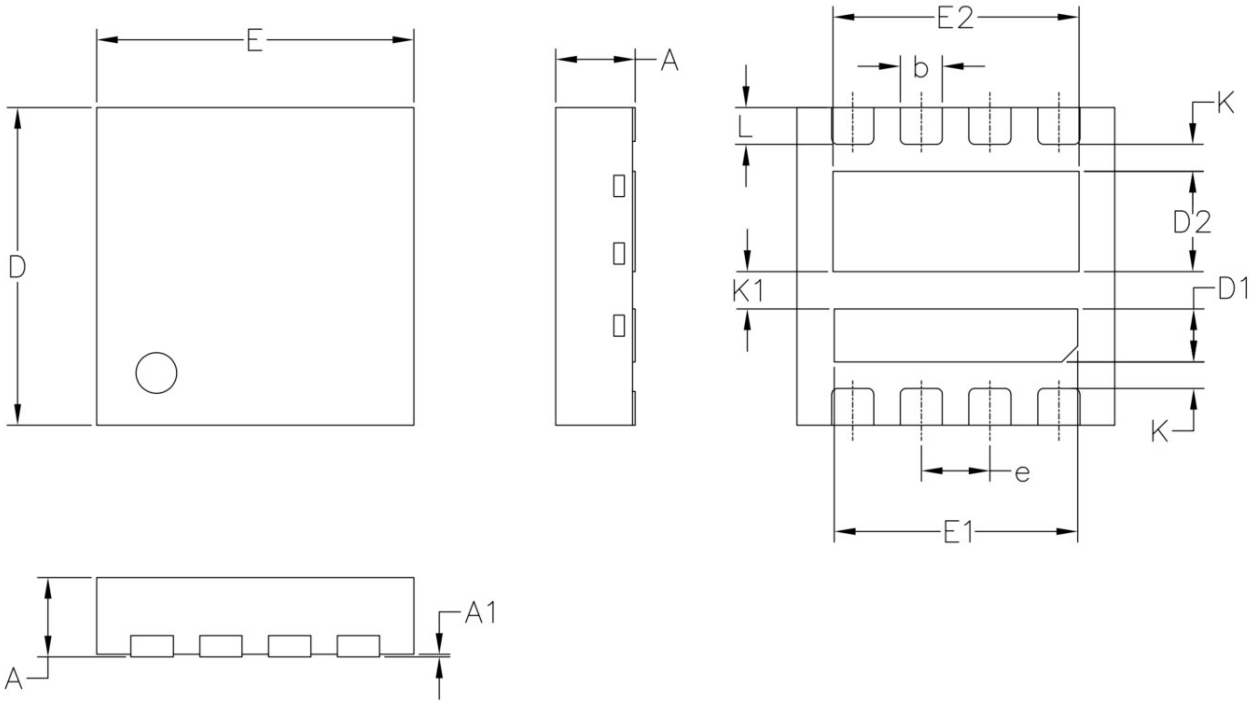
Marking Information



1st line: Vergiga Code（Vs）
2nd line: Part Number（3647DB）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code, code changed with Lot Number
Y: Year Code，refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

DFN3x3 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	--	0.05
b	0.35	0.40	0.45
D	2.90	3.00	3.10
D1	0.40	0.50	0.60
D2	0.85	0.95	1.05
E	2.90	3.00	3.10
E1	2.20	2.30	2.40
E2	2.20	2.325	2.45
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.25	0.35	0.45
L	0.27	--	0.40

Customer Service

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