Features

- P-Channel，-5V Logic Level Control
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ V_{GS}=-4.5 V
- Fast Switching
- Pb-free lead plating; RoHS compliant; Halogen Free

V_{DS}	-40	V
$R_{DS(on),max}$ @V_{GS}=-10V	29	mΩ
$R_{DS(on),max}$ @V_{GS}=-4.5V	44	mΩ
I_D	-5.5	A

Pb-Free RoHS HF Halogen-Free

SOT23-6L

Drain Pin1,2,5,6

Gate Pin3

Source Pin4

Part ID	Package Type	Marking	Tape and reel information
VS4518AH	SOT23-6L	VS11	3000pcs/reel

Maximum ratings, at T_j =25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		-40	V
I_S	Diode continuous forward current	T_A =25°C	-1	A
I_D	Continuous drain current @V_{GS}=-10V	T_A =25°C	-5.5	A
		T_A =100°C	-3.4	A
I_{DM}	Pulse drain current tested ①	T_A =25°C	-22	A
P_D	Maximum power dissipation	T_A =25°C	1.25	W
V_{GS}	Gate-Source voltage		±20	V
T_{STG} T_J	Storage and operating temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance，Junction to Lead	60	°C/W
$R_{\theta JA}$	Thermal Resistance，Junction to Ambient	100	°C/W

Typical Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=-40V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃)	V_{DS}=-40V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-1.3	-1.9	-2.4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance②	V_{GS}=-10V, I_D=-4A	--	29	38	mΩ
		V_{GS}=-4.5V, I_D=-3A	--	44	57	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=-20V,V_{GS}=0V, f=1MHz	1000	1310	1600	pF
C_{oss}	Output Capacitance		60	115	170	pF
C_{rss}	Reverse Transfer Capacitance		40	90	140	pF
R_g	Gate Resistance	f=1MHz	--	10	--	Ω
Q_g	Total Gate Charge	V_{DS}=-20V,I_D=-4A, V_{GS}=-10V	--	30	--	nC
Q_{gs}	Gate-Source Charge		--	4	--	nC
Q_{gd}	Gate-Drain Charge		--	6	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=-20 V, I_D=-4A, R_G=3Ω, V_{GS}=-10V	--	9	--	nS
t_r	Turn-on Rise Time		--	7	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	192	--	nS
t_f	Turn-Off Fall Time		--	64	--	nS
Source- Drain Diode Characteristics@ T_j= 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=-4A,V_{GS}=0V	--	-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=-4A, V_{GS}=0V di/dt=-100A/μs	--	17	--	nS
Q_{rr}	Reverse Recovery Charge			7		nC

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

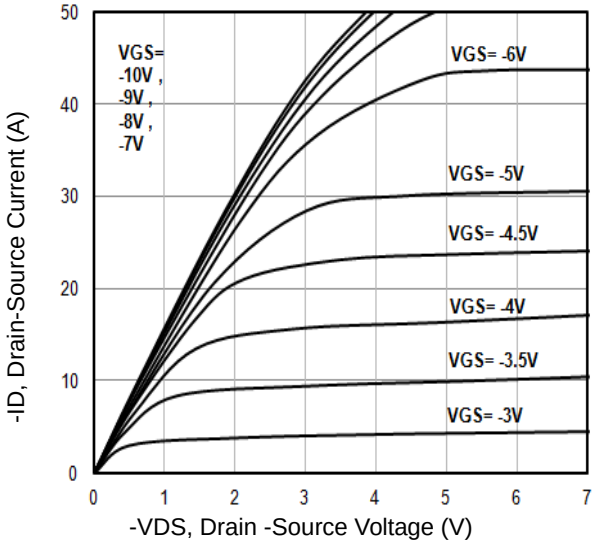


Fig1. Typical Output Characteristics

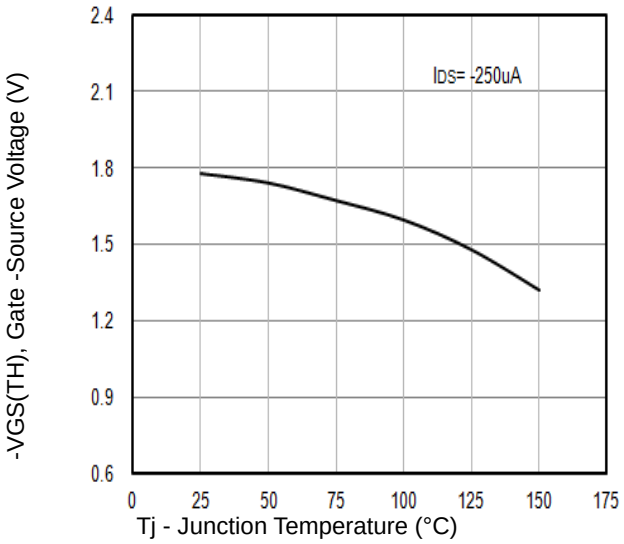


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

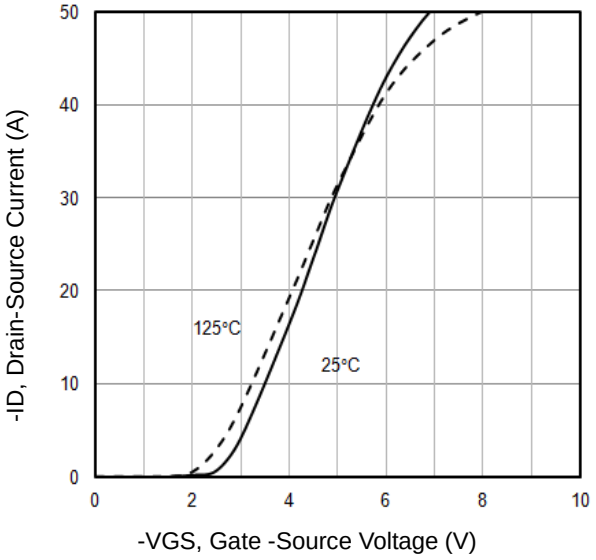


Fig3. Typical Transfer Characteristics

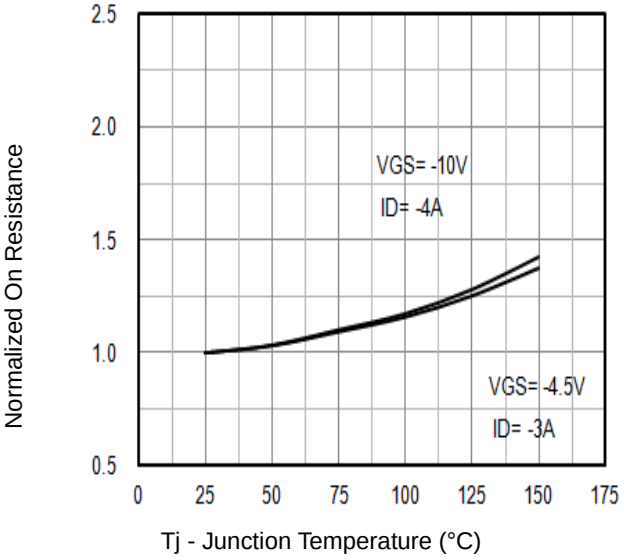


Fig4. Normalized On-Resistance Vs. Tj

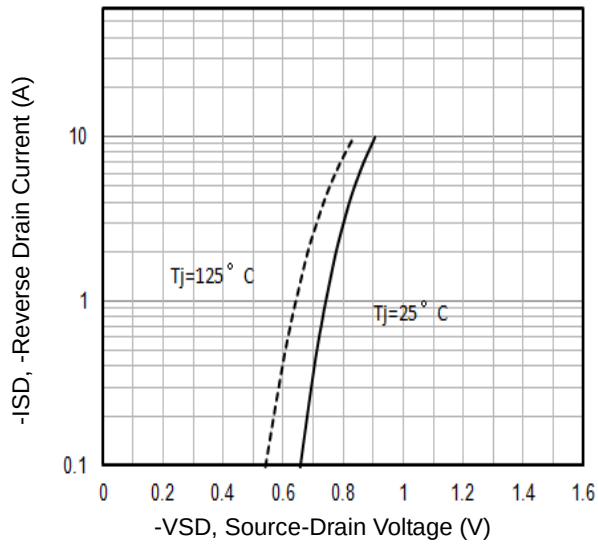


Fig5. Typical Source-Drain Diode Forward Voltage

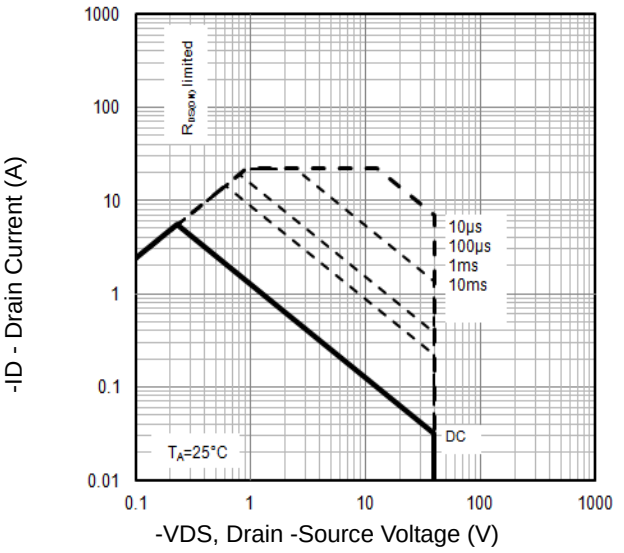


Fig6. Maximum Safe Operating Area

Typical Characteristics

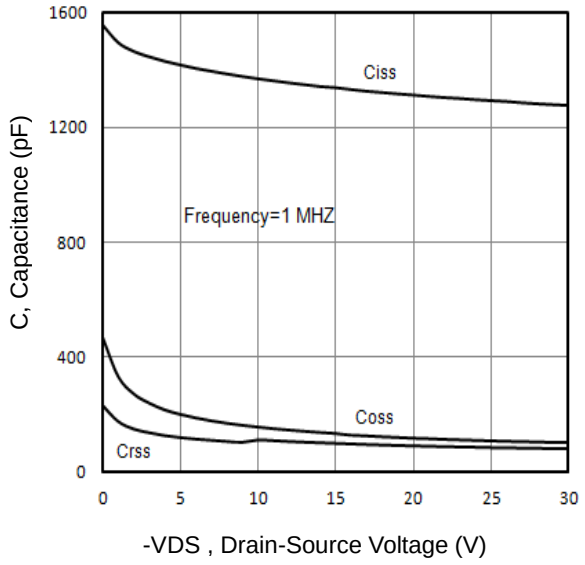


Fig7. Typical Capacitance Vs.Drain-Source Voltage

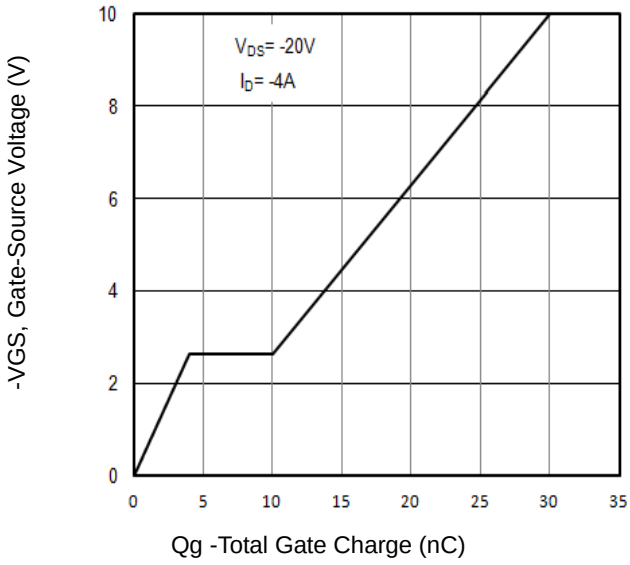


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

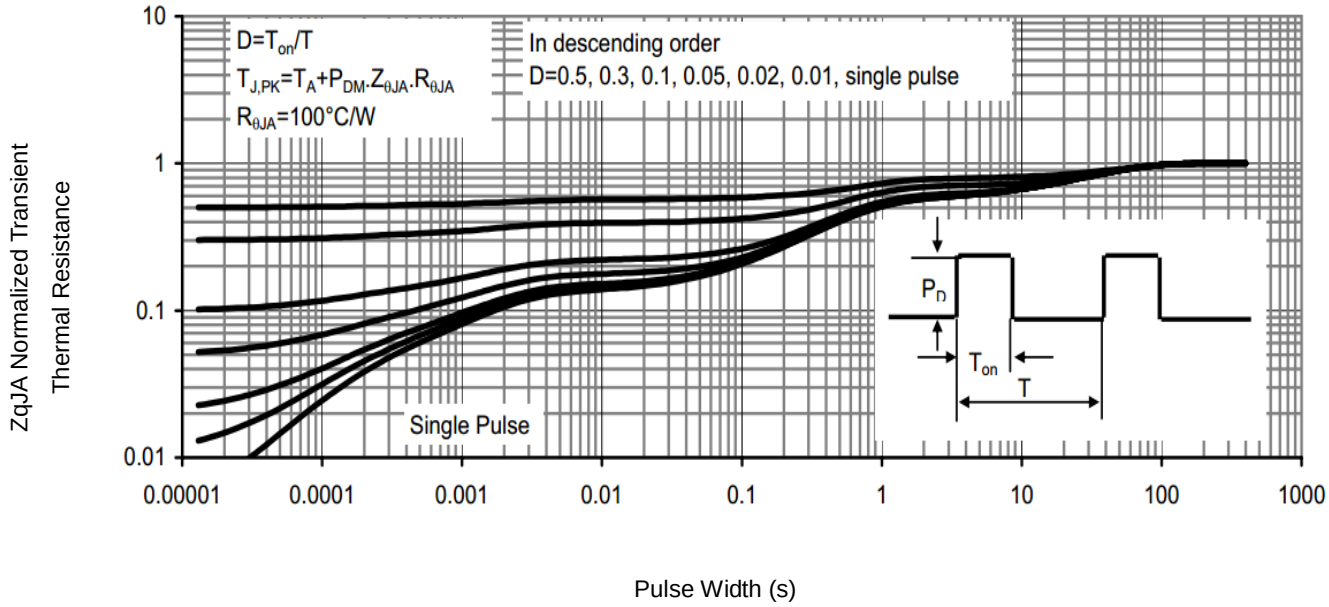


Fig9. Normalized Maximum Transient Thermal Impedance

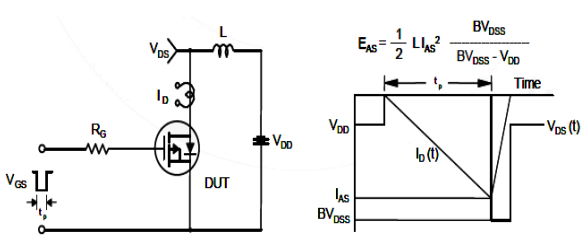


Fig10. Unclamped Inductive Test Circuit and waveforms

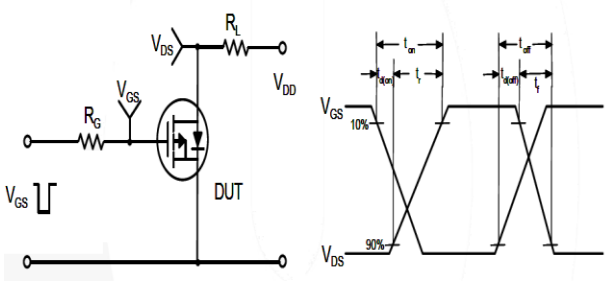
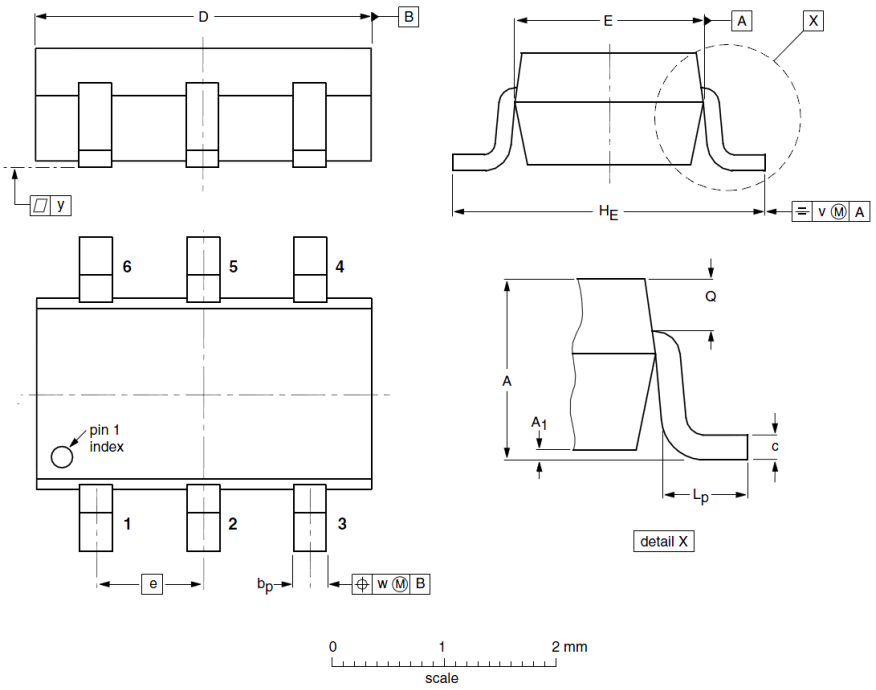


Fig11. Switching Time Test Circuit and waveforms

SOT23-6L Package Outline



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.90	1.07	1.45
b_p	0.30	0.35	0.40
D	2.70	2.92	3.10
e	--	0.95	--
L_p	0.30	0.45	0.60
v	--	0.20	--
y	--	0.10	
A_1	0.01	0.05	0.15
c	0.10	0.15	0.22
E	1.30	1.55	1.70
H_E	2.50	2.80	3.00
Q	0.23	0.29	0.33
w	--	0.20	--

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "bp" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "bp" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Customer Service

Sales and Service:
sales@vgsemi.com
Vanguard Semiconductor CO., LTD
TEL: (86-755) -26902410
FAX: (86-755) -26907027
WEB: **www.vgsemi.com**