

Features

- N-Channel, 5V Logic Level Control
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- Fast Switching
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

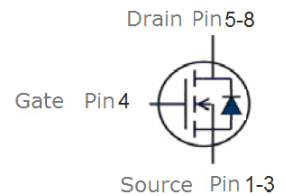

Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VS4618AE	PDFN3333	4618AE	5000PCS/Reel

V_{DS}	40	V
$R_{DS(on),TYP@ V_{GS}=10\text{ V}}$	10	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5\text{ V}}$	15	mΩ
I_D	43	A

PDFN3333


Pin1



Maximum ratings, at $T_A=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
V _{(BR)DSS}	Drain-Source breakdown voltage		40	V
I _S	Diode continuous forward current	T _C =25°C	43	A
I _D	Continuous drain current@VGS=10V	T _C =25°C	43	A
		T _C =100°C	27	A
I _{DM}	Pulse drain current tested ①	T _C =25°C	172	A
EAS	Avalanche energy, single pulsed ②		32	mJ
P _D	Maximum power dissipation	T _C =25°C	30	W
VGS	Gate-Source voltage		±20	V
T _{STG} T _J	Storage and operating temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	4.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	35	$^\circ\text{C/W}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j =25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V,V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =40V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	1.3	1.9	2.4	V
R _{DS(ON)}	Drain-Source On-State Resistance③	V _{GS} =10V, I _D =15A	--	10	13	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance③	V _{GS} =4.5V, I _D =10A	--	15	19	mΩ
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V,V _{GS} =0V, f=1MHz	1100	1295	1500	pF
C _{oss}	Output Capacitance		50	100	150	pF
C _{rss}	Reverse Transfer Capacitance		40	80	120	pF
R _g	Gate Resistance	f=1MHz	--	4.1	--	Ω
Q _g	Total Gate Charge	V _{DS} =20V,I _D =15A, V _{GS} =10V	--	22	--	nC
Q _{gs}	Gate-Source Charge		--	4.5	--	nC
Q _{gd}	Gate-Drain Charge		--	4.2	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =15A, R _G =3.0Ω, V _{GS} =10V	--	7.5	--	nS
t _r	Turn-on Rise Time		--	3.8	--	nS
t _{d(off)}	Turn-Off Delay Time		--	24	--	nS
t _f	Turn-Off Fall Time		--	5.5	--	nS
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =15A,V _{GS} =0V	--	0.8	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C,I _{sd} =15A, V _{GS} =0V	--	8.5	--	nS
Q _{rr}	Reverse Recovery Charge	di/dt=500A/μs		8		nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{jmax} , starting $T_j = 25^{\circ}\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 9A$, $V_{GS} = 10V$. Part not recommended for use above this value
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

Typical Characteristics

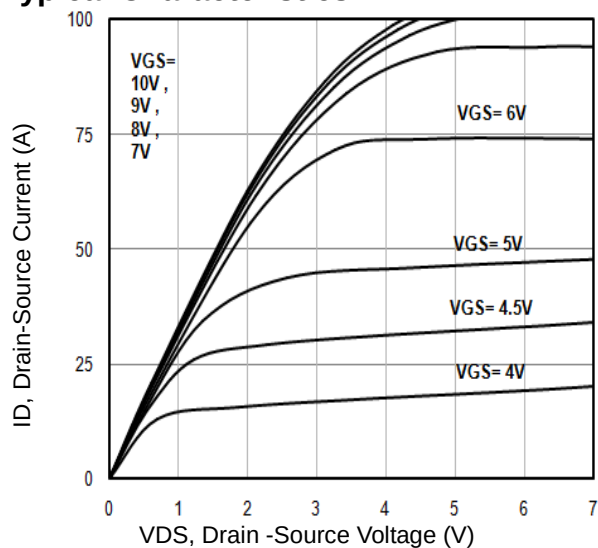


Fig1. Typical Output Characteristics

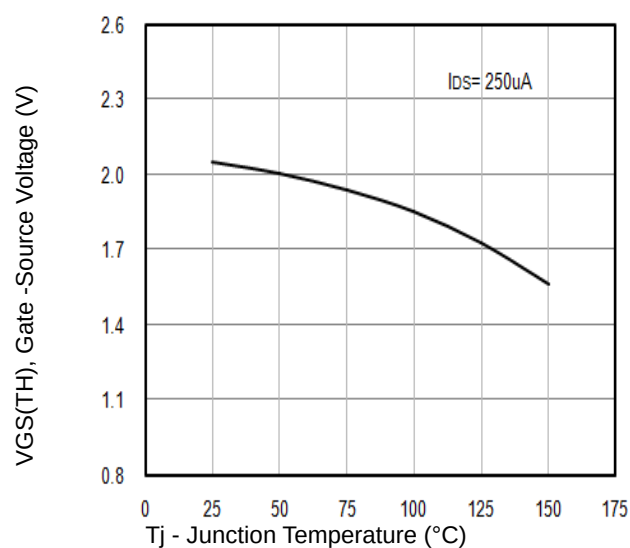


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_J

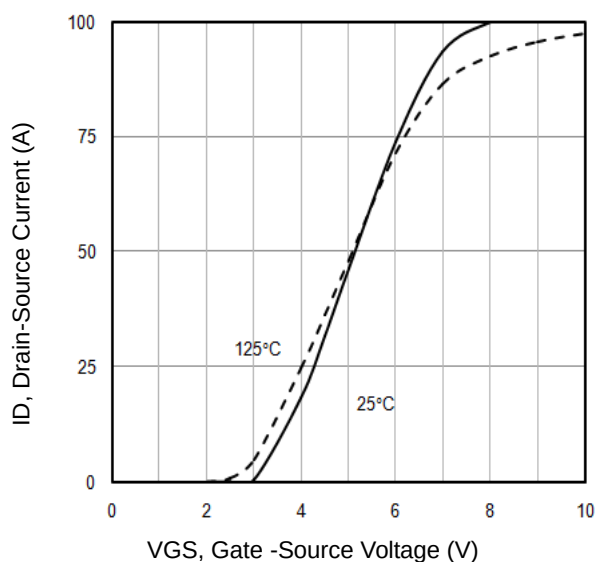


Fig3. Typical Transfer Characteristics

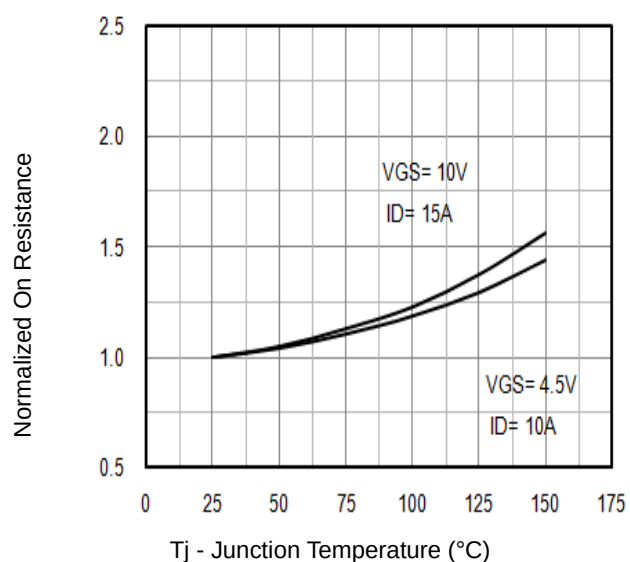


Fig4. Normalized On-Resistance Vs. T_J

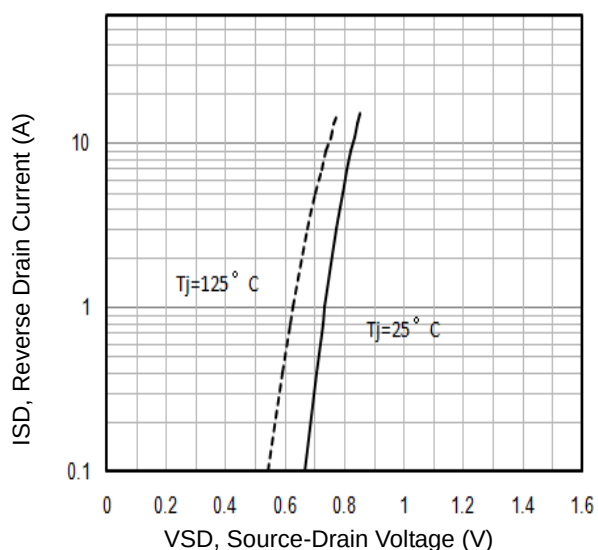


Fig5. Typical Source-Drain Diode Forward Voltage

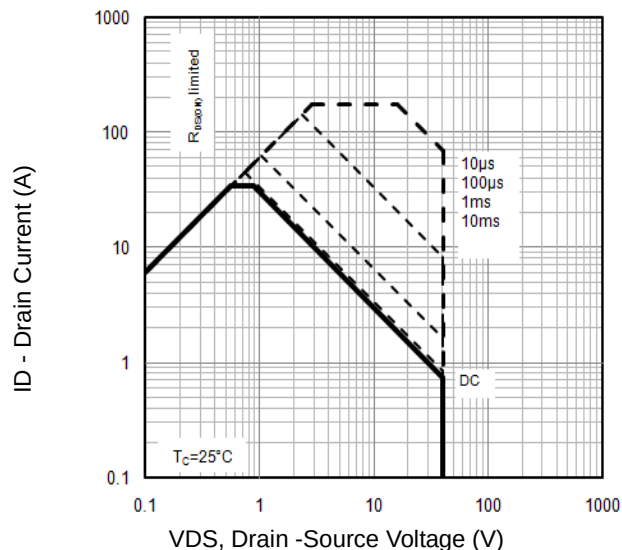


Fig6. Maximum Safe Operating Area



Typical Characteristics

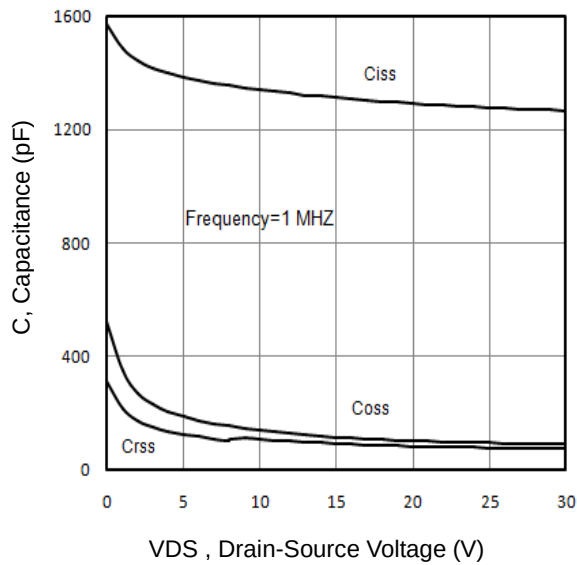


Fig7. Typical Capacitance Vs. Drain-Source Voltage

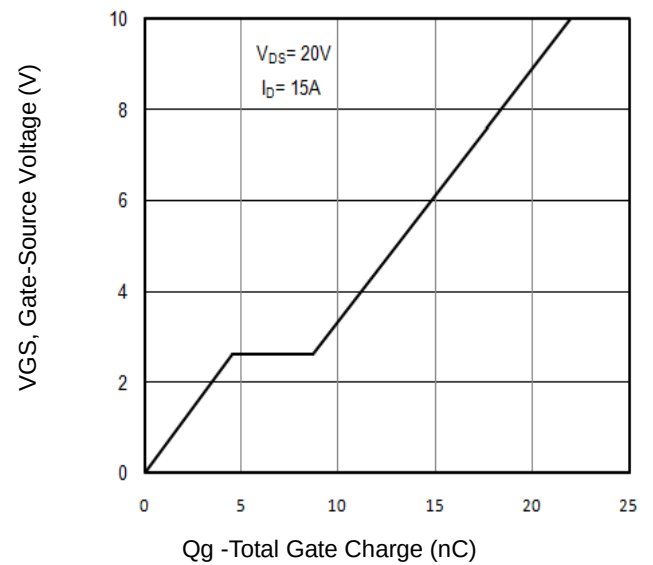


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

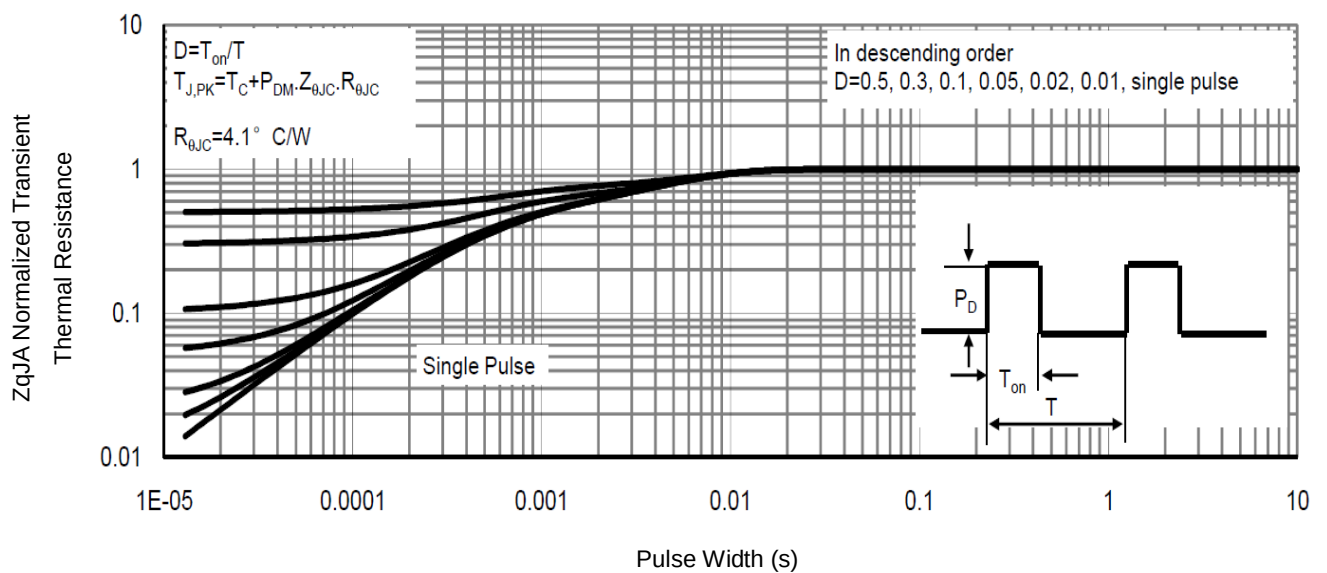


Fig9. Normalized Maximum Transient Thermal Impedance

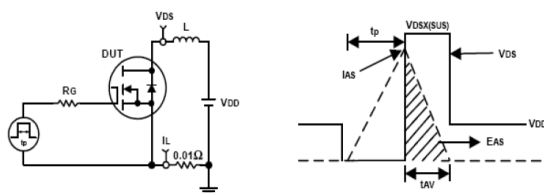


Fig10. Unclamped Inductive Test Circuit and waveforms

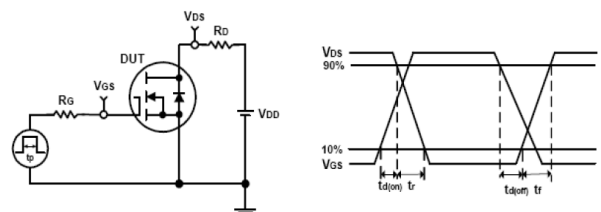
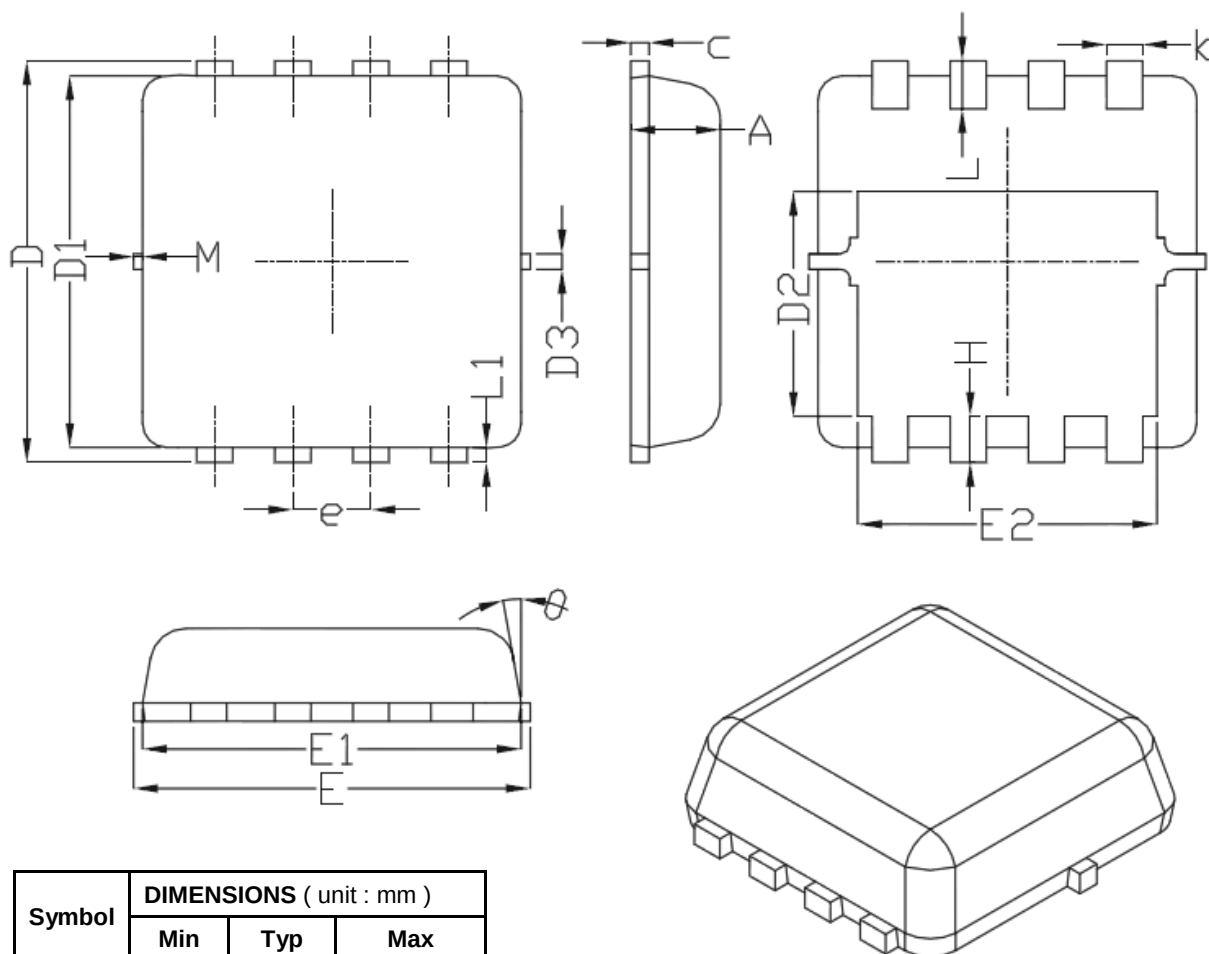


Fig11. Switching Time Test Circuit and waveforms

PDFN3333 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.7	0.75	0.8
b	0.25	0.3	0.35
C	0.1	0.15	0.25
D	3.25	3.35	3.45
D1	3	3.1	3.2
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.2	3.3	3.4
E1	3	3.15	3.2
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.3	0.39	0.5
L	0.3	0.4	0.5
L1	--	0.13	--
θ	--	10°	12°
M	*	*	0.15
* Not specified			

Notes:

1. Follow JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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