

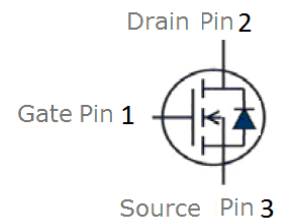
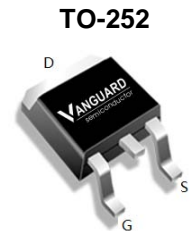
Features

- N-Channel, 5V Logic Level Control
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- VitoMOS[®] Technology
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Tape and reel information
VS6412ADL	TO-252	6412AD	2500PCS/Reel

V_{DS}	60	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	14	m Ω
$R_{DS(on),TYP} @ V_{GS}=4.5\text{ V}$	18	m Ω
I_D	40	A



Maximum ratings, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	60	V
I_S	Diode continuous forward current	$T_C=25^\circ\text{C}$ 40	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C=25^\circ\text{C}$ 40	A
		$T_C=100^\circ\text{C}$ 28	A
I_{DM}	Pulse drain current tested ①	$T_C=25^\circ\text{C}$ 160	A
EAS	Avalanche energy, single pulsed ②	25	mJ
P_D	Maximum power dissipation	$T_C=25^\circ\text{C}$ 51	W
V_{GS}	Gate-Source voltage	± 20	V
$T_{STG} T_J$	Storage and operating temperature range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.95	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	100	$^\circ\text{C/W}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =60V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.8	2.4	V
R _{DS(ON)}	Drain-Source On-State Resistance③	V _{GS} =10V, I _D =15A	--	14	18	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance③	V _{GS} =4.5V, I _D =10A	--	18	21	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	900	995	1100	pF
C _{oss}	Output Capacitance		50	95	150	pF
C _{rss}	Reverse Transfer Capacitance		40	85	140	pF
R _g	Gate Resistance	f=1MHz		3		Ω
Q _g	Total Gate Charge	V _{DS} =30V, I _D =15A, V _{GS} =10V	--	19	--	nC
Q _{gs}	Gate-Source Charge		--	5	--	nC
Q _{gd}	Gate-Drain Charge		--	6	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =15A, R _G =3Ω, V _{GS} =10V	--	12	--	nS
t _r	Turn-on Rise Time		--	6	--	nS
t _{d(off)}	Turn-Off Delay Time		--	41	--	nS
t _f	Turn-Off Fall Time		--	48	--	nS
Source- Drain Diode Characteristics @ T_j= 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =15A, V _{GS} =0V	--	0.8	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =15A, di/dt=100A/μs	--	19	--	nS
Q _{rr}	Reverse Recovery Charge				13	

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{jmax}, starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 10A, V_{GS} = 10V. Part not recommended for use above this value
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

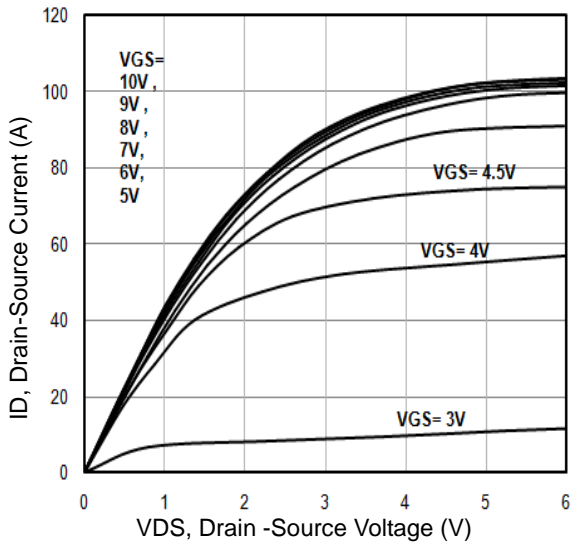


Fig1. Typical Output Characteristics

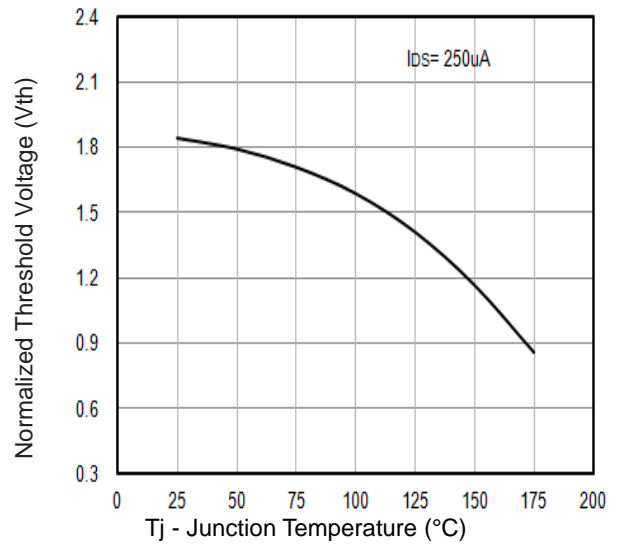


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

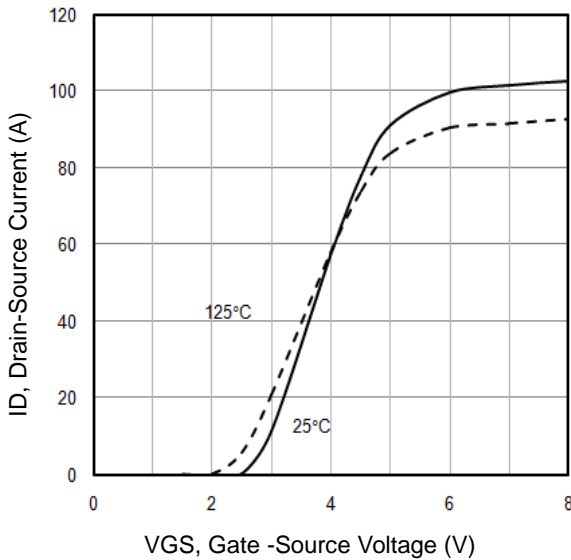


Fig3. Typical Transfer Characteristics

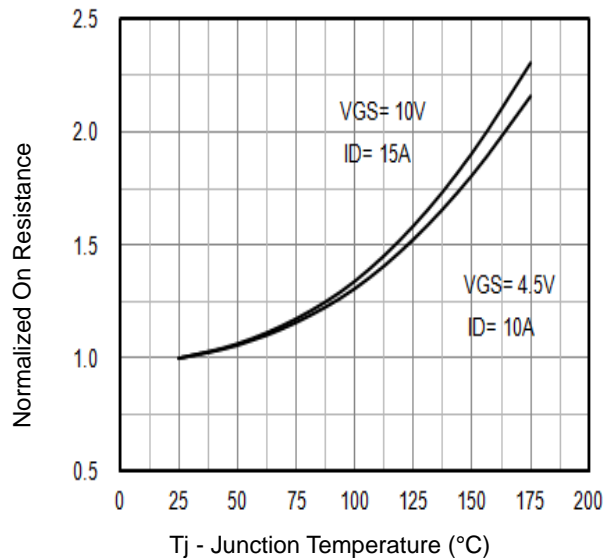


Fig4. Normalized On-Resistance Vs. T_j

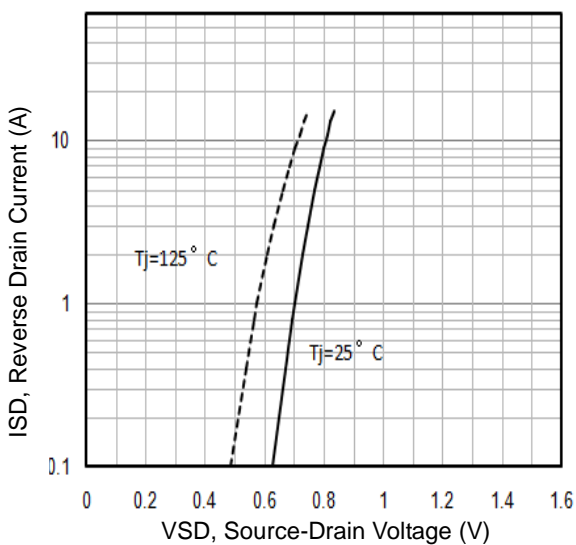


Fig5. Typical Source-Drain Diode Forward Voltage

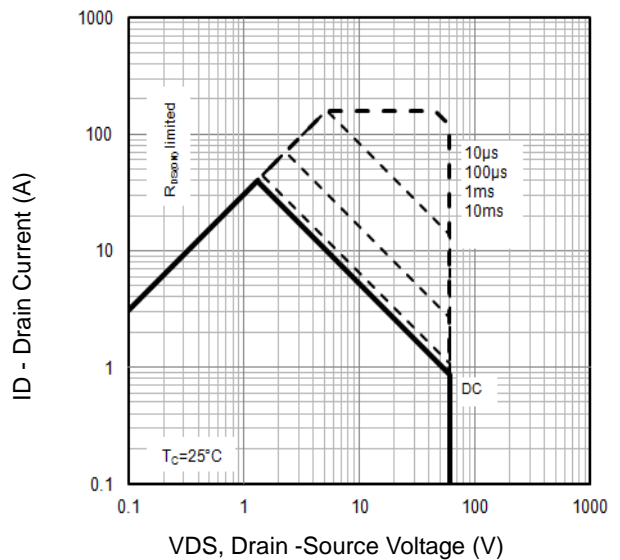


Fig6. Maximum Safe Operating Area

Typical Characteristics

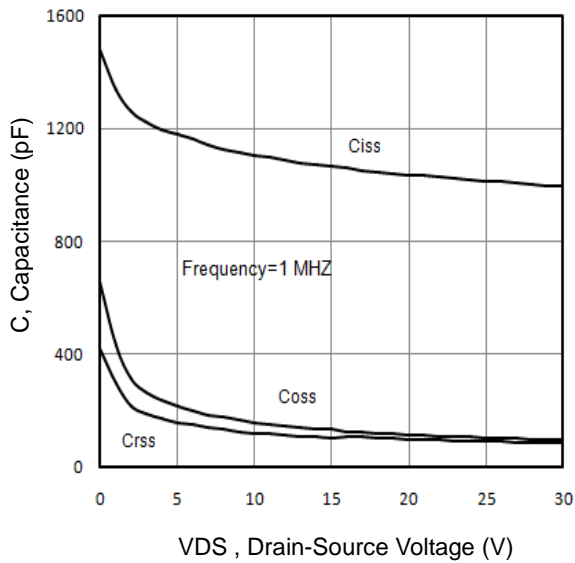


Fig7. Typical Capacitance Vs.Drain-Source Voltage

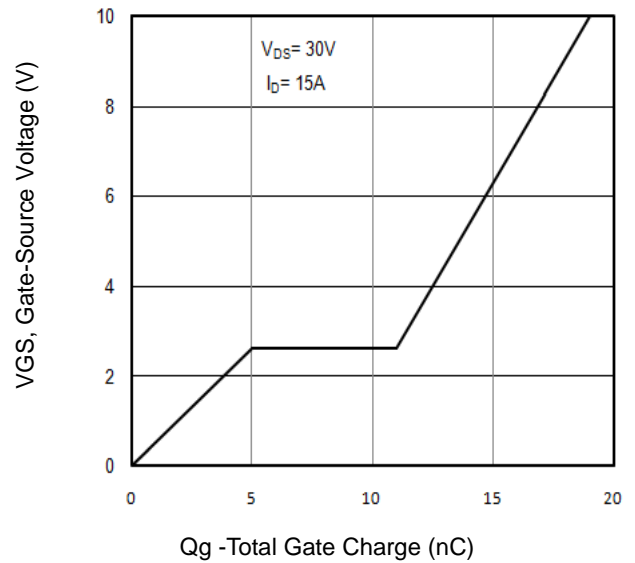


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

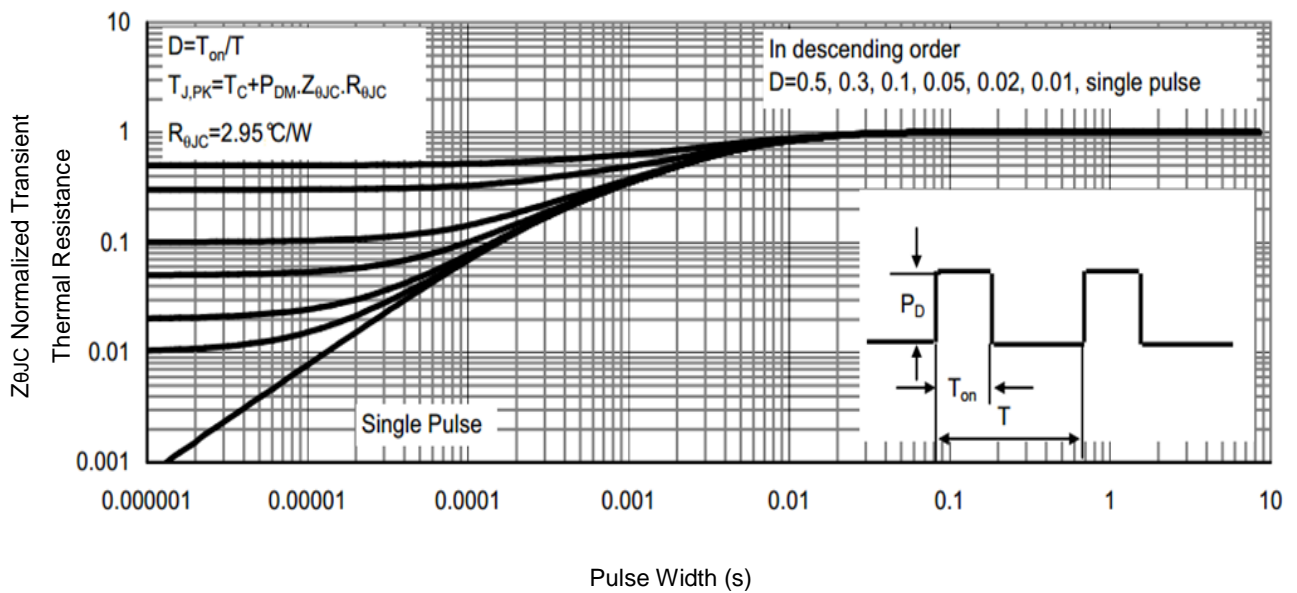


Fig9 . Normalized Maximum Transient Thermal Impedance

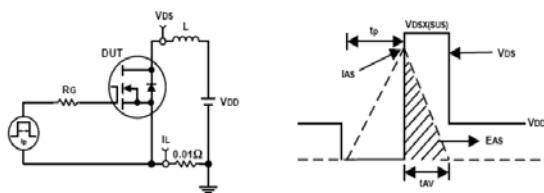


Fig10. Unclamped Inductive Test Circuit and waveforms

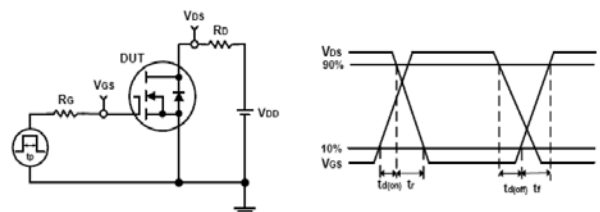
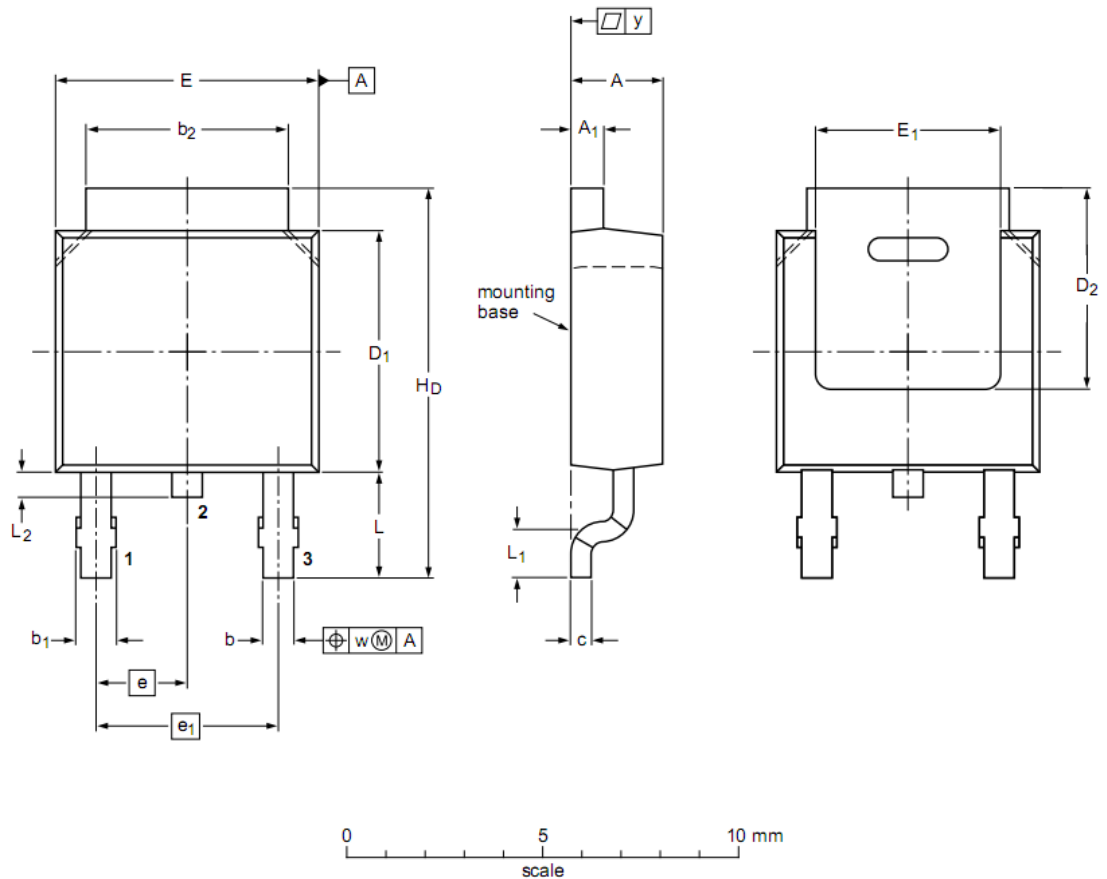


Fig11. Switching Time Test Circuit and waveforms

TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A ₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b ₁	0.77	0.85	1.14
b ₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D ₁	5.98	6.10	6.223
D ₂	5.21	--	--
E	6.40	6.60	6.731
E ₁	4.40	--	--
e	2.286 BSC		
e ₁	--	4.57	--
H _D	9.40	10.00	10.40
L	2.743 REF		
L ₁	1.40	1.52	1.77
L ₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

Customer Service

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