

## Features

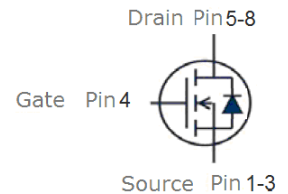
- N-Channel, 5V Logic Level Control
- Enhancement mode
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5\text{ V}$
- VitoMOS<sup>®</sup> Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Tape and reel information
VS6412AEL	PDFN3333	6412AE	5000PCS/Reel

$V_{DS}$	60	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	15	m $\Omega$
$R_{DS(on),TYP} @ V_{GS}=4.5\text{ V}$	17	m $\Omega$
$I_D$	33	A

PDFN3333



## Maximum ratings, at $T_A = 25^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	60	V
$I_S$	Diode continuous forward current	$T_C = 25^\circ\text{C}$ 33	A
$I_D$	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C = 25^\circ\text{C}$ 33	A
		$T_C = 100^\circ\text{C}$ 21	A
$I_{DM}$	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$ 132	A
EAS	Avalanche energy, single pulsed ②	121	mJ
$P_D$	Maximum power dissipation	$T_C = 25^\circ\text{C}$ 32	W
$V_{GS}$	Gate-Source voltage	$\pm 20$	V
$T_{STG} T_J$	Storage and operating temperature range	-55 to 150	$^\circ\text{C}$

## Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	3.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	35	$^\circ\text{C/W}$

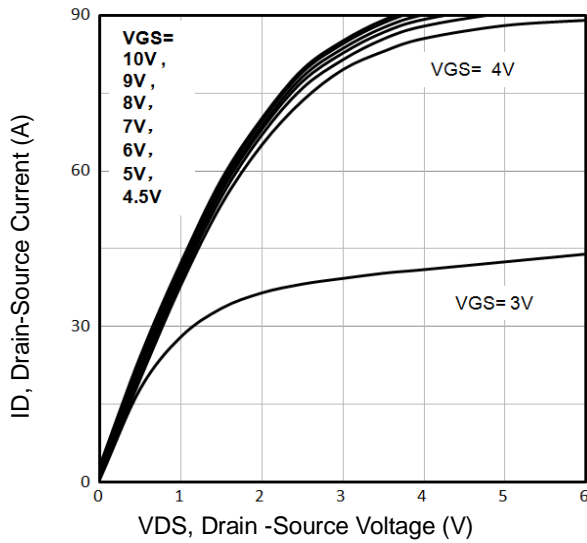


Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics @ T<sub>j</sub>=25°C (unless otherwise stated)</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	--	--	0.1	μA
	Zero Gate Voltage Drain Current(T <sub>j</sub> =125°C)	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	--	--	100	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	--	--	±100	nA
V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.6	2.5	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>③</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =15A	--	15	17	mΩ
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>③</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	--	17	20	mΩ
<b>Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz	--	1240	--	pF
C <sub>oss</sub>	Output Capacitance		--	95	--	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	85	--	pF
R <sub>g</sub>	Gate Resistance	f=1MHz	--	2.4	--	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V	--	21	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	6	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	8.5	--	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =30V, I <sub>D</sub> =5A, R <sub>G</sub> =6.8Ω, V <sub>GS</sub> =10V	--	12	--	nS
t <sub>r</sub>	Turn-on Rise Time		--	8.5	--	nS
t <sub>d(off)</sub>	Turn-Off Delay Time		--	42	--	nS
t <sub>f</sub>	Turn-Off Fall Time		--	6	--	nS
<b>Source- Drain Diode Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
V <sub>SD</sub>	Forward on voltage	I <sub>SD</sub> =15A, V <sub>GS</sub> =0V	--	0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	T <sub>j</sub> =25°C, I <sub>sd</sub> =5A, V <sub>GS</sub> =0V di/dt=100A/μs	--	22	--	nS
Q <sub>rr</sub>	Reverse Recovery Charge		--	86	--	nC

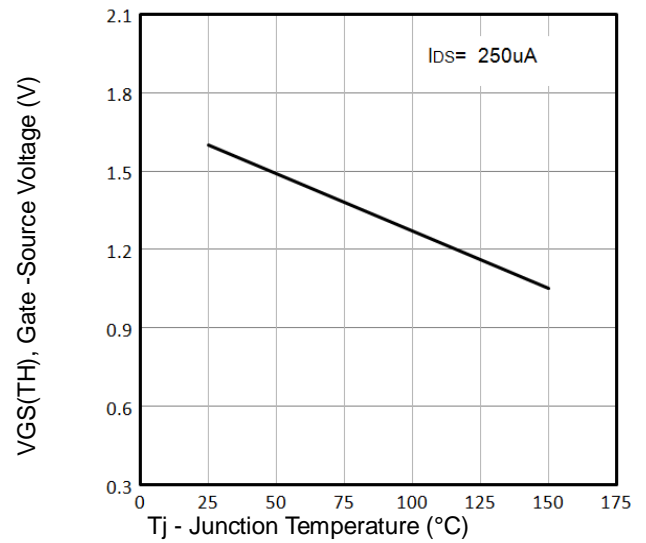
NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>jmax</sub>, starting T<sub>j</sub> = 25°C, L = 0.5mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 22A, V<sub>GS</sub> = 10V. Part not recommended for use above this value
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

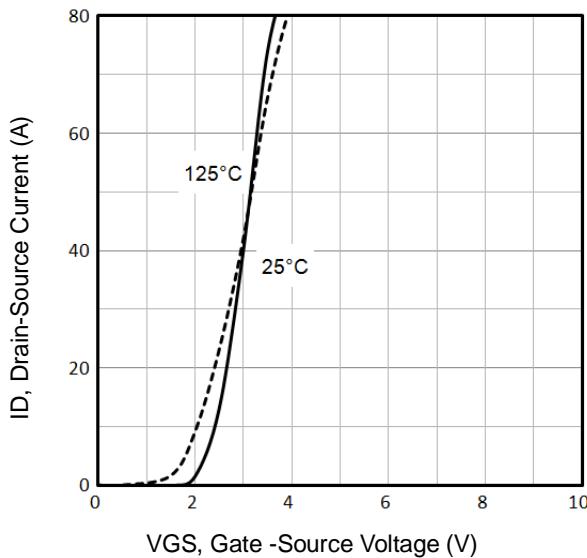
**Typical Characteristics**



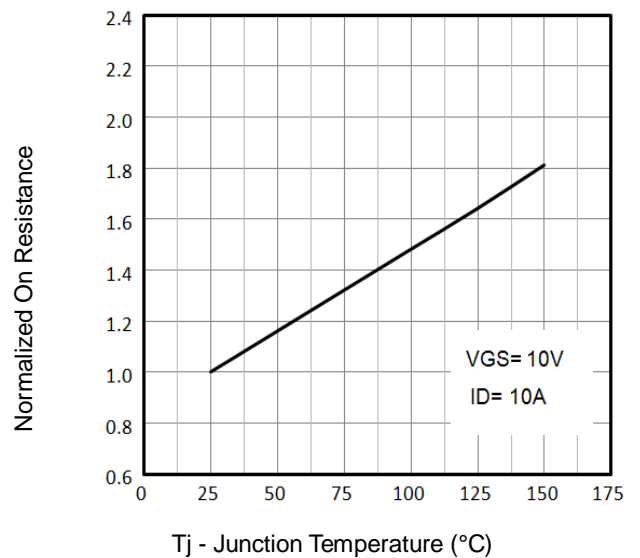
**Fig1.** Typical Output Characteristics



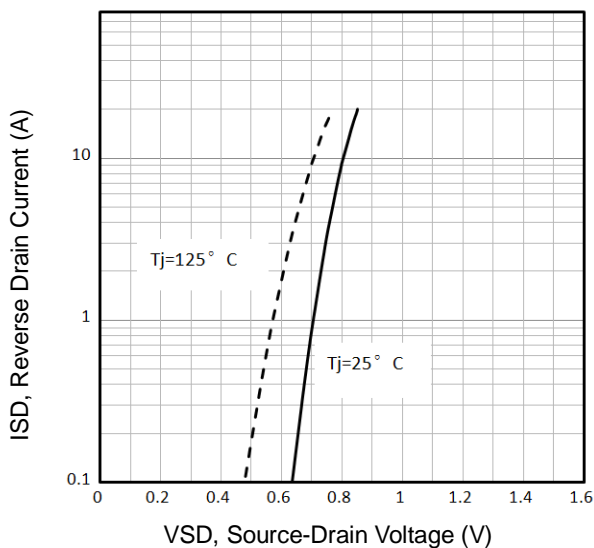
**Fig2.**  $V_{GS(TH)}$  Gate-Source Voltage Vs.  $T_j$



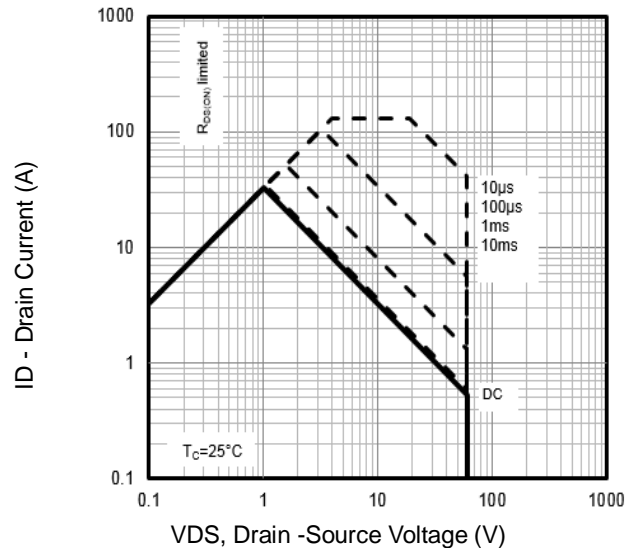
**Fig3.** Typical Transfer Characteristics



**Fig4.** Normalized On-Resistance Vs.  $T_j$



**Fig5.** Typical Source-Drain Diode Forward Voltage



**Fig6.** Maximum Safe Operating Area

Typical Characteristics

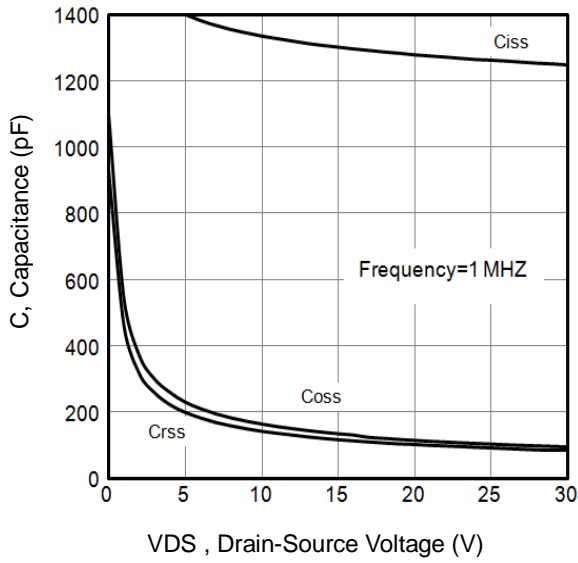


Fig7. Typical Capacitance Vs.Drain-Source Voltage

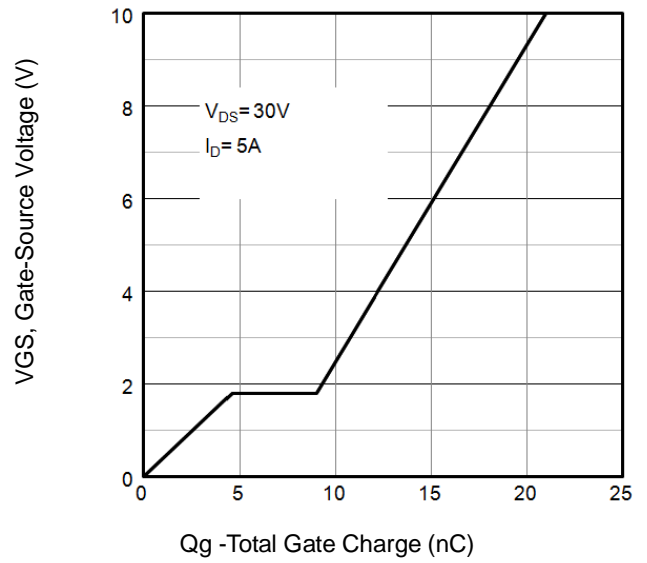


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

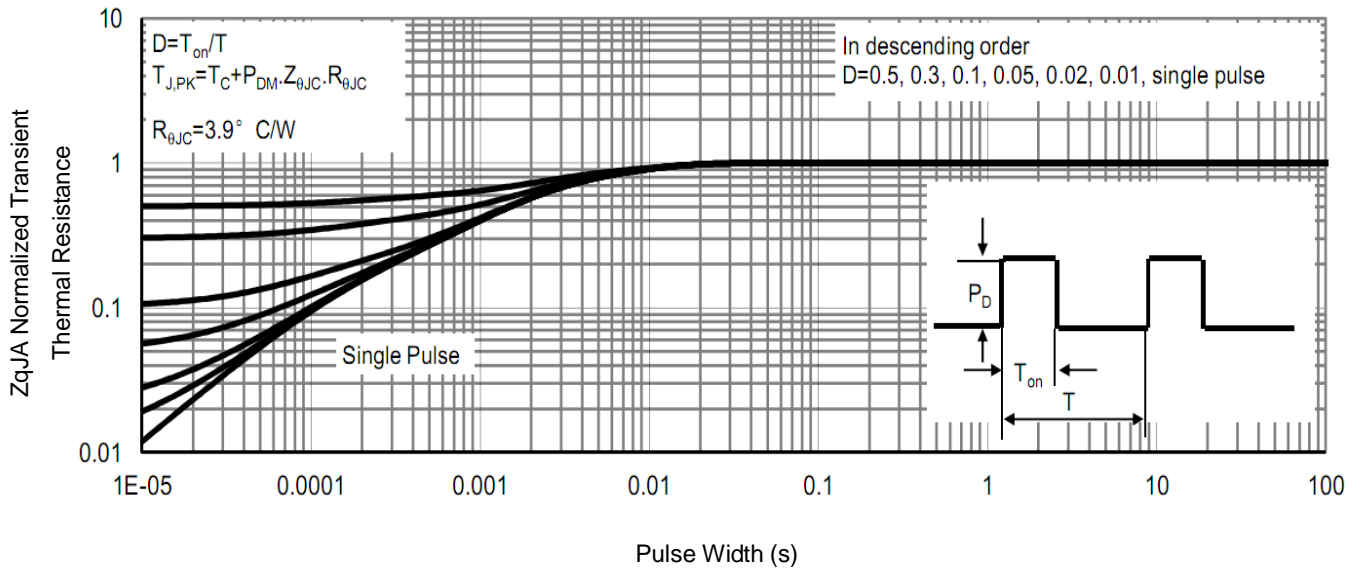


Fig9. Normalized Maximum Transient Thermal Impedance

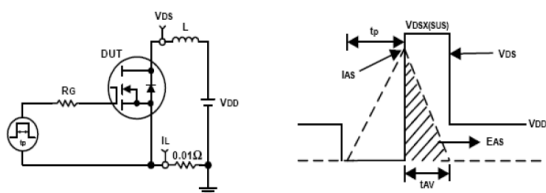


Fig10. Unclamped Inductive Test Circuit and waveforms

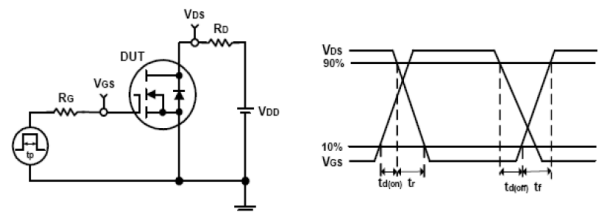
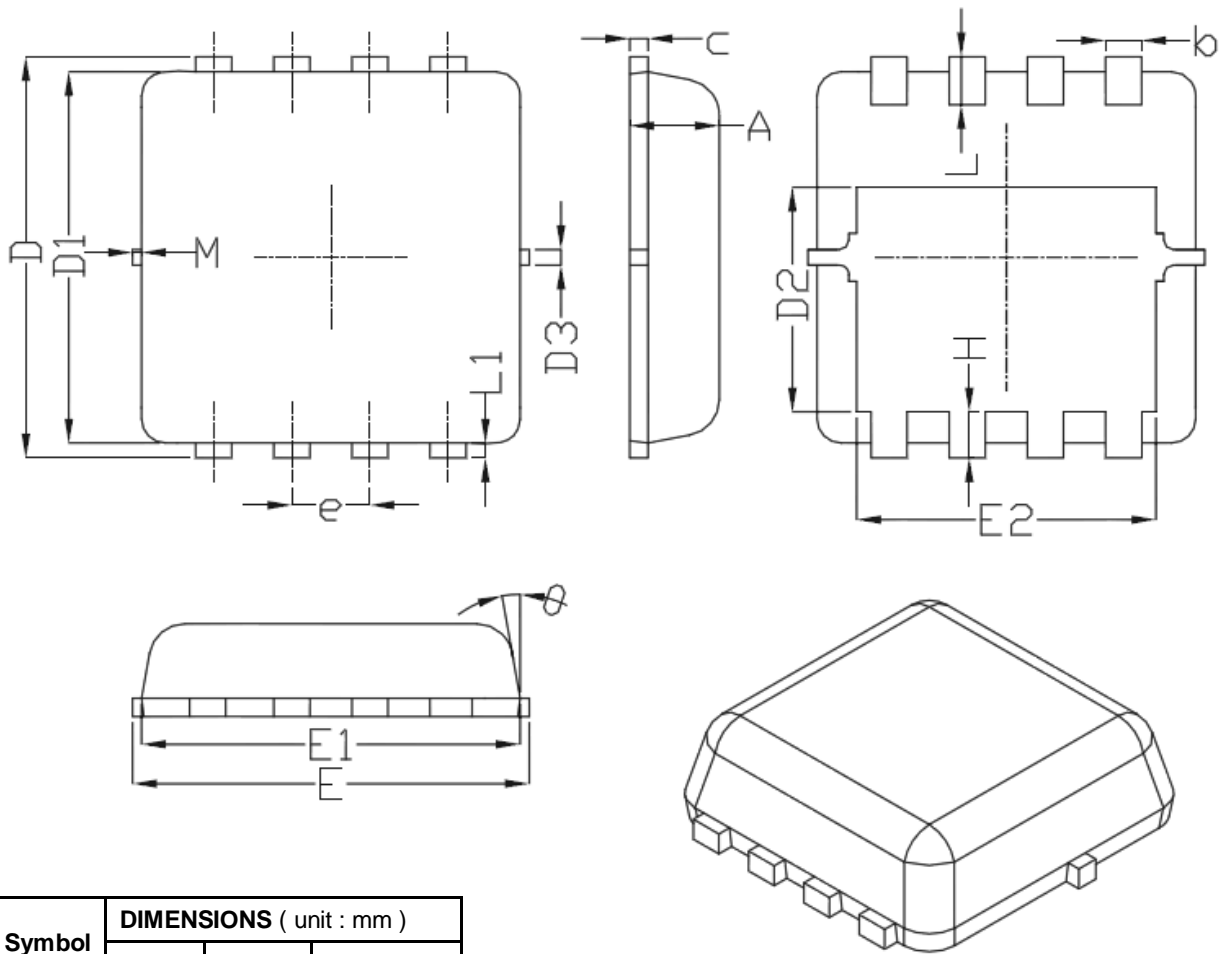


Fig11. Switching Time Test Circuit and waveforms

**PDFN3333 Package Outline Data**



Symbol	DIMENSIONS ( unit : mm )		
	Min	Typ	Max
A	0.7	0.75	0.8
b	0.25	0.3	0.35
C	0.1	0.15	0.25
D	3.25	3.35	3.45
D1	3	3.1	3.2
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.2	3.3	3.4
E1	3	3.15	3.2
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.3	0.39	0.5
L	0.3	0.4	0.5
L1	--	0.13	--
θ	--	10°	12°
M	*	*	0.15
* Not specified			

Notes:

1. Follow JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

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