

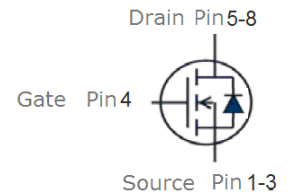
Features

- N-Channel, 5V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- VitoMOS[®] Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Tape and reel information
VS6412ASL	SOP8	6412AS	3000PCS/Reel

V_{DS}	60	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	14.5	m Ω
$R_{DS(on),TYP} @ V_{GS}=4.5\text{ V}$	16.0	m Ω
I_D	10	A



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	60	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_A = 25^\circ\text{C}$	3 A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	10 A
		$T_A = 100^\circ\text{C}$	6 A
I_{DM}	Pulse drain current tested ①	$T_A = 25^\circ\text{C}$	40 A
EAS	Avalanche energy, single pulsed ②	121	mJ
P_D	Maximum power dissipation	$T_A = 25^\circ\text{C}$	3.1 W
MSL		Level 3	
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	24	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	$^\circ\text{C/W}$



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	--	--	0.1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =60V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.6	2.4	V
R _{DS(ON)}	Drain-Source On-State Resistance ③	V _{GS} =10V, I _D =10A	--	14.5	18.0	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ③	V _{GS} =4.5V, I _D =5A	--	16.0	20.0	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	1150	1250	1350	pF
C _{oss}	Output Capacitance		71	91	111	pF
C _{rss}	Reverse Transfer Capacitance		49	69	89	pF
R _g	Gate Resistance	f=1MHz	--	2.4	--	Ω
Q _g	Total Gate Charge	V _{DS} =30V, I _D =5A, V _{GS} =10V	--	21	--	nC
Q _{gs}	Gate-Source Charge		--	6	--	nC
Q _{gd}	Gate-Drain Charge		--	8.5	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =5A, R _G =6.8Ω, V _{GS} =10V	--	12	--	nS
t _r	Turn-on Rise Time		--	8.5	--	nS
t _{d(off)}	Turn-Off Delay Time		--	42	--	nS
t _f	Turn-Off Fall Time		--	6	--	nS
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =10A, V _{GS} =0V	--	0.80	1.0	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =5A, V _{GS} =0V di/dt=100A/μs	--	22	--	nS
Q _{rr}	Reverse Recovery Charge		86	--	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{jmax}, starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 22A, V_{GS} = 10V. Part not recommended for use above this value
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

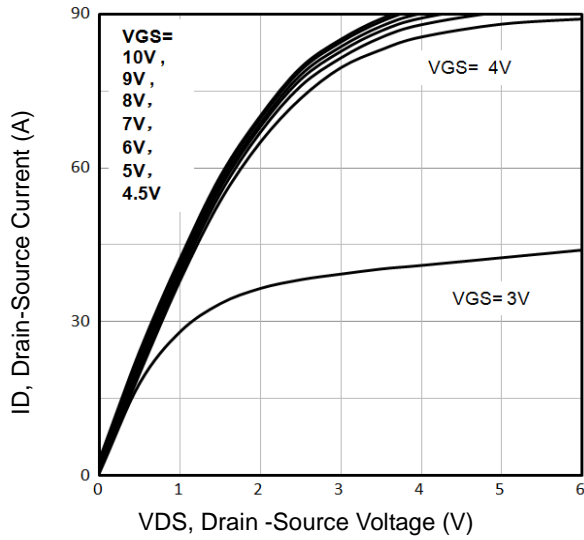


Fig1. Typical Output Characteristics

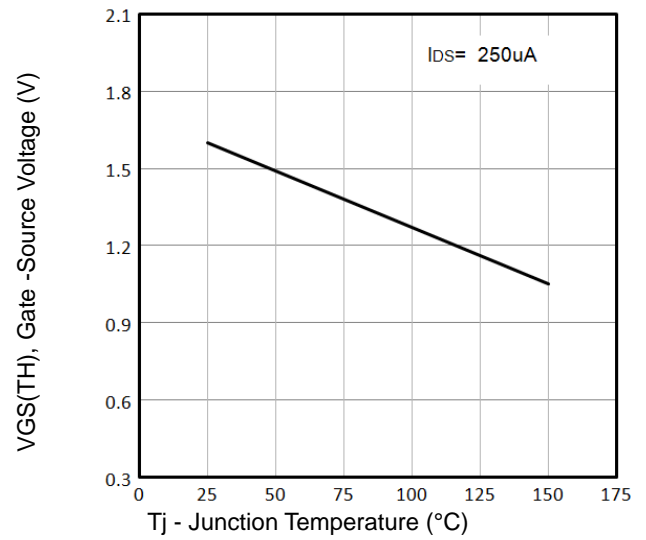


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

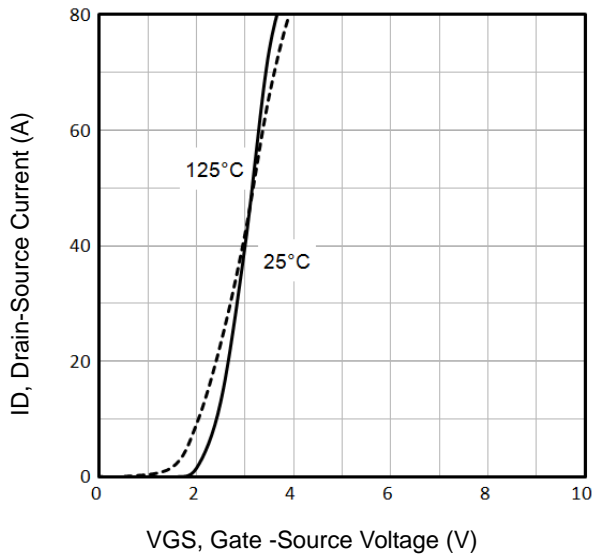


Fig3. Typical Transfer Characteristics

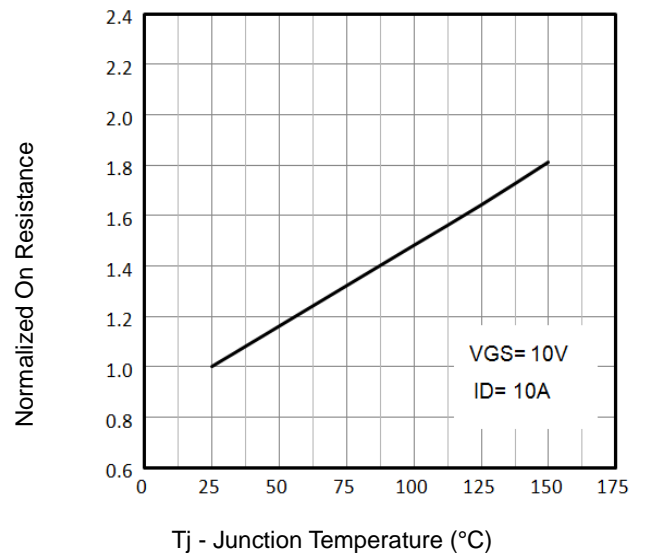


Fig4. Normalized On-Resistance Vs. T_j

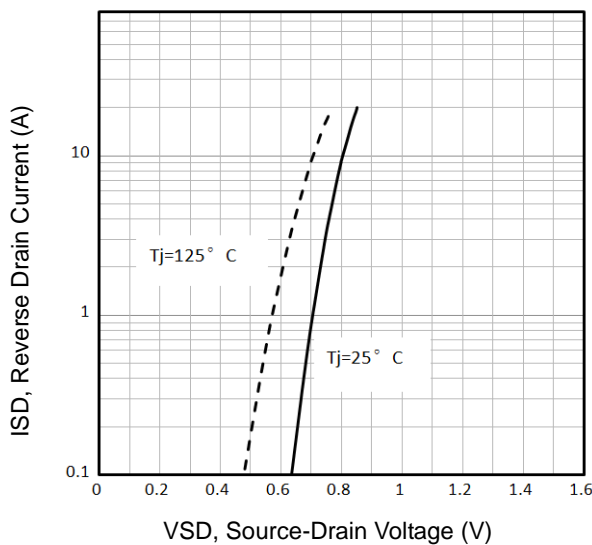


Fig5. Typical Source-Drain Diode Forward Voltage

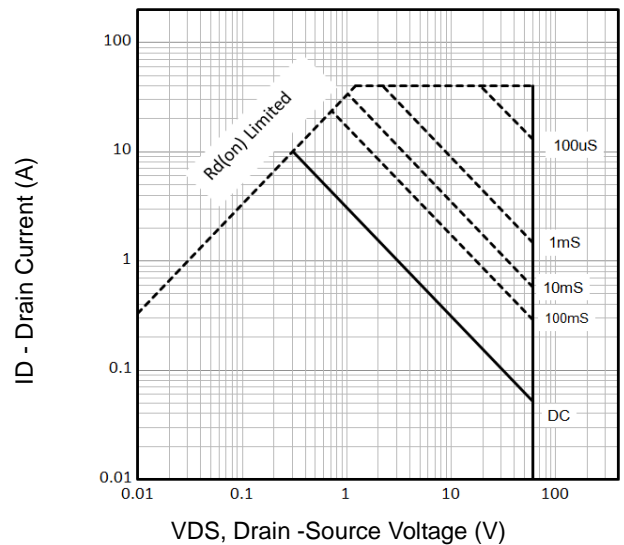


Fig6. Maximum Safe Operating Area

Typical Characteristics

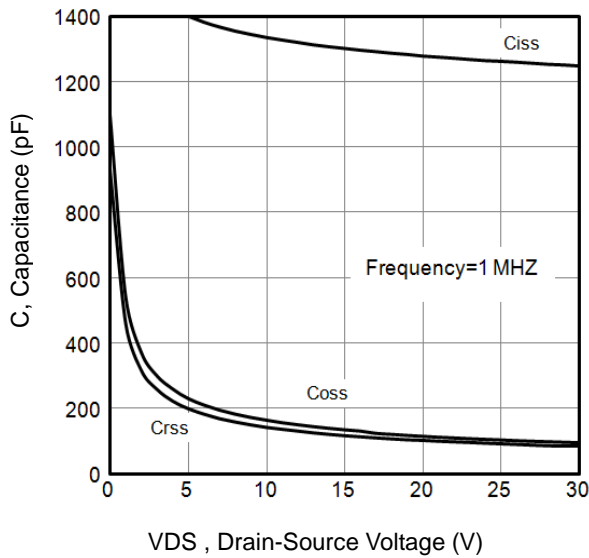


Fig7. Typical Capacitance Vs.Drain-Source Voltage

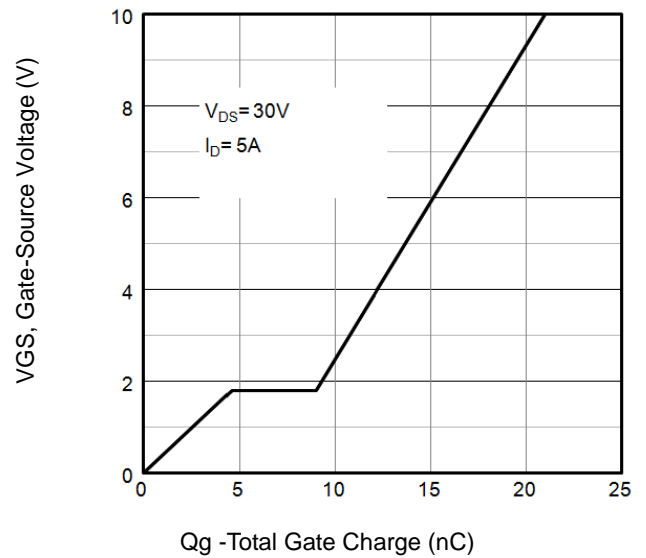


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

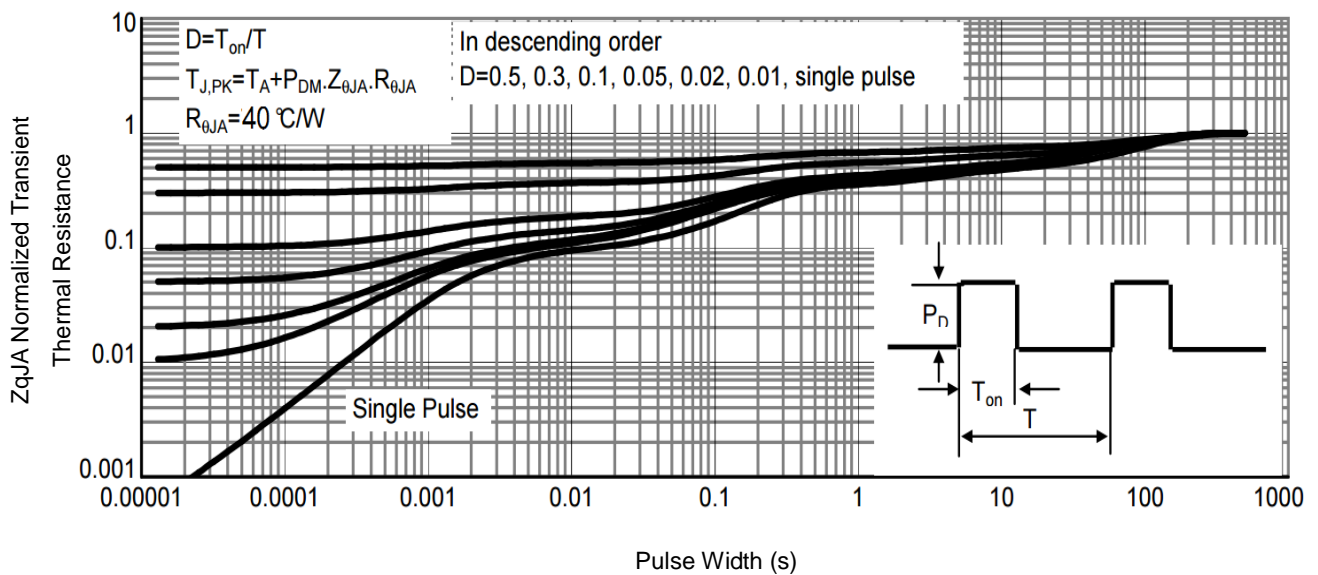


Fig9. Normalized Maximum Transient Thermal Impedance

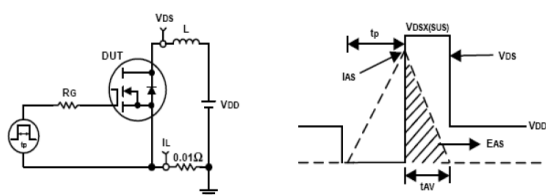


Fig10. Unclamped Inductive Test Circuit and waveforms

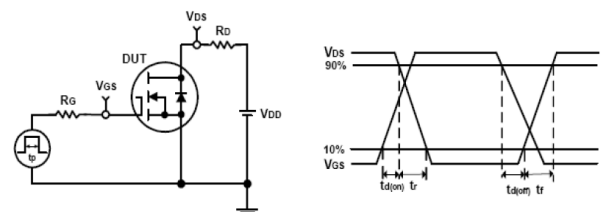
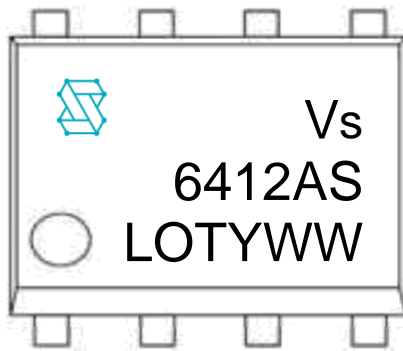


Fig11. Switching Time Test Circuit and waveforms



Marking Information



1st line: Company Code (Vs), Company Logo

2nd line: Part Number (6412AS)

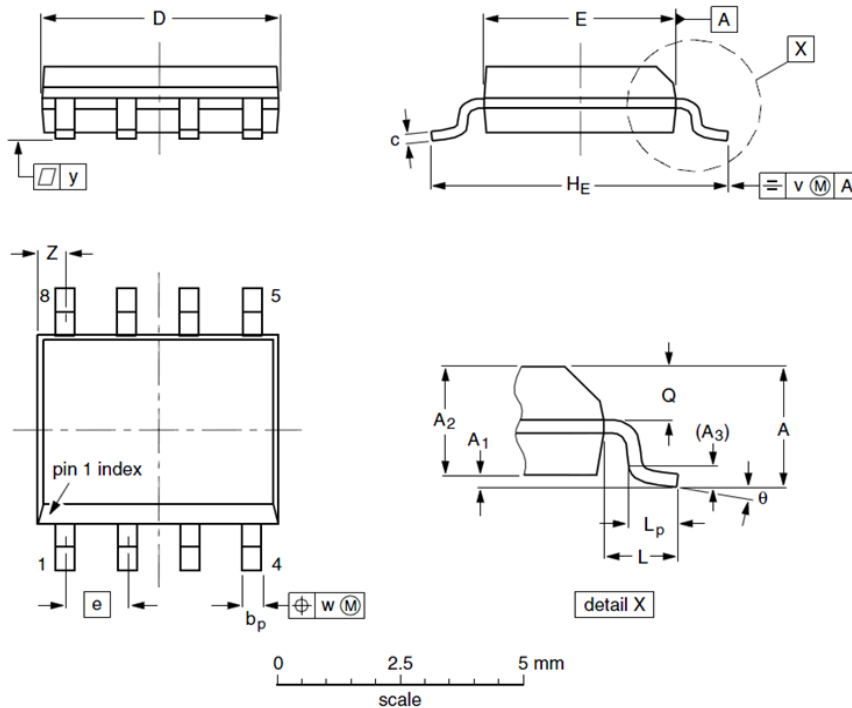
3rd line: Date code (LOTYWW)

LOT: Wafer Lot Number

Y: Year Code, e.g. E means 2017

WW: Week Code

SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A ₁	0.10	0.18	0.25
A ₂	1.25	1.35	1.50
A ₃	--	0.25	--
b _p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H _E	5.80	6.00	6.20
L	--	1.05	--
L _p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "b_p" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "b_p" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Customer Service

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