VS6502

VGA Color CMOS Image Sensor Module

Features

- **Small physical size: integrated lens in a SmOP (Small Optical Package)**
- **640 x 480 VGA resolution**
- **Up to 30 frame/s VGA, 60 frame/s QVGA**
- **On-chip 10-bit ADC**
- **Automatic dark calibration**
- **2.6 V to 3.6 V power supply**
- **I^2C communications**
- **Low power suspend mode**
- **4 or 5 wire nibble output**
- **Socket available separately**

Description

The VS6502 is a VGA resolution SmOP sensor module. SmOP technology combines the image sensor and fixed focus lens system in a single module. The SmOP sensor module is connected to the PCB either via a socket or flex option. The socket allows the PCB to use standard reflow soldering techniques.

The sensor outputs 10-bit raw digital image data which directly interface to a range of STMicroelectronics companion processors via 4/5 wire interface.

An I^2C interface allows the processor to configure the device and control exposure and gain settings.

There are three different digital video output formats:

- VGA mode - 640 x 480 image size
- Sub-sampled QVGA mode - 320 x 240 image size
- Window Of Interest QVGA mode - 320 x 240 pixel

Applications

- Miniature USB web cameras (STV0676 - STV0674)
- Embedded cameras (STV0676 - STV0674): Handhelds, Cell phones, Network cameras
- Digital stills cameras (STV0674): Minicam, miniature USB flash drive cameras
- Digital video cameras (STV0674)

Technical Specifications

Pixel resolution	644 x 484 (VGA)
Pixel size	5.6 µm x 5.6 µm
Array size	3.6 mm x 2.7 mm
Dynamic range	> 52 dB
Analogue gain	0 to 24dB
Sensitivity (typical)	2.05 V / lux-s
Signal/Noise ratio	+ 37 dB
Supply voltage	2.6 to 3.6 V
Power consumption	Active (30 frame/s) < 30 mA
	Suspend (no clk) < 10 µA
Operating temperature	0 to 40°C
Package size	10.6 mm x 8.7 mm x 5.8 mm
Lens	47° HFOV, f#2.8
Package type	14 pad SmOP

Ordering information

Ordering code	Description
VS6502V015	VS6502 sensor module
XS0015/TR	Socket for sensor module

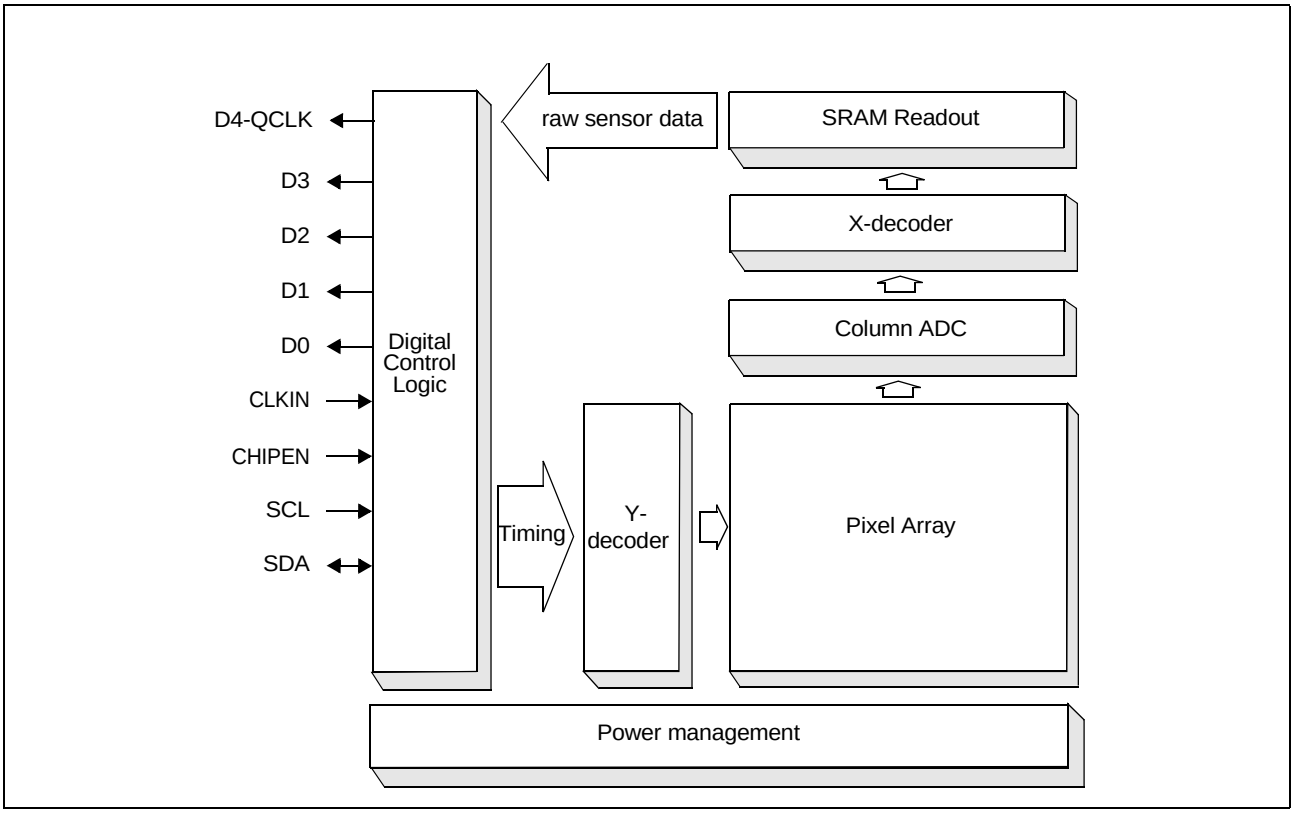
Table of Contents

1 Overview

1.1 Sensor overview

The VS6502 image sensor produces raw digital video data at up to 30 frames per second VGA or 60 frames per second QVGA. The image data is digitized using an internal 10-bit ADC. The resulting 10-bit output data includes embedded codes for synchronization. There are two data output modes; 4-bit nibbles with separate data qualification clock (QCK) or 5-bit nibbles without qualification clock. The sensor is controlled using an I^2C interface.

Figure 1: VS6502 block diagram

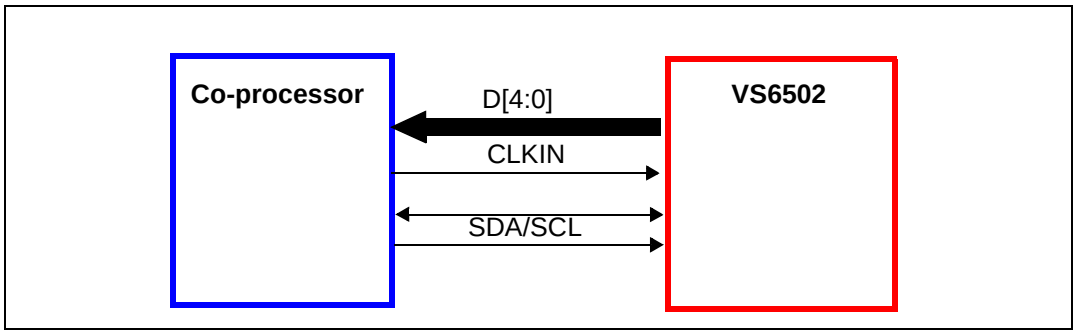


1.2 Typical applications

USB camera with STV0674 or STV0676

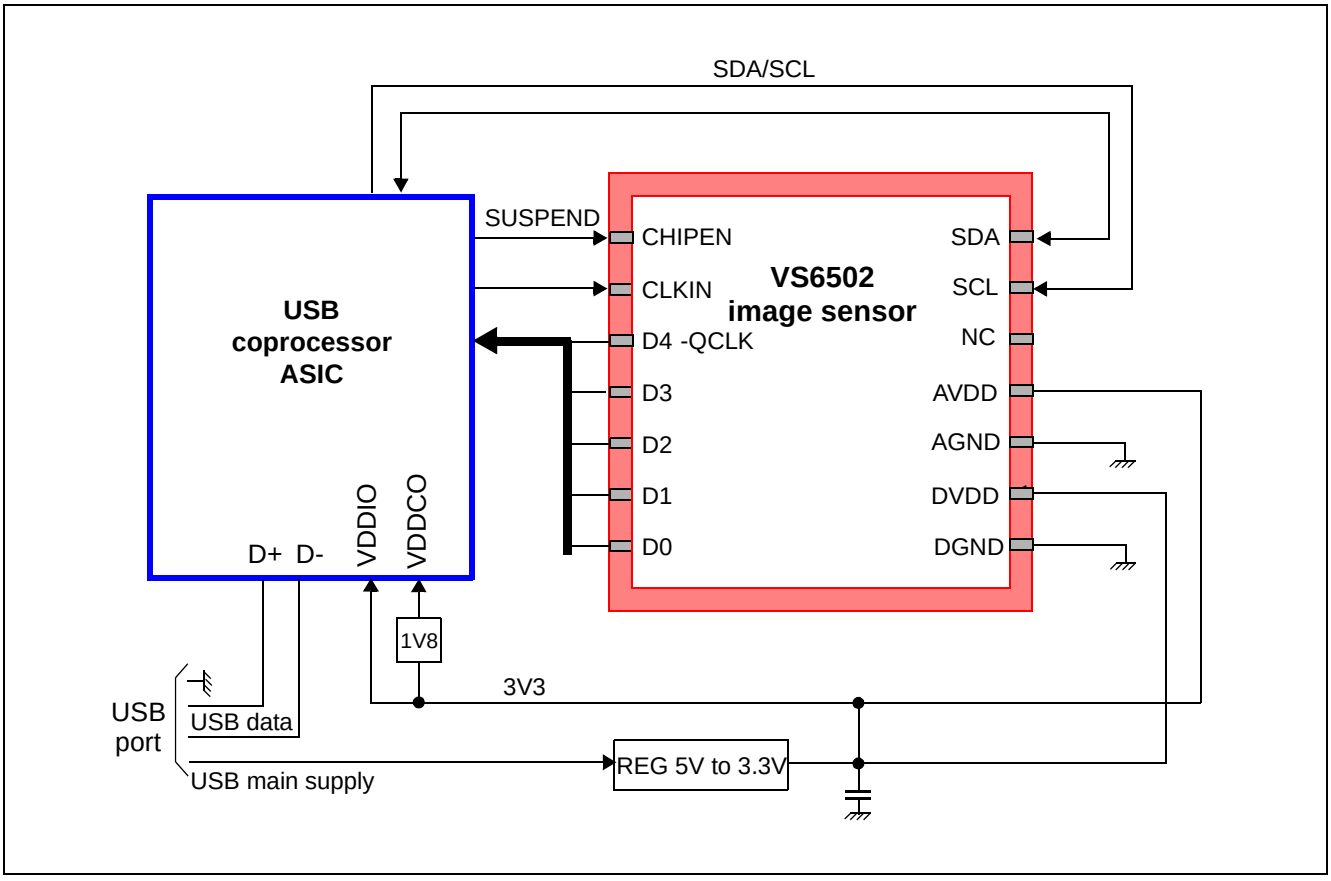
This is a USB video camera where the co-processor supplies the sensor clock CLKIN and uses the embedded control sequences to synchronize with the frame and line level timings.

Figure 2: Overview of USB camera using the VS6502



The USB input supply is 5 V. In the application, a regulator must deliver 3.3 V to both the co-processor and sensor analogue and digital blocks.

Figure 3: USB camera using STV0676/STV0674



1.3 Module Pad Description

1.3.1 Pad assignment

Figure 4: SmOP1.5 - pad assignment

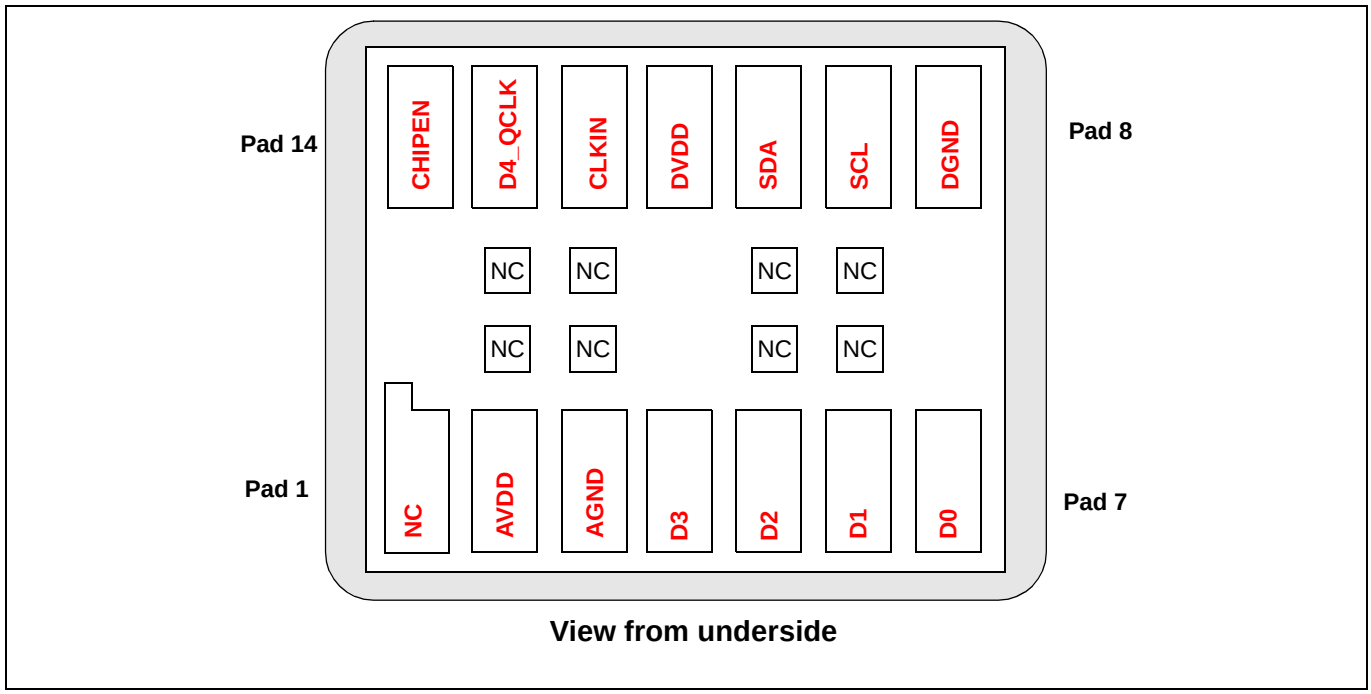


Table 1: Signal description

Pad Number	Pad Name	I/O Type	Description
1	NC	-	Not connected
2	AVDD	PWR	Analogue power supply 3.3V
3	AGND	PWR	Analogue ground
4	D3	O	Data output D3
5	D2	O	Data output D2
6	D1	O	Data output D1
7	D0	O	Data output D0
8	DGND	PWR	Digital Ground
9	SCL	I	I^2C Clock
10	SDA	I/O	I^2C Data
11	DVDD	PWR	Digital power supply 3.3V
12	CLKIN	I	Master clock input
13	D4_QCLK	O	Data output D4 (in 5 -wire mode) Data qualification clock (in 4-wire mode)
14	CHIPEN	I	Chip enable input (LOW = enabled)

2 Functional Description

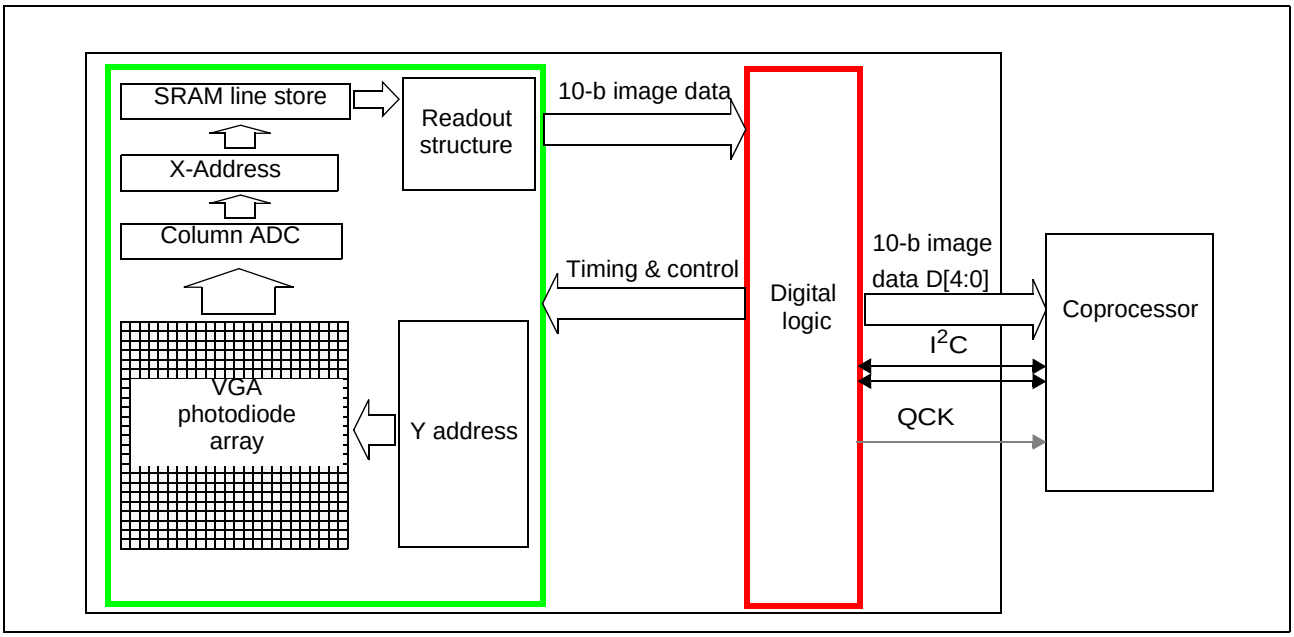
2.1 Video block

2.1.1 Overview

The analogue core of the video block contains a VGA sized pixel array. The integration time and access for a row of pixels is controlled by the Y-address block. The row of pixels being read is converted using a 10-bit in-column ADC. The digitised data is read out into the digital block for formatting. The 10-b data is transferred to the co-processor over a 5-wire digital bus as two 5-b nibbles. An alternative mode allows the transfer of the data as 8 bits per pixel with an additional qualification clock signal (QCK)

The exposure or integration time for the pixel array is calculated by the external co-processor and delivered to the sensor using the I2C interface.

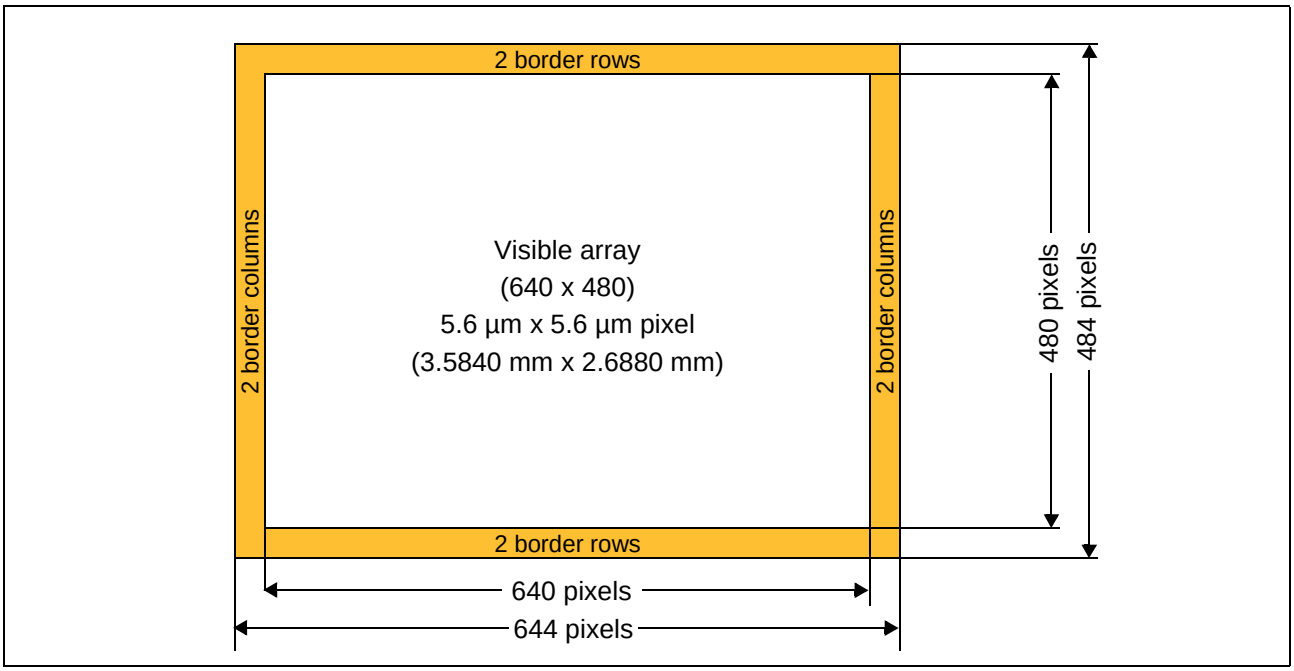
Figure 5: Overview of video block



2.1.2 Imaging array

The physical pixel array is 656 x 496 pixels. The pixel size is 5.6 µm by 5.6 µm. The image size is 644 x 484 pixels in VGA and 324 x 244 pixels in QVGA.

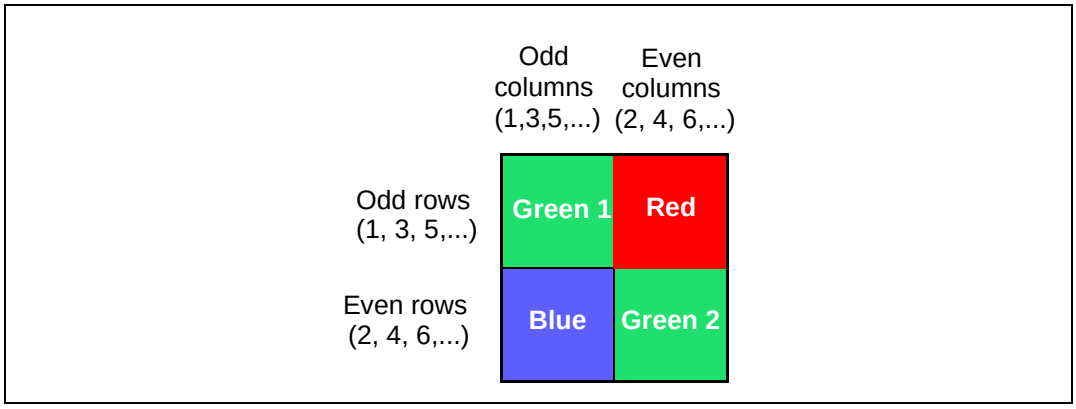
Figure 6: Pixel array interface diagram



2.1.3 Bayer colorization pattern

The image array is covered by a bayer colorization pattern as show in *Figure 7*.

Figure 7: Bayer colorization pattern



2.1.4 Microlenses

The device has microlenses on top of each pixel of the active array area, these micolenses improve the sensor sensitivity by refocusing light towards the sensing area of the pixel.

2.2 Image Formats

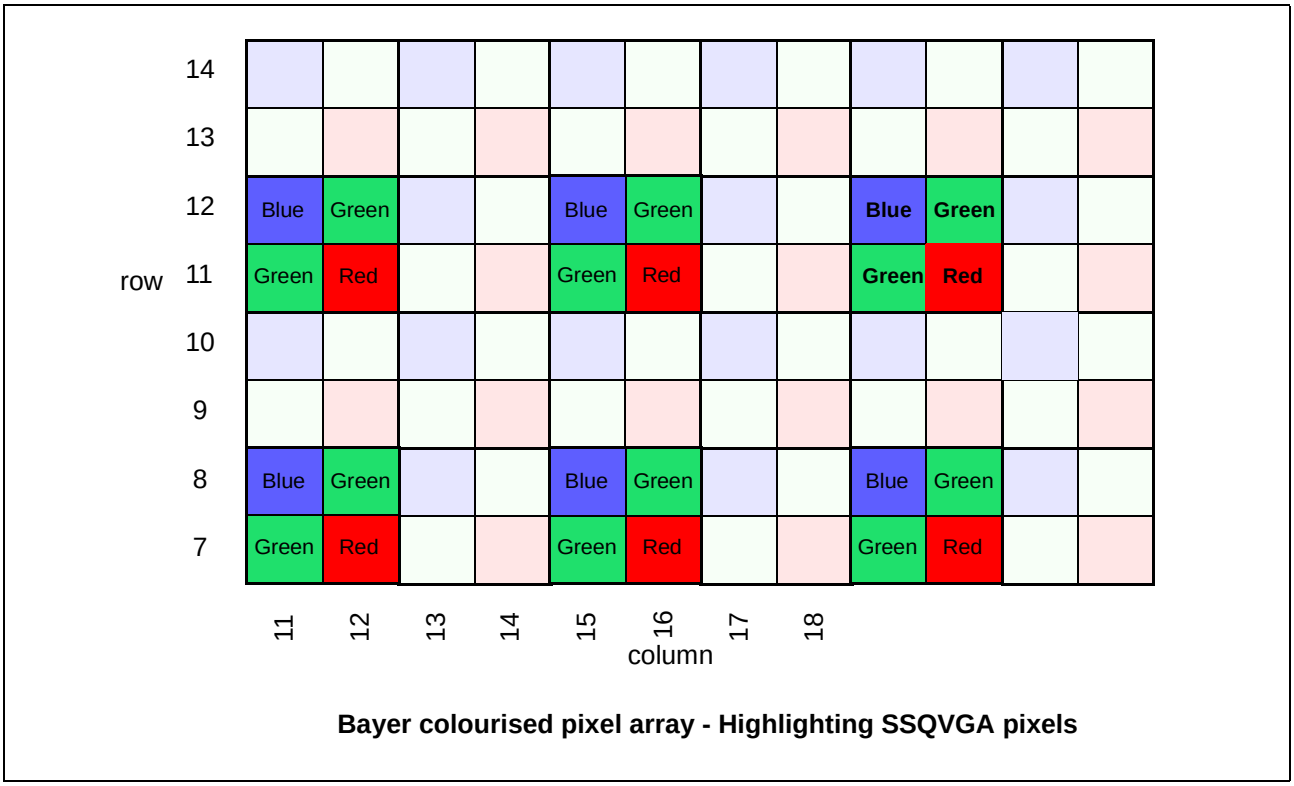
2.2.1 VGA Format

This is the default format and produces an output of 644 pixels by 484 pixels.

2.2.2 Sub-sampled QVGA format

In this mode the QVGA image is generated by sub-sampling the VGA image in groups of 4 to preserve the Bayer pattern with every second group of pixels and lines skipped as illustrated in *Figure 8*. Although the former would not necessarily apply to a monochrome sensor the same address sequence is preserved. Due to the crude nature of the sub-sampling, the resultant output image will be of inferior quality but contains full field of view and is intended as a preview option before switching to view the required scene region in more detail.

Figure 8: Sub-sampled QVGA image format



2.2.3 Window Of Interest QVGA

In WOI mode the QVGA image is generated by cropping the VGA image. I2C registers 87, 88 and 90 allow the user to select the coordinate of the top left corner of the QVGA WOI within the VGA picture (an offsetof (0,0) means top left of the full VGA array). The default frame rate in this modeis twice that of the default VGA mode

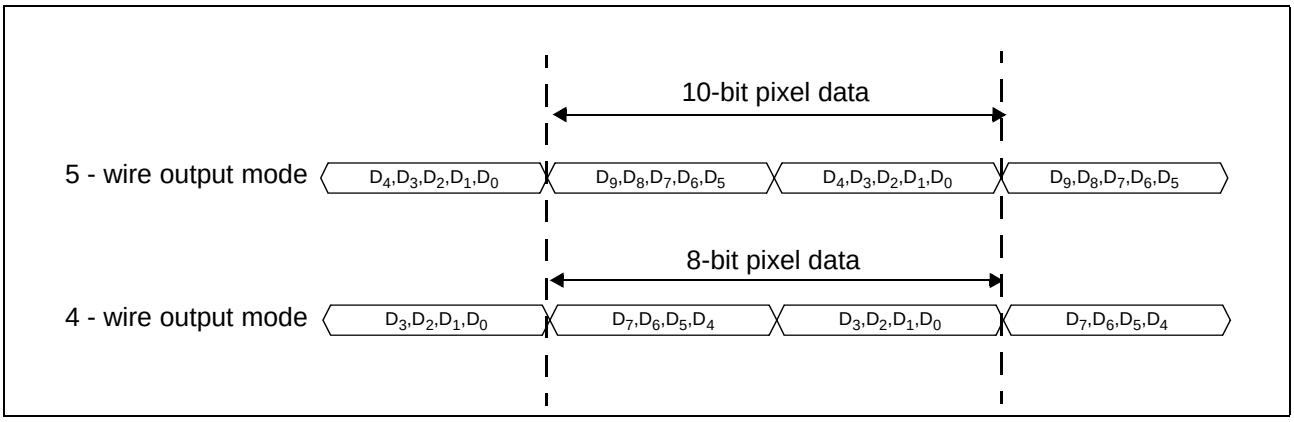
2.3 Data format

The video interface consists of a mono-directional, tri-stateable 5 wire data bus.

There are two data output modes controlled by serial register [23]

- **4- wire mode:** data is 8 bits per pixel, output as two 4-bit nibbles, most significant nibble first. In this mode a data qualification clock is also provided.
- **5-wire mode:** data is 10 bits per pixel, output as two 5-bit nibbles, most significant nibble first. , on 4 wires. In this mode there is NO qualification clock

Figure 9: Digital data output modes



2.3.1 QCLK Control

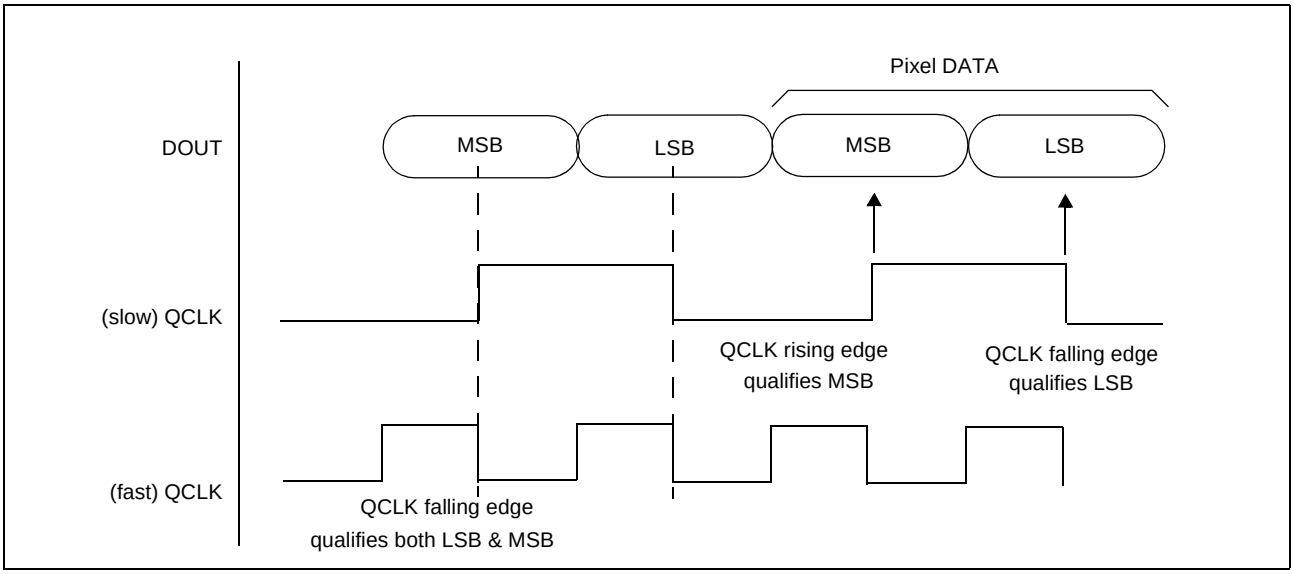
QCLK Type

The QCLK output (only available in 4-wire mode) may be one of two different types, controlled via serial register [20]

- **SLOW:** in this mode the rising edge of QCLK qualifies the MS nibble of each pixel and the falling edge of QCLK qualifies the LS nibble
- **FAST:** in this mode the falling edge of QCLK is used to qualify bith nibbles.

This is illustrated in *Figure 10* below;..

Figure 10: Pixel output timing



Frame-level position of QCLK signal

QCLK can operate in 2 different modes, selectable using register [20]

- **Free running**: in this mode, QCLK is runs continuously
- **Active only**: in this mode QCLK only qualifies the visible lines

2.3.2 Line format

The line format is shown in *Figure 11*. Each line starts with a Start of Active Video (SAV) sequence which consists of an escape sequence (FF-FF-00) followed by a single byte line code that identifies the line type and then two bytes containing the line number (with parity bits).

The line number format is shown in *Figure 12* and the line codes are described in *Section 2.3.3*.

Each line is terminated with an End of Active Video (EAV) sequence consisting of an escape sequence followed by the End of Line (EOL) code followed by the average value of the pixels on that line (repeated).

Following the EAV sequence there is a blanking period where the data is 0xFF. The length of this interline blanking period is shown in *Table 3 on page 12*.

Figure 11: Line format

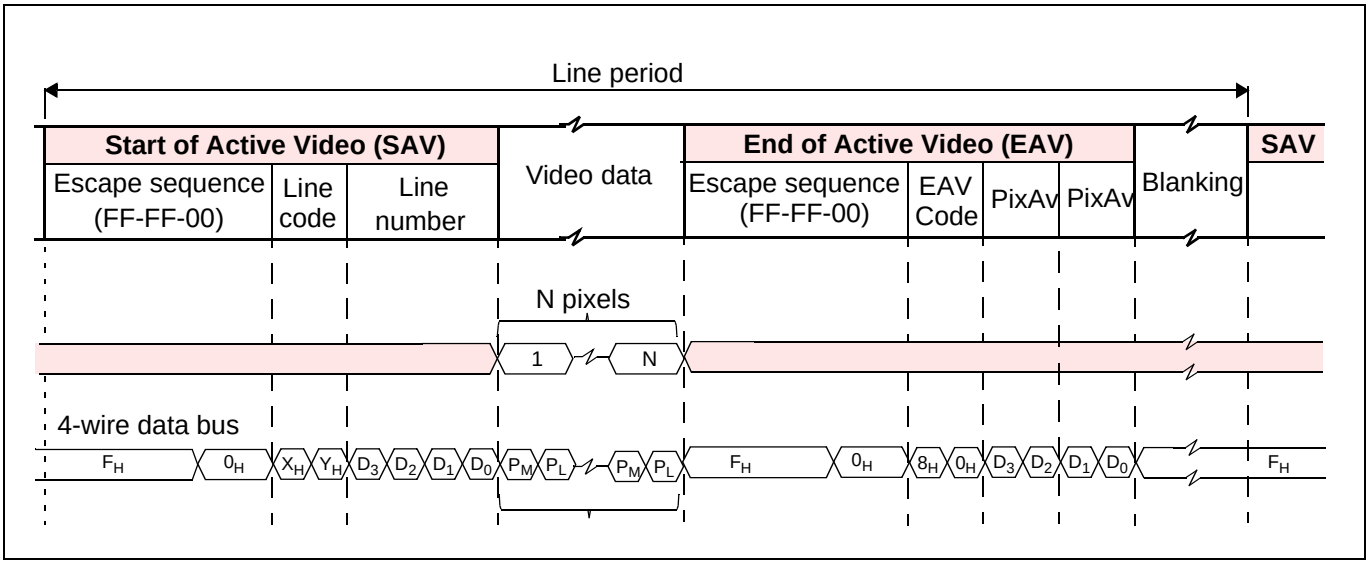
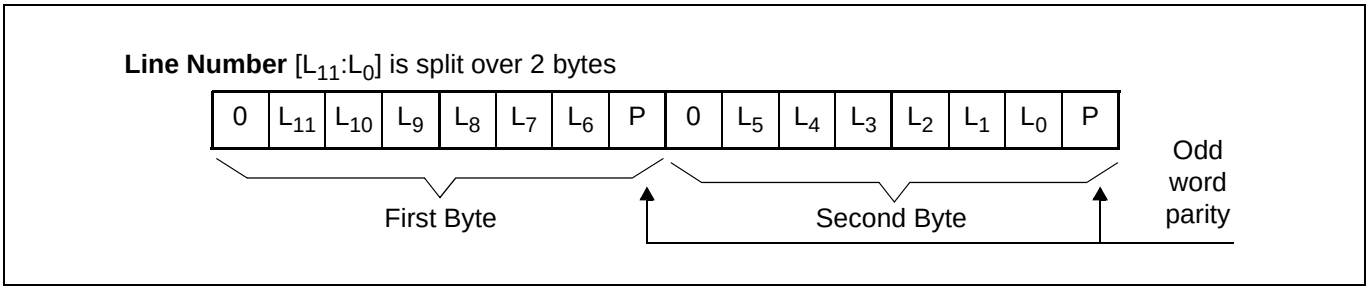


Figure 12: Line Number Data Format



2.3.3 Line Codes

All line codes are 8 bit numbers. When the 502 is in 5-wire mode ie outputting 10-bit pixel data then the codes are shifted left by 2 bits i.e. multiplied by 4.

Table 2: Line Codes

Line Type	Line Code
Start of Frame (SOF)	199 ($C7_H$)
Blank Line (BL)	157 ($9D_H$)
Dark line (DK)	171 (AB_H)
Visible Line (VL)	182 ($B6_H$)
End of Frame (EOF)	218 (DA_H)
End of Line (EOL)	128 (80_H)

2.3.4 Extending line length

The user can extend the line length by writing to serial registers 82 and 83. The line length padding is inserted after the EAV sequence, ensuring that the distance between the SAV and EAV sequences remains constant.

2.3.5 Line Timing

Table 3 lists the image durations and interline intervals in VGA and QVGA

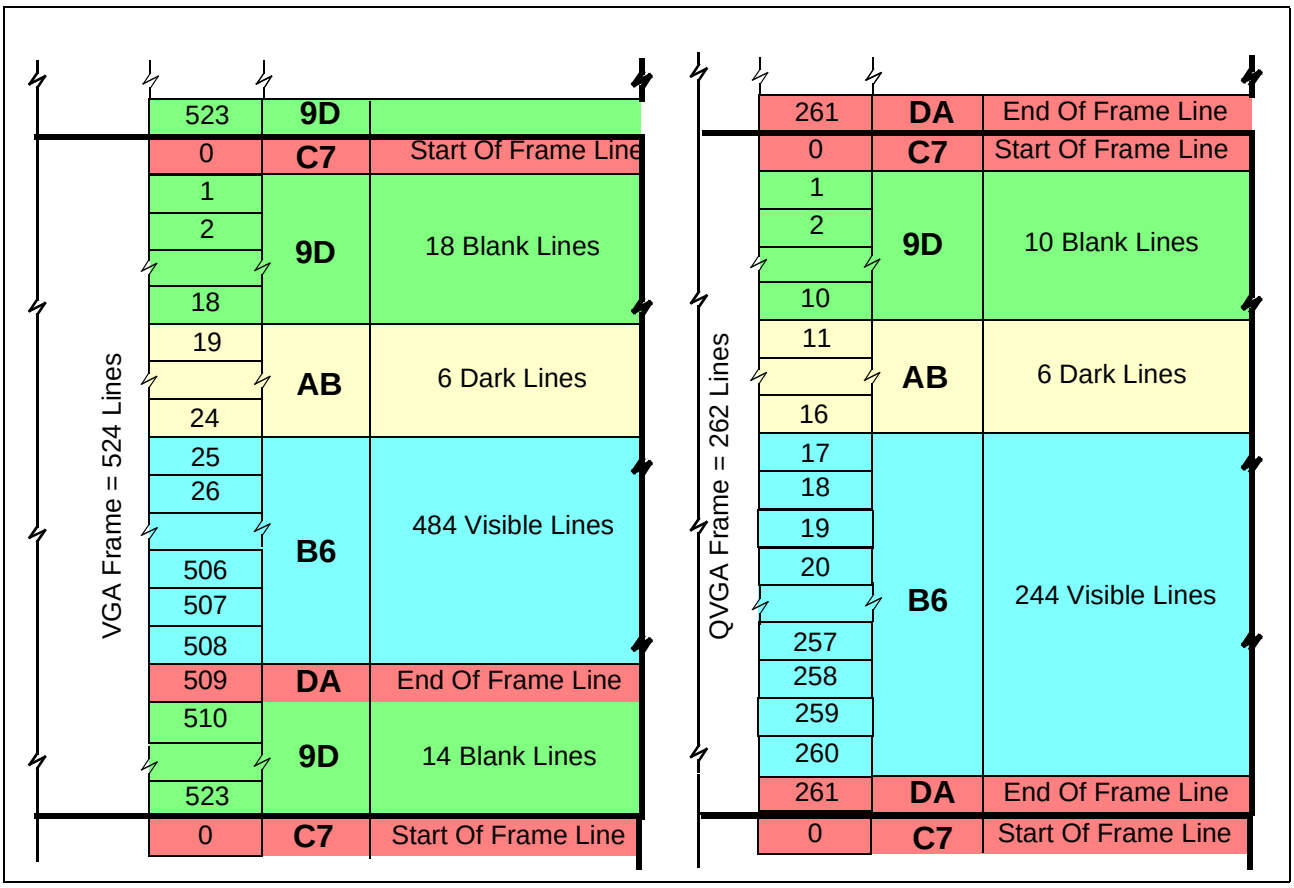
Table 3: Video mode line timing

Mode	QCK (MHz)	Image		Interline		Line total	
		QCKs	µs	QCKs	µs	QCKs	µs
VGA	12	644	53.6	118	9.8	762	63.5
QVGA	6	324	54	57	9.5	381	63.5
QVGA	12	324	27	57	4.75	381	31.75

2.3.6 Frame Format

Each frame is built as a sequence of lines, each line has an embedded line code.

Figure 13: Frame formats in VGA and QVGA modes



2.3.6.1 Start of Frame (SOF) line timing

The start of frame line at the beginning of each video frameframe contains status data. Please contact STMicroelectronics for details.

2.3.6.2 Blank lines

The blank lines contain blank bytes (07_H).

2.3.6.3 Dark lines

The dark line contains the dark calibrated values of the optically shielded lines. The average value is 16 when dark calibration is enabled.

2.3.6.4 End of frame line

The end of frame line at the end of each video frame contains no video data. Its sole purpose is to indicate the end of the active video portion of a frame.

2.3.6.5 Extending frame length

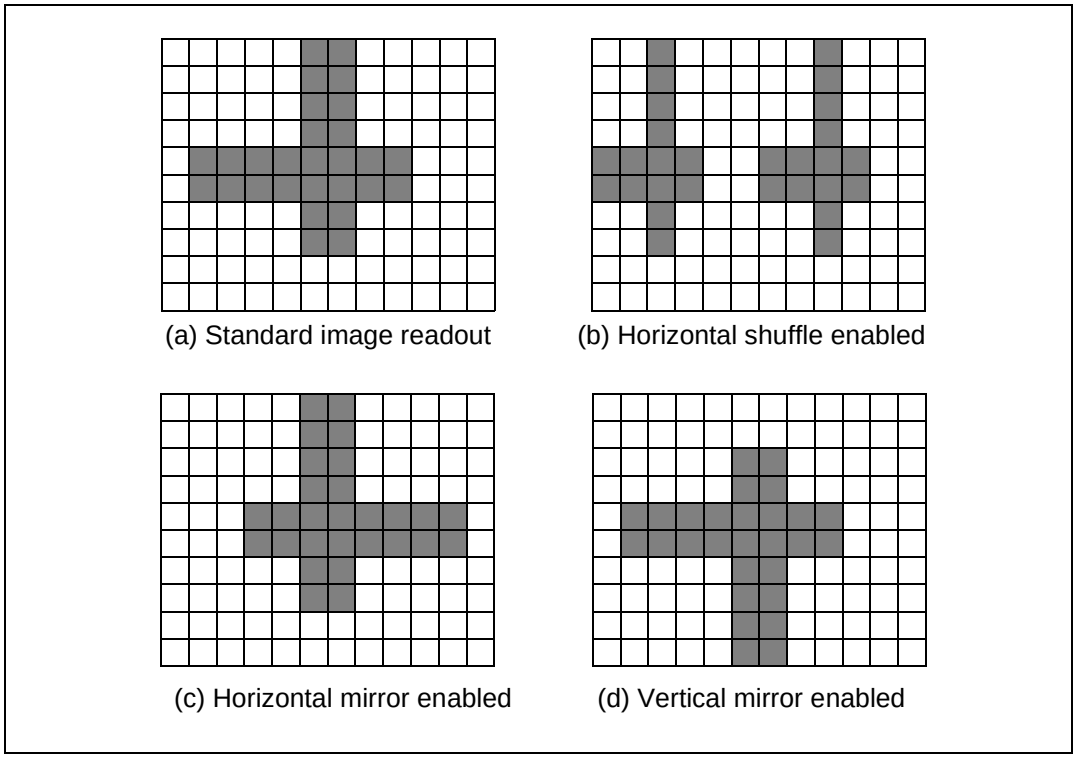
The user can extend the inter-frame period by increasing the frame length. This is achieved by writing to serial registers 97 and 98. In this event, the appropriate number of additional blank lines is inserted between the End Of frame (EOF) line and the Start Of Frame (SOF) line. This means that the distance between SOF and EOF remains constant.

2.3.7 Image translations

The imaging array can be readout with different modes as described here below:

- Shuffle horizontal readout, bit [7] of serial register [17]. Even columns (2,4,6.) are readout first.
- Mirror horizontal readout, bit [3] of serial register [22]. Columns are readout in reverse order.
- Mirror vertical readout, enabled by setting [4] of serial register [22]. Rows are readout in reverse order.

Figure 14: Image readout modes



2.3.8 Dark calibration

The VS6502 has an automatic dark calibration system which is used to set the black level of the output video data to 16. The VS6502 has special ‘dark’ pixel rows which have the same exposure setting as the visible lines but are shielded from incident light. The VS6502 uses these lines to calculate an offset which is then be applied to the video data AND to the dark lines themselves. In this case the mean value of the dark lines output will be 16.

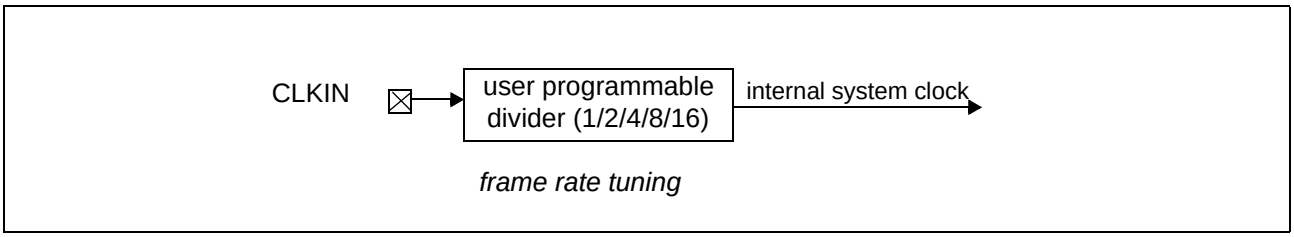
The measured dark line offsets are reported in registers [9] and [10]. By default these offsets are applied to the video data but a user may choose to apply no offset at all or their own offset which may be entered in registers [44] and [45] in 2’s complement format.

The dark calibration function is controlled via register [46].

2.3.9 Clock management and on-chip divider

The VS6502 has a built-in clock divider which acts on the input clock as shown in *Figure 15.* The clock divide ratio is controlled by register 37.

Figure 15: VS6502 clock divider



With the user programmable divider set to its default value of 1 (i.e. no divide), a 24 MHz input clock will generate the frame and pixel rates shown in *Table 4*.

Note: The VS6502 can operate with a maximun external clock frequency of 27 MHz.

Table 4: Default video frame rates

Video Mode	CLKIN (MHz)	Frame rate (Hz)	Pixel rate (MHz)
VGA	24	30	12
SSQVGA	24	60	6
WOIQVGA	24	60	6

For values of clock divider other than 1, the rates shown above can be divided accordingly.

These rates are based on the default line and frame lengths. If the user increases either of these then the frame rate will be reduced.

2.3.10 Exposure/gain control

The sensor does not contain any form of automatic exposure or gain control. To produce a correctly exposed image, exposure and gain values must be calculated externally and written to the sensor via the serial interface. This function is handled by ST co-processors.

Exposure calculation

The exposure time for a pixel and the ADC range (therefore the gain) are programmable via the serial interface. The explanation below assumes that the gain and exposure values are updated together as part of a 5 byte serial interface auto-increment sequence.

Exposure time combines coarse, fine exposure, pixel rate also related to frame and line lengths, all defined in *Table 5*.

Table 5: Definitions related to exposure

Frame length	Number of lines per frame [default=524] The frame length may be increased to 1023 by writing to the frame length register.
Line length	Number of pixels in a line [default = 762] The line length may be increased to 1023 by writing to the line length register.
Exposure	The pixel exposure time is determined by the course and fine exposure values
Coarse exposure value	The number of lines a pixel exposes for. Limited by frame length. Coarse exposure value is in the range [0 - (frame length -2)].
Fine exposure value	Number of additional pixel periods a pixel exposes for. Limited by line length. Fine exposure value is in the range [11 - (line length)].
Pixel period	Determined by the input clock frequency (Fclkin) and user clk_div setting. PixPeriod=(2*N)/Fclkin where N = clock divider ratio
Exposure time	PixPeriod x [($Coarse_{num\_lines}$ x $Line\_Length_{num\_pixels}$) + $Fine_{pixels}$]

Example of exposure calculation in default VGA video mode

coarse exposure = 522

fine exposure = 762

Input clock frequency - Fclkin = 24MHz,

Pixel period = $2/(24 \times 10^6) = 8.33 \times 10^{-8}$ s

Calculation: exposure time = 8.33×10^{-8} x [(522 x 762) +762] = 33.2 ms

The available range of exposure (without using clock division) is shown in *Table 6*.

Table 6: Exposure ranges [24MHz system clock]

Range	Coarse (no. lines)	Line length (no. pixels)	Fine (no. pixels)	Exposure	
				No. pixels	Time
Min.	0	762	11	0	0.92 µs
Max (default-VGA)	522	762	762	400,050	33.2 ms
Max (available)	1023	1023	1023	$1023^2 + 1023$	87.3 ms

2.3.11 Gain timing and exposure updates

Exposure and gain values are re-timed within the sensor to ensure that a new set of values is only applied to the sensor array at the start of each frame. The status register [2] shows is set high when a new exposure value is written via the serial interface but has not yet been applied to the sensor array.

There is a 1 frame latency between a new exposure value being applied to the sensor array and the results of the new exposure value being read-out. The same latency does not exist for the gain value. To ensure that the new exposure and gain values are aligned up correctly the sensor delays the application of the new gain value by one frame relative to the application of the new exposure value.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain settings, if the serial interface communication extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to any location in the exposure page of the serial interface register map. Thus, if the 5 bytes of exposure and gain data is sent as an auto-increment sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

2.4 Device operating modes

The VS6502 sensor has three main operating modes. The current mode of the device is reported in register [29].

2.4.1 Sleep Mode (also referred to as low power)

This is the default state of the sensor on power up. In this mode all analogue circuitry is powered down and there is no video output. All I2C registers are accessible (provided that a system clock is present).

2.4.2 Idle Mode

In this mode the analogue circuitry is powered up and the QCLK output is present. There is no video data output and the FST and LST signals remain low.

2.4.3 Run Mode

In this mode the device is fully operational and produces video output.

2.5 Mode Control

The VS6502 modes are controlled by two I2C registers:

- Register[16] - Setup0
- Register[28] - IDLE mode control

On power up, the VS6502 is in low-power mode and bit 0 of register [16] is set. Clearing this bit via the I2C interface causes the VS6502 to go directly into RUN mode and start producing video data.

Warning:Entering RUN mode directly from SLEEP does not give the analogue circuitry in the sensor enough time to stabilise before video data is produced. The first few frames of video data will not appear to be correctly exposed. For streaming video applications this may be perfectly acceptable but this could cause problems for systems which wish to capture and use the first video frame output from the sensor.

In order to guarantee a valid first video frame it is necessary to enter IDLE mode to allow the analogue circuitry to be powered on. The sensor must remain in IDLE mode for at least 10 ms.

IDLE mode may be entered from SLEEP mode as follows:

- set bits 0 and 1 of register[28]
- clear bit 0 of register[16]

The transition from IDLE to RUN is now controlled by bit 1 of register[28].

The first video frame will appear (along with the first FST pulse) one exposure time after the sensor goes into RUN mode.

Note: The default value of exposure is maximum (ie 1/30th second) but may be changed as required.

2.5.1 Standby mode (CHIPEN high)

Standby mode is entered asynchronously by driving the CHIPEN pin high. In this mode the analogue blocks of the sensor are powered down and the video timing logic is reset with all data lines driven high.The external sensor clock is gated and no I2C communication is possible. To achieve absolute minimum power consumption, the external clock should be switched off. During standby mode the register contents are preserved.

2.5.2 Sensor reset via the serial interface

It is possible to completely reset the VS6502 via the serial interface by setting bit 1 of the SETUP0 register. This will reset all the VS6502 registers.

3 Serial Control Bus

3.1 General description

The 2-wire I2C serial interface bus is used to read and write the sensor control registers.

Some status registers are read-only.

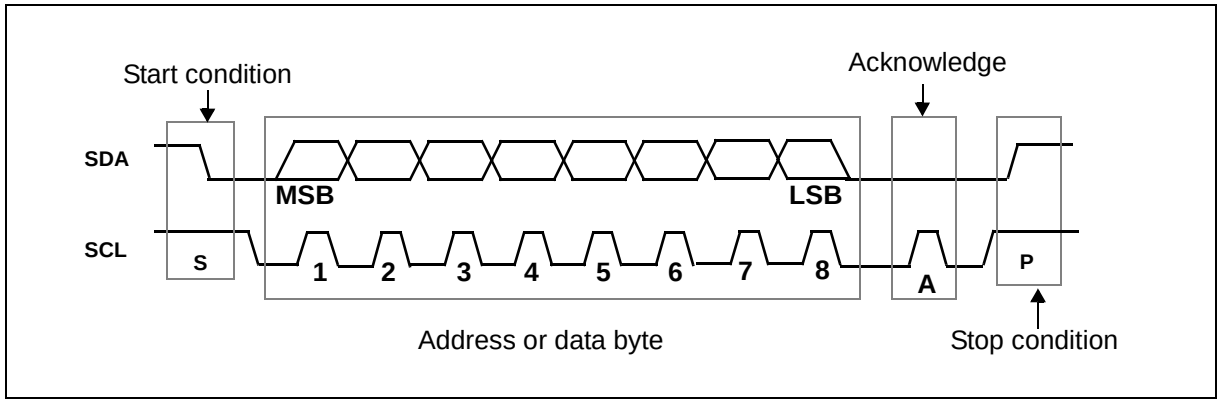
The main features of the serial interface include:

- Variable length read/write messages
- Indexed addressing of information source or destination within the sensor
- Automatic update of the index after a read or write message
- Message abort with negative acknowledge from the master
- Byte oriented messages

3.2 Serial communication protocol

The co-processor must perform the role of communication ‘master’ and the sensor acts as a ‘slave’. The communication from host to sensor takes the form of 8-bit data with a maximum serial clock frequency of 100 kHz. Since the serial clock is generated by the bus master it determines the data transfer rate. Data transfer protocol on the bus is illustrated in *Figure 16*.

Figure 16: Serial Interface data transfer protocol



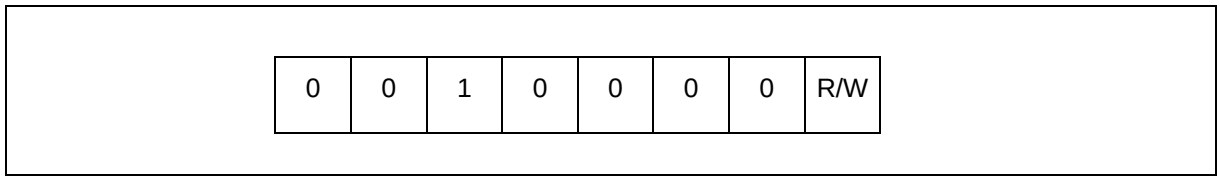
3.2.1 Data format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is produced by sampling *sda* at a rising edge of *scl*. The external data must be stable during the high period of *scl*. Exceptions to this are *start* (S) or *stop* (P) conditions when *sda* falls or rises respectively, while *scl* is high.

A message contains at least two bytes preceded by a *start* condition and followed by either a *stop* or *repeated start, (Sr)* followed by another message.

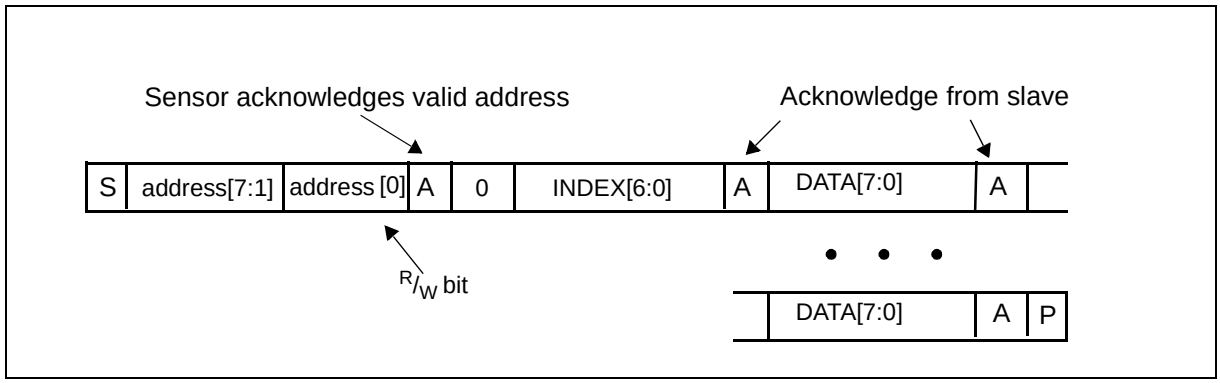
The first byte contains the device address byte which includes the data direction *read,* (r)*, ~write*, (~w), bit.

Figure 17: VS502 Serial interface address



The byte following the address byte contains the address of the first data byte (also referred to as the *index*). The serial interface can address up to 128 byte registers.

Figure 18: Serial interface data format



3.2.2 Message interpretation

All serial interface communications with the sensor must begin with a *start* condition. If the *start* condition is followed by a valid address byte then further communications can take place. The sensor will acknowledge the receipt of a valid address by driving the *sda* wire low. The state of the *read/~write* bit (LSB of the address byte) is stored and the next byte of data, sampled from *sda,* can be interpreted.

During a write sequence the second byte sent to the sensor is an index and is used to point to one of the internal registers.

The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a *stop* condition or sends a *repeated start (Sr)*.

As data is received by the slave, it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the current index is read out in the byte following the device address byte. The next byte read from the slave device includes the contents of the register addressed by the current index. The contents of this register are then parallel loaded into the serial/parallel register and clocked out of the device by *scl.*

At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. Although VS6502 is always considered to be a slave device, it acts as a transmitter when the bus master requests a read from the sensor.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

3.3 Types of messages

This section gives guidelines on the basic operations to read data from and write data to the serial interface.

The serial interface supports variable length messages. A message may contain no data bytes, one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available is detailed below.

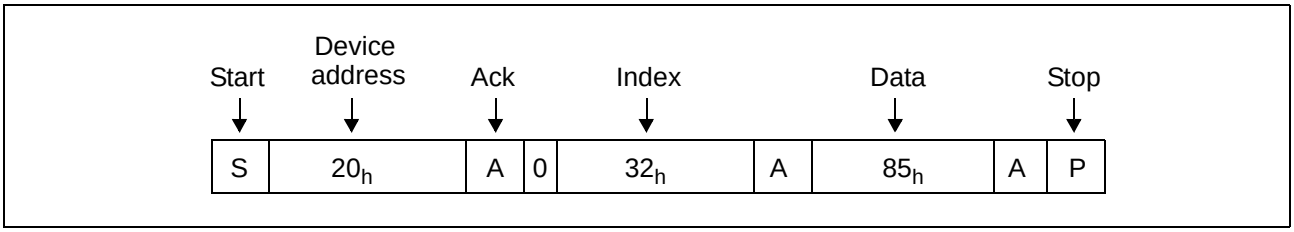
- No data writes are used to set the index for a subsequent read message.
- Multiple location writes may be used for fast information transfers.

Examples of these operations are given below. A full description of the internal registers is given in *Chapter 4*. For all examples, the slave address used is 0x20 for writing and 0x21 for reading. The write address includes the read/write bit (the LSB) set to zero while this bit is set in the read address.

3.3.1 Single location, single data write

When a single value is written to the sensor, the message looks as shown in *Figure 19*.

Figure 19: Single location, single write

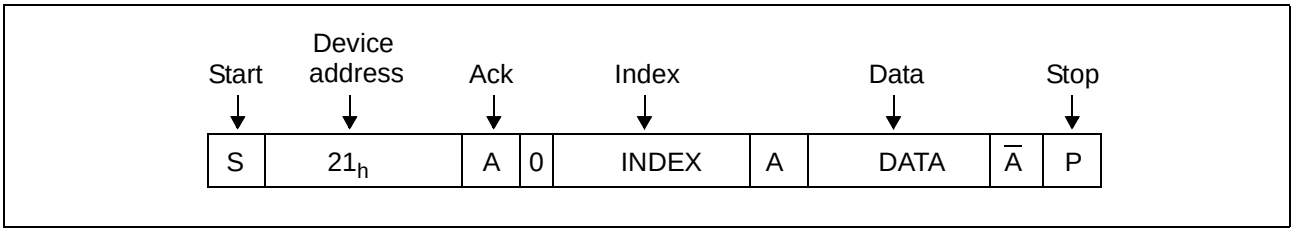


In this example, the register with index = 32 is set to 85. The index value is preserved in the sensor and may be used by a subsequent read. The write message is terminated with a stop condition from the master.

3.3.2 Single location, single data read

During a read sequence the sensor always sends the index used to get the first byte of data before sending the data itself. The index can only be set by a write message.

Figure 20: Single location, single read

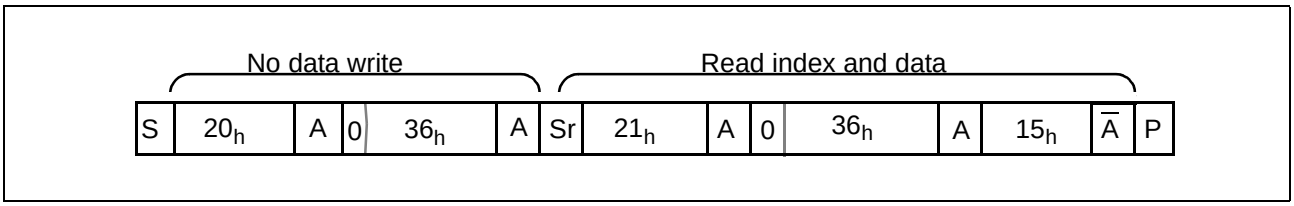


3.3.3 No data write followed by same location read

When a location is to be read and the value of the stored index is not known, a write message with no data byte must be written first in order to set the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master, a repeated start

condition is asserted between the write and read messages.
In this example, the *gain* value (index = 36_{10}) is read as 15_{10} (see *Figure 21*).

Figure 21: No data write followed by same location read

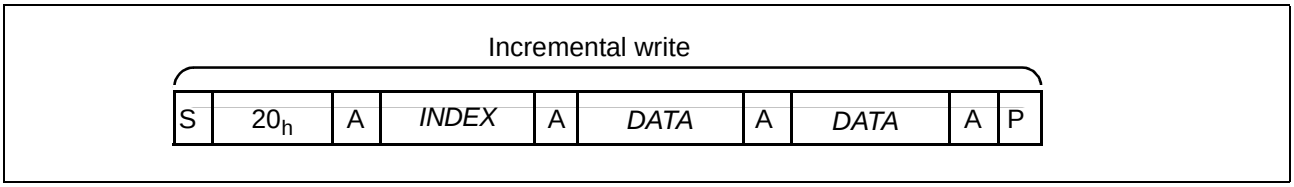


As in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

3.3.4 Multiple location write

It is possible to write data bytes to consecutive internal registers without having to send explicit indexes prior to sending each data byte. After sending the first data byte, the master sends an acknowledge followed by the next byte and so on as shown in *Figure 22*.

Figure 22: Multiple location write

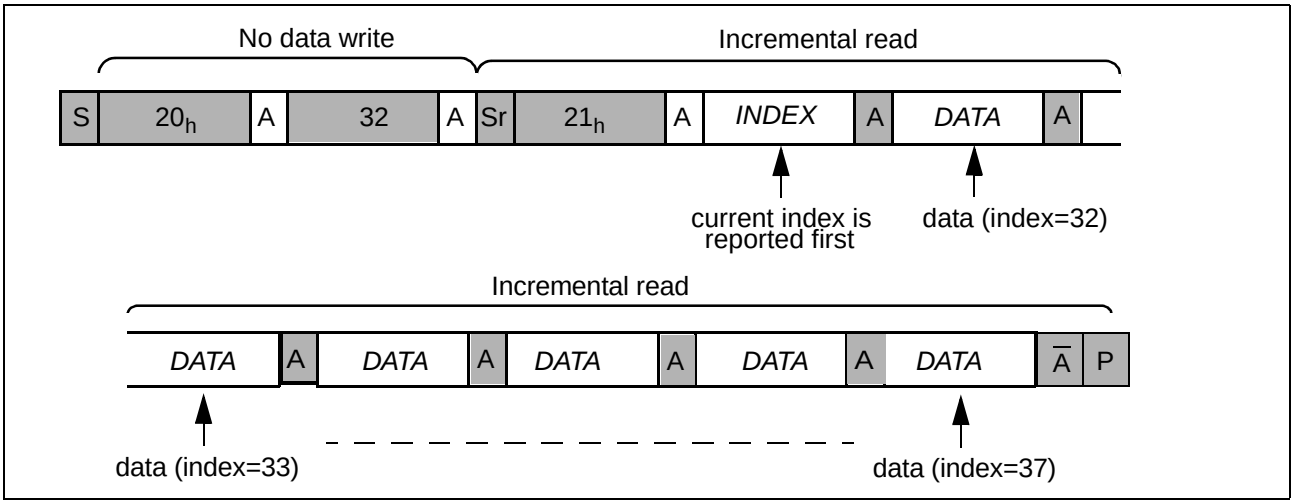


3.3.5 Multiple location read

In the same manner as writing, multiple locations can be read with a single read message. In this example a no data write is performed first in order to set the required index and then six consecutive indexes are read. After each data byte is received the master issues an acknowledge (ACK).

After the last required byte is received, the master issues a negative acknowledge (NACK) followed by a stop condition to terminate the transaction.

Figure 23: Multiple location read



4 I²C Register Description

4.1 Register summary

The 8-bit registers within the sensor are accessible via the serial interface. Registers are grouped according to their function. The primary register groups for the VS6502 are:

- Status registers
- Setup registers with bit significant functions
- Exposure register for parameters that influence the output image brightness
- Format registers

Some registers are Read Only (RO), all others are readable and writable (R/W).

Table 7: Serial interface address map

Index	Name	Length	Type	Comments
Status registers				
0	deviceH	8	RO	Chip identification number including revision indicator (502 Rev0).
1	deviceL	8	RO	
2	status0	8	RO	User can determine whether timed serial interface data has been consumed by interrogating flag states
9	dark_avgH	4	RO	This is the average pixel value returned from the dark line offset cancellation algorithm (2's complement notation)
10	dark_avgL	8	RO	
14	frame counter	8	RO	Current frame number (0 to 255)
Setup registers				
16	setup0	8	R/W	Low-power & video timing
17	Shuffle	8	R/W	Shuffle
20	fg_modes	8	R/W	Frame grabbing modes (FST and QCK)
22	shuffle/mirror	8	R/W	Read-out order of data
23	op_format	7	R/W	Output coding formats
28	IDLE mode control	2	R/W	IDLE mode control register
29	Mode State	3	RO	Reports current mode
Exposure registers				
32	fineH	2	R/W	Fine exposure
33	fineL	8	R/W	
34	coarseH	2	R/W	Coarse exposure
35	coarseL	8	R/W	
36	analogue gain	4	R/W	Analogue gain setting

Table 7: Serial interface address map

Index	Name	Length	Type	Comments
37	clk_div	4	R/W	Clock division
44	dark offsetH	3	R/W	Dark line offset cancellation value (2's complement notation)
45	dark offsetL	8	R/W	
46	dark offset setup	3	R/W	Dark line offset cancellation enable
Video format registers - [82-98]				
82	line_lengthH	2	R/W	Line Length (pixel clocks)
83	line_lengthL	8	R/W	
87	x-offsetH	1	R/W	WOI X offset
88	x-offsetL	8	R/W	
90	y-offsetL	8	R/W	WOI Y offset
97	frame_lengthH	2	R/W	Frame length (Lines)
98	frame_lengthL	8	R/W	

4.2 Status registers

4.2.1 [0-1] - DeviceH and DeviceL

These registers provide read only information to identify the sensor type that has been coded as a 12-bit number and a 4-bit mask set revision identifier. The device identification number for VS6502 is 502 (0001 1111 0110_2). The initial mask revision identifier is 0 (0000_2).

Table 8: [0] - DeviceH

Bits	Function	Value	Comment
[7:0]	Device type identifier	1F	Most significant 8 bits of the 12 bit code identifying the chip type.

Table 9: [1] - DeviceL

Bits	Function	Value	Comment
[7:4]	Device type identifier	6	Least significant 4 bits of the 12 bit code identifying the chip type.
[3:0]	Mask set revision identifier	1	

4.2.2 [2] - Status0

Table 10: [2] - Status0

Bits	Function	Default	Comment
[7]	Video timing parameter update pending flag	0	Video timing parameters sent but not yet consumed by sensor
[4]	Odd/even frame	1	The flag will toggle state on alternate frames
[3]	Clock division update pending	0	Clock divisor sent but not yet consumed by the sensor
[2]	Gain value update pending	0	Gain value sent but not yet consumed by the sensor
[1]	Coarse exposure value update pending	0	Coarse exposure value sent but not yet consumed by the sensor
[0]	Fine exposure value update pending	0	Fine exposure value sent but not yet consumed by the sensor

4.2.3 [9-10] - Dark Average

Table 11: [9-10] - Dark_Avg

Regiter index	Bits	Function	Default	Comment
9	[2:0]	Dark average ms bits	-	The calculated pixel average over a series of dark lines. The pixel sample size from each dark line will be image size dependent up to a maximum of 256
10	[7:0]	Dark average lsb	-	

4.2.4 [14] - Frame Counter

Table 12: [14] - Frame Counter

Regiter index	Bits	Function	Default	Comment
14	[7:0]	Frame count	0	Increments by 1 each frame

4.3 Setup registers

4.3.1 [16] - Setup0

Table 13: [2] - Setup0 [16]

Bits	Function	Default	Comment
[7:5]	Video Timing Mode Select	001	See *Table 14*
[2]	Soft Reset	0	Setting this bit resets the sensor to its power-up defaults. This bit is also reset. 1: apply soft-reset
[0]	Low-Power	1	0: device is active 1: device is in low-power mode

Table 14: Video Timing modes

setup0 [7:5]	Video Data	Line Length	Frame Length	Comment
001	644 x 484	762	524	VGA (default)
100	324 x 244	381	262	WOI QVGA
110	324 x 244	381	262	SSQVGA

4.3.2 [17] - Shuffle

Table 15: [17] - shuffle

Bits	Function	Default	Comment
[7]	Pixel read-out order	1	1 = shuffled readout order 0 = normal readout order

4.3.3 [20] - fg_modes

Table 16: [20] - fg_modes

Bits	Function	Default	Comment
[3:2]	QCK mode	00	00 = no QCLK 01 = free running 10 = only during visible lines
0	QCK type	0	0 = slow 1 = fast

4.3.4 [22] - shuffle/mirror

Table 17: [22] - shuffle/mirror

Bits	Function	Default	Comment
[4]	Line read-out order (vmirror)	0	
[3]	Pixel read-out order (hmirror)	0	

4.3.5 [23] - op_format

Table 18: [23] - op_format

Bits	Function	Default	Comment
[5]	Output tristate control	0	0 = outputs active 1 = outputs tristate
[2]	Embedded code control	0	0 = embedded codes present. 1 = no embedded codes
[0]	Data format select	0	0 = 5 wire mode (10 bits per pixel) 1 = 4-wire mode (8 bits per pixel)

4.3.6 [28] - Idle Mode Control

Table 19: [28] - IDLE mode control

Bits	Function	Default	Comment
[1]	IDLE mode control	0	0 = IDLE Off 1 = select IDLE mode ONLY WORKS IF BIT[0] = 1
[0]	IDLE mode enable	0	0 = No IDLE Mode 1 = IDLE mode enabled

4.3.7 [29] - Mode State

Table 20: [29] - Mode State

Bits	Function	Default	Comment
[2:0]	State	001	000: Suspend 001: Low-Power 010: Parallel reset 011: IDLE 100: Running 101: Wait Frame 110: Set Flags

4.4 Exposure Control Registers

A set of programmable registers controls the sensitivity of the sensor. The registers are as follows:

- Fine exposure
- Coarse exposure time
- Analogue gain
- Clock division

The gain parameter does not affect the integration period rather it amplifies the video signal at the output stage of the sensor core.

Note: The external exposure (coarse, fine, clock division or gain) values do not take effect immediately. Data from the serial interface is read by the exposure algorithm at the start of a video frame. If the user reads an exposure value via the serial interface then the value reported is the data as yet unconsumed by the exposure algorithm, because the serial interface logic locally stores all the data written to the sensor.

Between writing the exposure data and the point at which the data is consumed by the exposure logic, bit 0 of the status register is set. The gain value is updated a frame later than the coarse, fine and clock division parameters, since the gain is applied directly at the video output stage and does not require the long set up time of the coarse and fine exposure and the clock division.

The range of some parameter values is limited and any value programmed out of this range will be clipped to the maximum allowed.

4.4.1 [32-33] - Fine Exposure

Table 21: [32]-[33] - Fine Exposure

Bits	Function	Default	Comment
32 [1:0]	Fine Exposure [9:8]	00	
33 [7:0]	Fine Exposure [7:0]	00000000	

4.4.2 [34-35] - Coarse Exposure

Table 22: [34] - [35]- Coarse Exposure

Bits	Function	Default	Comment
34 [1:0]	Coarse Exposure [9:8]		Default value is maximum for mode VGA = 522
35 [7:0]	Coarse Exposure [7:0]		

4.4.3 [36] - Analogue gain

Table 23: [36] - Analogue gain

Bits	Function	Default	Comment
[3:0]	GAIN [3:0]	0000	0000 = 1.0, Min. Gain = (0dB) 0001 = 1.06 0010 = 1.14 0011 = 1.23 0100 = 1.33 0101 = 1.45 0110 = 1.60 0111 = 1.78 1000 = 2.0 1001 = 2.29 1010 = 2.67 1011 = 3.2 1100 = 4.0 1101 = 5.33 1110 = 8.0 1111 = 16, Max Gain = (24dB)

4.4.4 [37] - Clock Divider

Table 24: [37] - Clock divider settings

Bits	Function	Default	Comment
[3:0]	Clock divider setting	0000	0000 = No divide (default) 0001 = Divide by 2 001x = Divide by 4 010x = Divide by 6 011x = Divide by 8 100x = Divide by 10 101x = Divide by 12 110x = Divide by 14 111x = Divide by 16

4.4.5 [44 -45] - Dark Line Pixel Offset

Table 25: [44 -45] - Pixel offset

Index	Bits	Function	Default	Comment
44	[2:0]	MS Dark line pixel offset	000	This register contains an offset that can be applied to the digitized pixels in the digital output coding block. The offset is a 2's complement number, giving an offset range -1024,+1023.
45	[7:0]	LS Dark line pixel offset	0000_0000	

4.4.6 [46] Dark Line Offset Cancellation Setup Register

Table 26: Dark line offset cancellation setup register

Bits	Function	Default	Comment
[0]	Apply Dark Offset	1	0 = Do not apply offset 1= Apply offset
[1]	Offset source	0	0 = Internally calculated offset (value reported in [9] and [10] 1 = External offset from registers [44] and [45]

4.5 Video format registers

The following registers control the line & frame lengths of video output and the position of the QVGA output window when window of interest mode is selected.

The length of a line is specified in a number of pixel clocks, whereas the length of a frame is specified in a number of lines.The range of some parameter values is limited and any value programmed outside this range will be clipped.

Table 27: Video timing registers

Index	Bits	Function	Default	Comments
82	[1:0]	Line Length MSB value	761	Specified in number of clocks Maximum = 1023 Must program desired line length minus 1
83	[7:0]	Line Length LSB value		
87	0	X-offset MSB value	160	Sets X co-ordinate of top left corner of QVGA window of interest Range 0 to 320
88	[7:0]	X-offset LSB value		
90	[7:0]	Y-offset LSB value	120	Sets Y co-ordinate of top left corner of QVGA window of interest Range 0 to 240
97	[1:0]	Frame Length MSB value	523	Specified in number of lines Maximum = 1023 Must program desired frame length minus 1
98	[7:0]	Frame Length LSB value		

5 Electrical Characteristics

5.1 Absolute maximum ratings

Table 28: Absolute maximum ratings

Symbol	Parameter	Max.	Unit
V_{DD}	Digital power supply	-0.5 to 6.0	V
V_{CC}	Analogue power supply	-0.5 to 3.6	V
I_{DD}	Digital input current	20	mA
T_{STO}	Storage temperature[a]	-25 to + 85	^{o}C
T_{LEAD}	Lead temperature (10 s) JDEC moisture level 3	225	°C

a. A temperature below 0°C can induce a slight humidity penetration into the package cavity. This humidity is easily removable by a short storage in standard climatic conditions (25°C/50% relative humidity).

Caution: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Operating conditions

Table 29: Operating conditions

Symbol	Parameter	Max.	Unit
V_{DD}, V_{CC}	Power supply	3.6	V
$I_{VDD±VCC}$	Current consumption in normal mode (VGA 30 fps)	30	mA
I_{STDBY}	Current consumption in standby mode	10	µA
T_A	Ambient temperature	-25 to +70	°C

5.3 Thermal data

Table 30: Thermal data

Symbol	Parameter	Value	Unit
Rth(j-a)	Junction/ambient thermal resistance	45	°C/W

5.4 DC electrical characteristics

Over operating conditions unless otherwise specified.

5.4.1 Power supply

Table 31: Power supply characteristics

Symbol	Parameter description	Min.	Typ.	Max.	Unit
V_{DD}	Digital power supply range of operation	2.6		3.6	V
V_{CC}	Analogue power supply range of operation	2.6		3.6	V
$I_{VDD±VCC}$	Normal mode sensor current consumption (VGA 30 frame/s)		20	30	mA
I_{STBY}	Current consumption in standby mode (CHIPEN pin high) and DVDD disabled		65	140	µA

5.4.2 Digital block

Table 32: Digital block electrical characteristics

Symbol	Parameter description	Min.	Typ.	Max.	Unit
CMOS digital inputs					
V_{IL}	Low level input voltage			0.8	V
V_{IH}	High level input voltage	2			V
I_{IL}	Low level input current			-1	µA
I_{IH}	High level input current			1	µA
CMOS digital outputs					
V_{OL}	Low level output voltage			0.2	V
V_{OH}	High level output voltage	2.8			V
Serial interface					
F_{SIF}	Operating frequency range	0		100	kHz

5.5 AC electrical characteristics

Table 33: Serial interface timing

Symbol	Parameter	Max.	Unit
f_{SCL}	SCL clock frequency	100	kHz

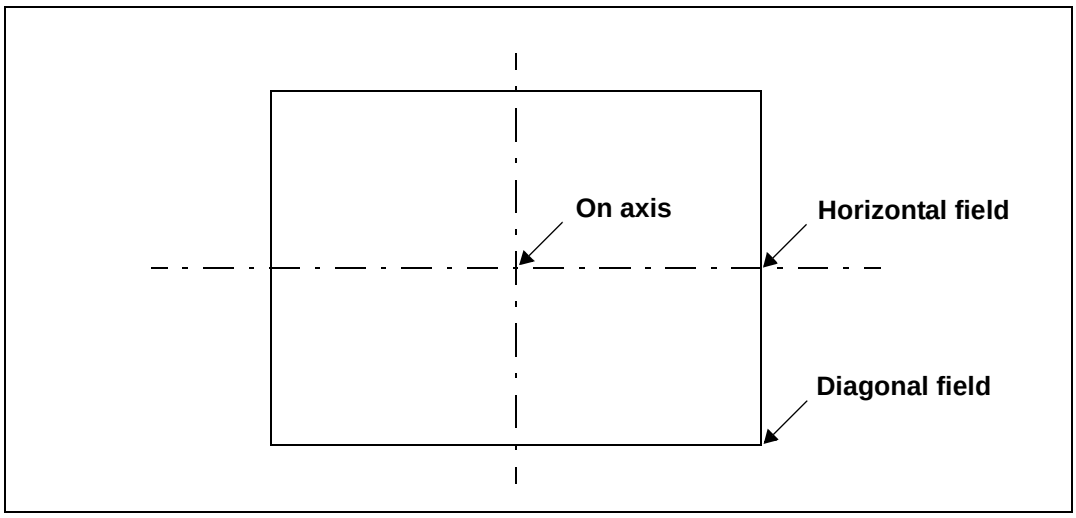
5.6 Optical specifications

Table 34: Optical specifications

Effective Focal Length	4 mm +-0.2 mm
Aperture	F2.8 aperture
Horizontal Field of View	$47^o \pm 2^o$
TV Distortion	TV distortion <2%
MTF[a] @ 60 cm @ 45 cycle/mm	On axis: 55 %
	Horizontal field: 38%
	Diagonal field: 35%

a. see *Figure 24* below

Figure 24: MTF points on the image field



6 Optical Characteristics

The average sensitivity is a measure of the image sensor response to a given light stimulus. The optical stimulus is a white light source with a color temperature of 3200K, producing uniform illumination at the surface of the sensor package. For a color sensor, an IR blocking filter, CM500, is added to the light source. The analog gain of the sensor is set to x1. The exposure time, Δ**t**, is set as 50% of maximum. The illuminance, **I**, is adjusted so the average sensor output code, **Xlight**, is roughly mid-range equivalent to a saturation level of 50%. Once Xlight has been recorded the experiment is repeated with no illumination to give a value **Xdark.**

The sensitivity is then calculated as $\frac{\mathrm{Xlight} - \mathrm{Xdark}}{\Delta t \cdot I}$. The result is expressed in volts per lux-second.

Dark signal

The dark signal is a measure of the effect of pixel leakage current on the sensor output. The measurement is performed without illumination. As the dark signal is small the analogue gain, **G**, of the sensor is increased to x4. For the same reason the clock divisor is set to16. As the leakage is highly temperature dependent, measurement is done at a controlled temperature of 25^{o}C. The mean sensor output is then recorded at 2 exposure settings: **Xdark** at the maximum exposure time; **Xblack** at zero exposure.

The dark signal is calculated as $\frac{\mathrm{Xdark} - \mathrm{Xblack}}{\Delta t \cdot G}$ and is expressed in volts per second.

Temporal noise of pixel and readout

A measure of the temporal noise is required to quantify the noise floor. As the signal is small the gain, **G**, is set to the maximum of x16. In order to remove fixed pattern noise sources it is calculated as the standard deviation, $\sigma_{\mathbf{black}}$, of the difference of a pair of zero exposure and zero illumination images. Random noise is expressed in mV.

Dynamic range

The dynamic range is the measure of the maximum and minimum signal levels at which the sensor can be used.

The figure for temporal noise is used to find the dynamic range as follows $20 \cdot \log\left(\frac{G \cdot Vsat}{\sigma black}\right)$.

Sensor SNR

The SNR measurement given here is based on the temporal noise. The SNR is calculated as the pixel saturation voltage divided by the temporal noise at that saturation level. The optical setup is the same as for the measurement of average sensitivity. The sensor gain, **G**, is set to x1.

The SNR figure is then calculated as: $20 \cdot \log\left(\frac{G \cdot Vsat}{\sigma signal}\right)$.

Fixed Pattern Noise (FPN)

The FPN of an image sensor is the average pixel non-temporal noise divided by the average pixel voltage. The illumination source is the same as for the average sensitivity measurement. The FPN is calculated at coarse exposure settings of 0,10,150,250 and 302 with a gain set to 1. 10 frames are grabbed and averaged to produce a temporally independent frame before each calculation. FPN is expressed in mV.

Vertical Fixed Pattern Noise (VFPN)

VFPN describes the spatial noise in an image sensor related to patterns with a vertical orientation. The VFPN is defined as the standard deviation over all columns of the average pixel voltage for each column determined at zero exposure and zero illumination. VFPN is expressed in mV.

Shading

Shading describes how average pixel values per “block” change across the image sensor array. For fine shading calculations, the image sensor array is split into 30 pixel by 30 pixel blocks. An average value is then calculated for each block, averages are then compared across the whole device. The blocks are increased in size to 60 pixels by 60 pixels for the gross shading calculation. Shading is expressed in mV.

6.1 Optical characterisation results

Table 35: Optical characterization

Optical parameter	Red	Green	Blue	Unit
Average sensitivity	-	2.05	-	V/lux.s
Dark signal	-	9.0	-	mV/s
Temporal noise	-	2.12	-	mV
Dynamic Range	-	52	-	dB
SNR	-	37	-	dB
Fixed Pattern Noise	-	1.13	-	mV
Vertical fixed pattern noise	-	0.68	-	mV
Shading (Gross)	1.1	1.3	1.0	%

6.2 Blooming

We do not perform any test measurements for blooming.

Blooming is a phenomenon that does not affect CMOS sensors the same way as CCD imagers are afflicted. CCD blooming can cause an entire column or set of columns to flood and saturate.

7 Defect Categorisation

7.1 Introduction

Two distinct categories of defects are discussed in this section:

- Pixel defects (*Section 7.2*- *Section 7.5*)
- Physical aberrations (*Section 7.6*)

The two categories differ in terms of test methodology as explained below.

7.2 Pixel defects

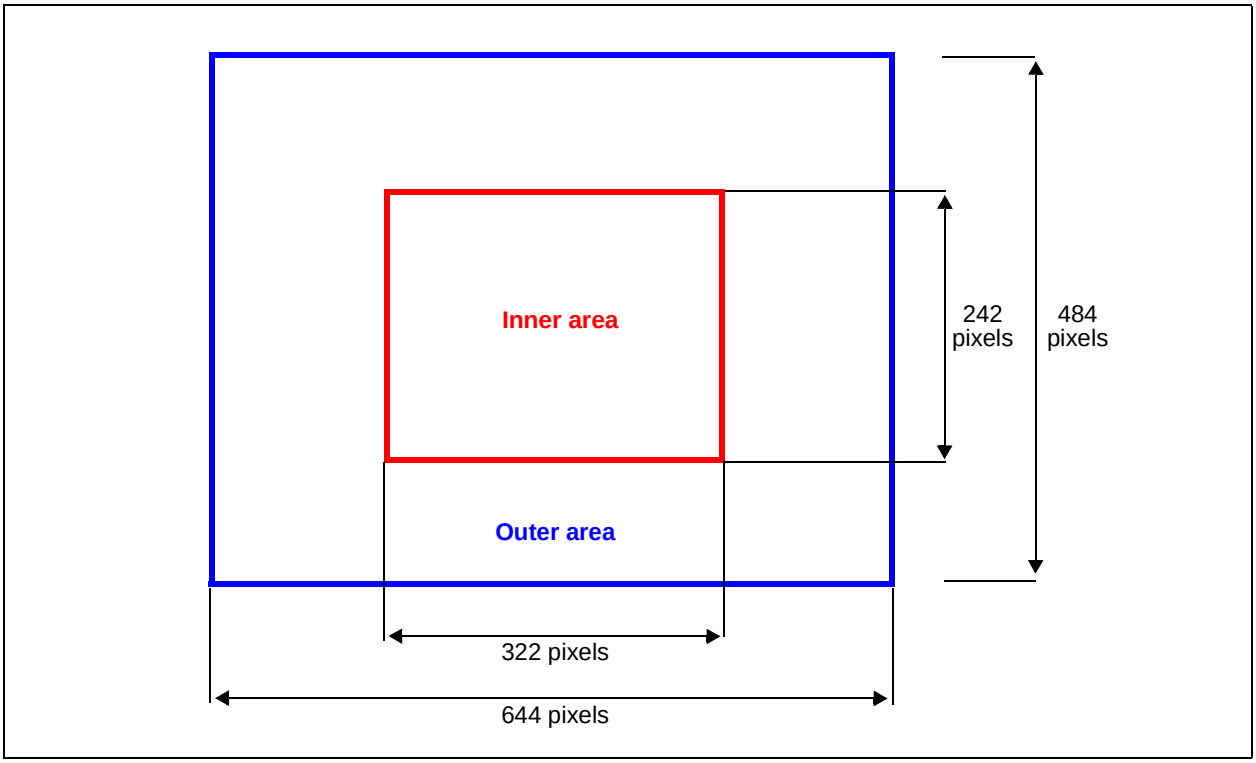
All packaged CMOS image sensors can contain impurities, either silicon faults, optical blemishes or external dirt particles which can be introduced in the product at various stages of the manufacturing process. These impurities can result in pixel defects, that is a pixel whose output is not consistent with the level of incident light falling on the image sensor. Precise definitions of the type of pixel defect tested by STMicroelectronics are outlined below. The ability to identify and correct these defects is central to both the design requirements and quality certification, via test of STMicroelectronics sensor products.

STMicroelectronics produces a number of hardware co-processors and software drivers that implement defect correction algorithms. The defect correction algorithms ensure that the VS6502 sensor in conjunction with a companion STMicroelectronics co-processor will produce a high quality final image.

7.3 Sensor array area definition

For specific aspects (refer to couplet test, see *Section 7.4.3*) of pixel defect testing, the image sensor array is subdivided into two regions as follows:

Figure 25: VS6502 array



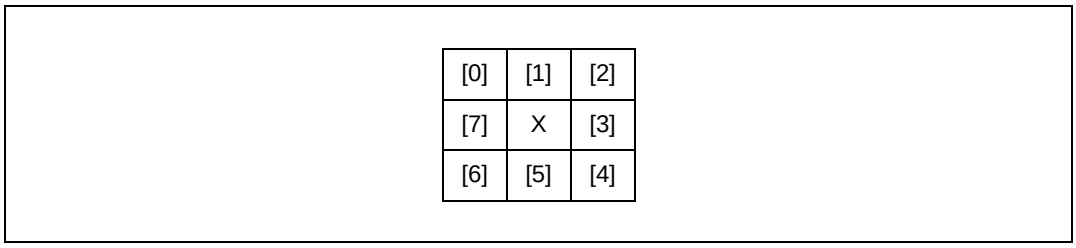
The inner array in *Figure 25* above is centre justified, in the x and y axis, with respect to the outer array. The inner array is 50% of the full width and 50% of the full height of the larger outer array, therefore the inner array is one quarter of the area of the outer array.

7.4 Pixel fault definitions

7.4.1 Pixel fault numbering convention

Please find the pixel notation described in *Figure 26* below. For test purpose, the 3x3 array describes 9 Bayer pixels of a common color, that is all the pixels will either be Red, Green or Blue. The pixel under test is **X**.

Figure 26: Pixel numbering notation

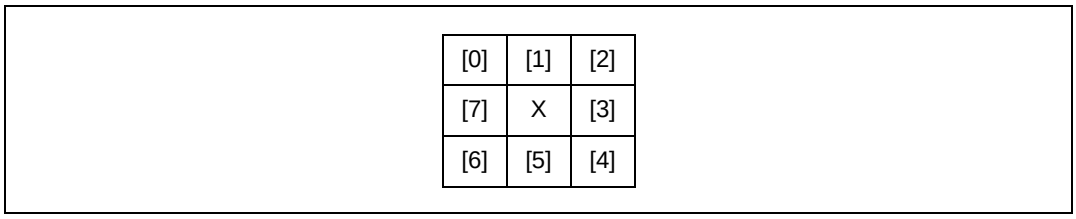


7.4.2 Single pixel faults

STMicroelectronics define a single pixel fail as a failing pixel with no adjacent failing neighbors of the same colour. A single pixel fail can be a “stuck at white” where the output of the pixel is permanently saturated regardless of the level of incident light and exposure level, a “stuck at black” where the pixel output is zero regardless of the level of incident light and exposure level or simply a pixel that differs from its immediate neighbors by more than the test threshold, that is differ by more than 8.0% from pixel average of color space neighbors.

In the example below in *Figure 27*, we assume that the pixel ‘X’ is a fail. This pixel is qualified as single pixel fail if the pixels at positions [0],[1],[2],[3],[4],[5],[6] and [7] are “good” pixels that pass the final test. The implemented test program qualifies a sensor with up to 120 single pixel faults. Defect correction algorithms correct the single pixel faults in the final image.

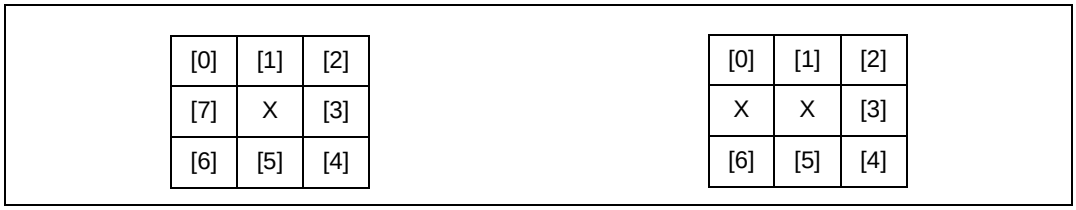
Figure 27: Single pixel fault



7.4.3 Couplet definition

A failing pixel at **X** with a failing pixel at position [0] or [1] or [2] or [3] or [4] or [5] or [6] or [7] such that there is a maximum of 2 failing pixels from the group of 9 pixels illustrated in *Figure 28* is described as a couplet fail. The example shown on the right in *Figure 28* has failing pixels at the centre location and at position [7].

Figure 28: General couplet examples



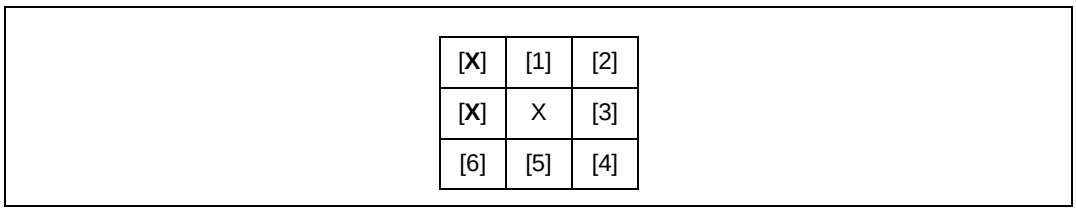
The basic couplet definition is further subdivided into minor and major couplets. With respect to the example in *Figure 28*, a minor couplet is defined as a defect pixel pair where one pixel can be an extreme fail, that is a “stuck at black” or “stuck at white”, but the second pixel in the pair must differ from the local pixel average by less than 15% of that average value. If the second pixel in the couplet differs by more than 15% of the local pixel average value then this would be defined as a major couplet.

Note that the test program considers a couplet as 2 independent pixels. If the test identifies two independent pixel fails (pixels that differ by more than 15% from pixel average of neighbors) that form a couplet with 2 minor pixel fails within the inner area, the device fails the test and is rejected. If however the test identifies 2 couplets where the pixels span the border between the inner and outer areas and where only one of the pixels in the inner area is determined as a major fail and the other a minor fail, then this device passes the test.

7.4.4 Cluster definition

We define a cluster fail as a failing pixel with at least two adjacent failing pixels. In the example from *Figure 29*, there are additional pixel fails in positions [0] and [7]. This example constitutes a cluster. A sensor containing a cluster is always rejected.

Figure 29: Cluster example



7.5 Summary pass criteria

Table 36: Sensor pixel defect pass criteria

Single pixel fails	Minor Couplet[a]	Major Couplet[b]	Clusters
<=120	1 (2)	0	0

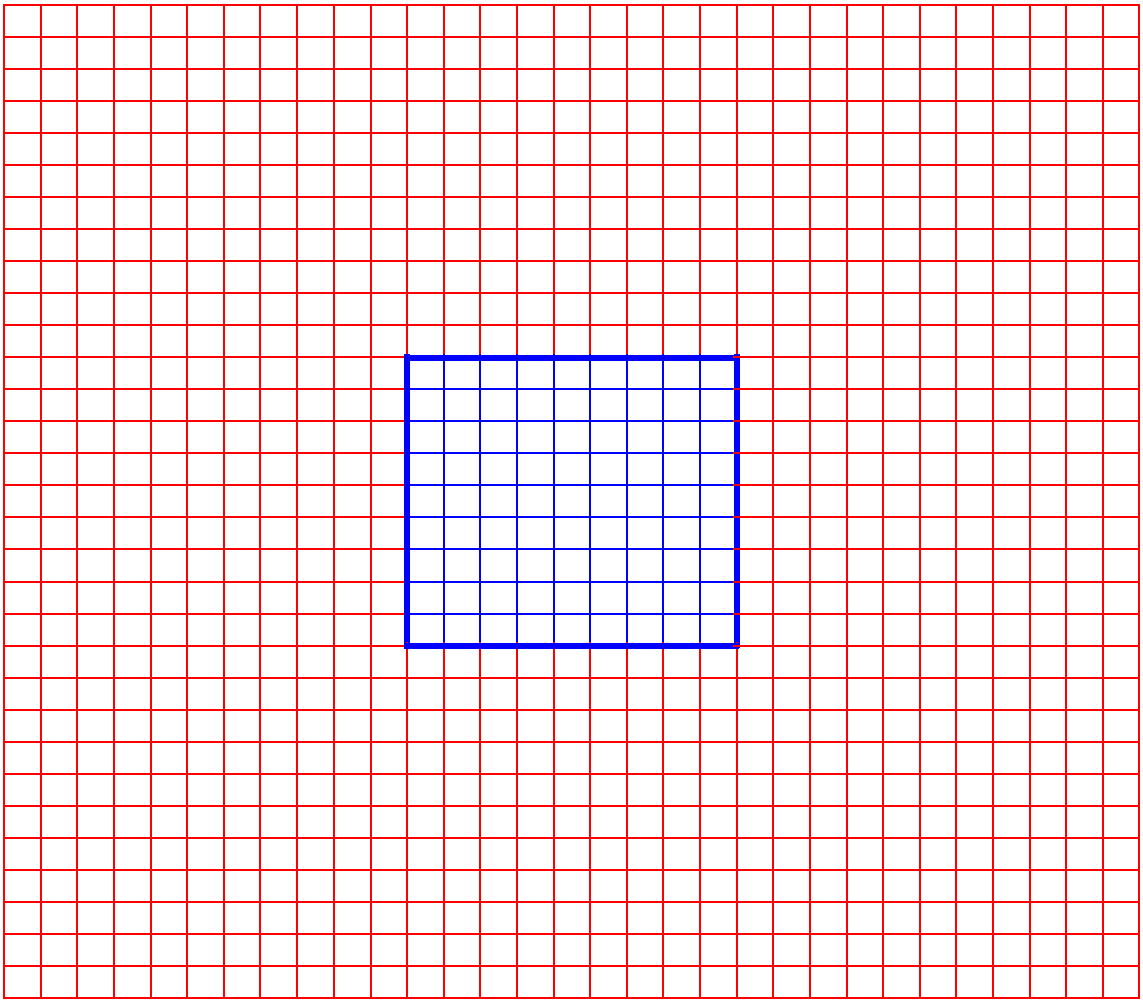
a. Test program will allow maximum of one minor couplet in inner zone of pixel array.
Test program will allow maximum of two minor couplets in outer zone of pixel array.
b. No major couplet allowed.

7.6 Physical aberrations

Silicon surface irregularities and external marks, both pits and deposits, on the package glass lids or lenses can cause a deterioration in image quality. STMicroelectronics recognize that this could compromise the product quality and therefore have introduced a specific test algorithm to identify and reject samples that display these phenomena. The pass/fail criteria for this test are given in *Section 7.6.1*.

7.6.1 Test details

Figure 30: Test area definition



The test defines 2 areas:

- A small area: 9 by 9 pixels with pixel under test at the centre of this area (shaded blue in *Figure 30*)
- A large region, 31 by 31 pixels (shaded red in *Figure 30*)

An average value is calculated for both the ‘small’ and ‘large’ areas.The areas then scan across the whole array so that every pixel is evaluated. Due to the nature of the test, only the red pixels are used. The next stage of the test is the creation of a pixel map with the coordinates of the failing pixels. A pixel location is identified as a fail in the map if it satisfies the criteria outlined in *Table 37* below.

Table 37: Criteria for pixel to be entered in failure map

Pixel location is a fail in map if
Small average < Large average - (1.2% of Large average) or Small average > Large average + (1.2% of Large average)

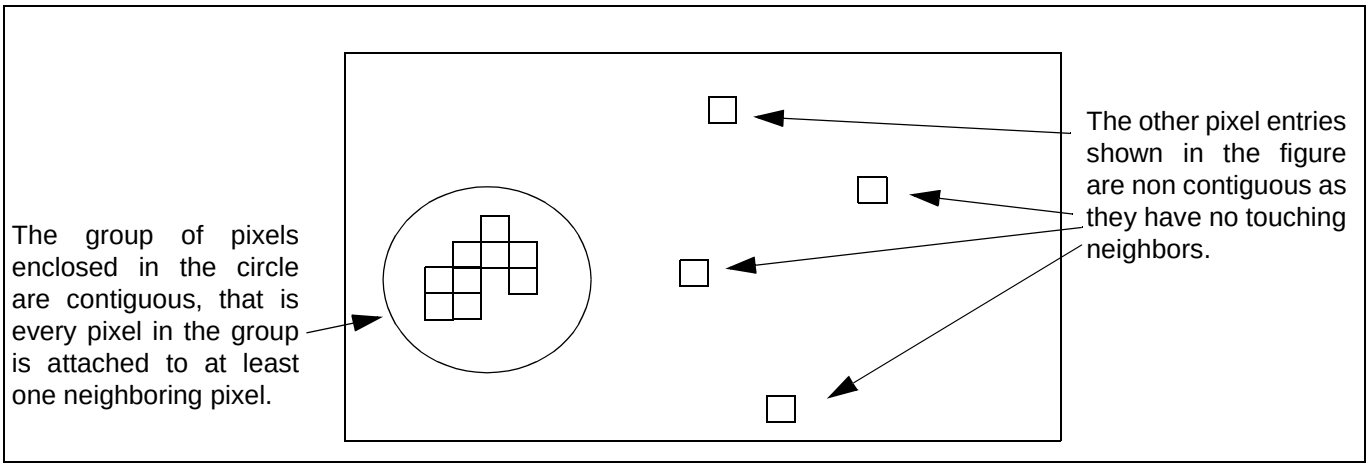
The contents of the fail map determine whether the sensor fails the physical aberration test. The fail criteria are given in *Table 38* below:

Table 38: Physical aberration test fail criteria

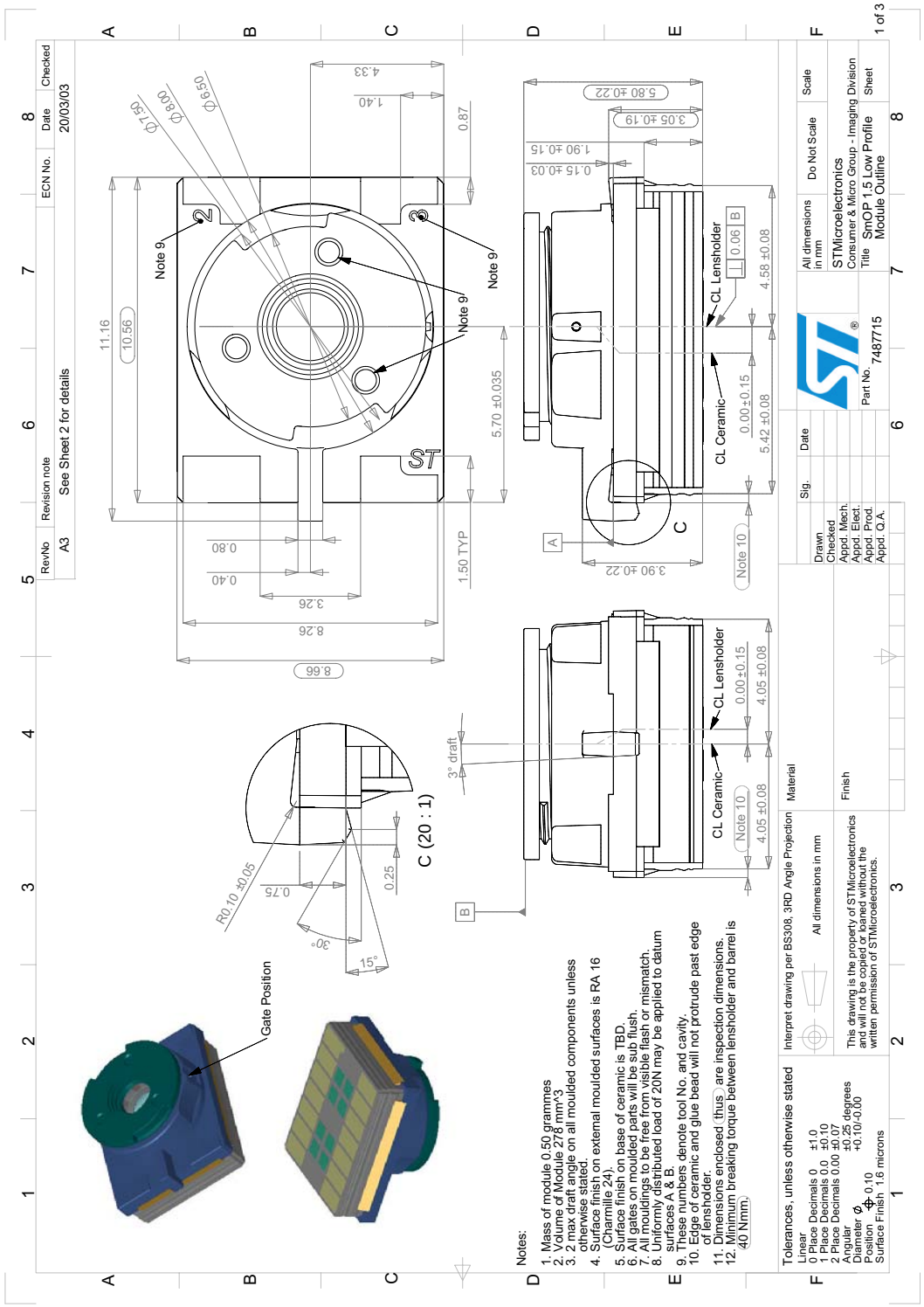
Fail physical aberration test if
> 82 contiguous[a] pixel entries in the failure map

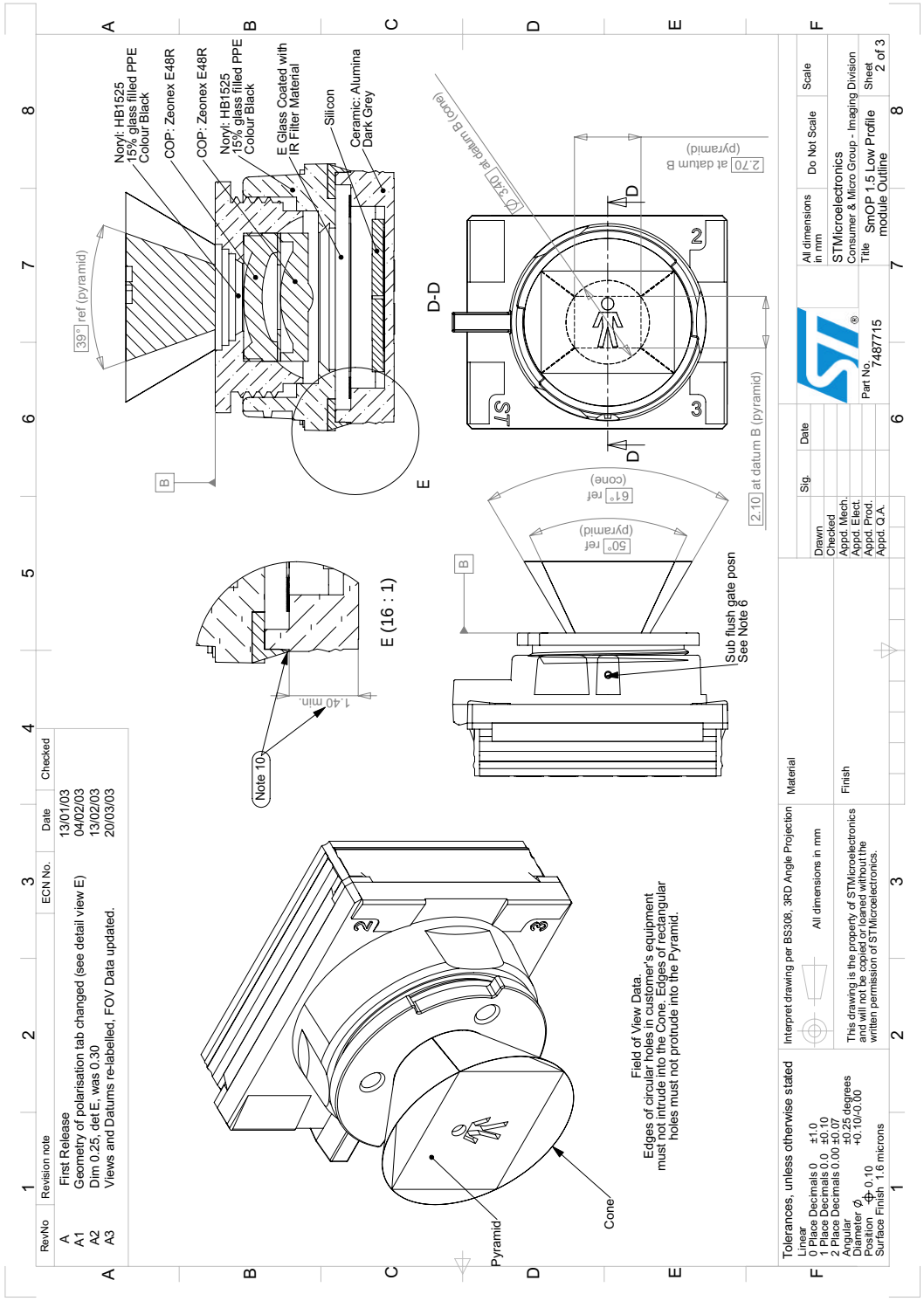
a. An example of contiguous pixels entries is given in *Figure 31*

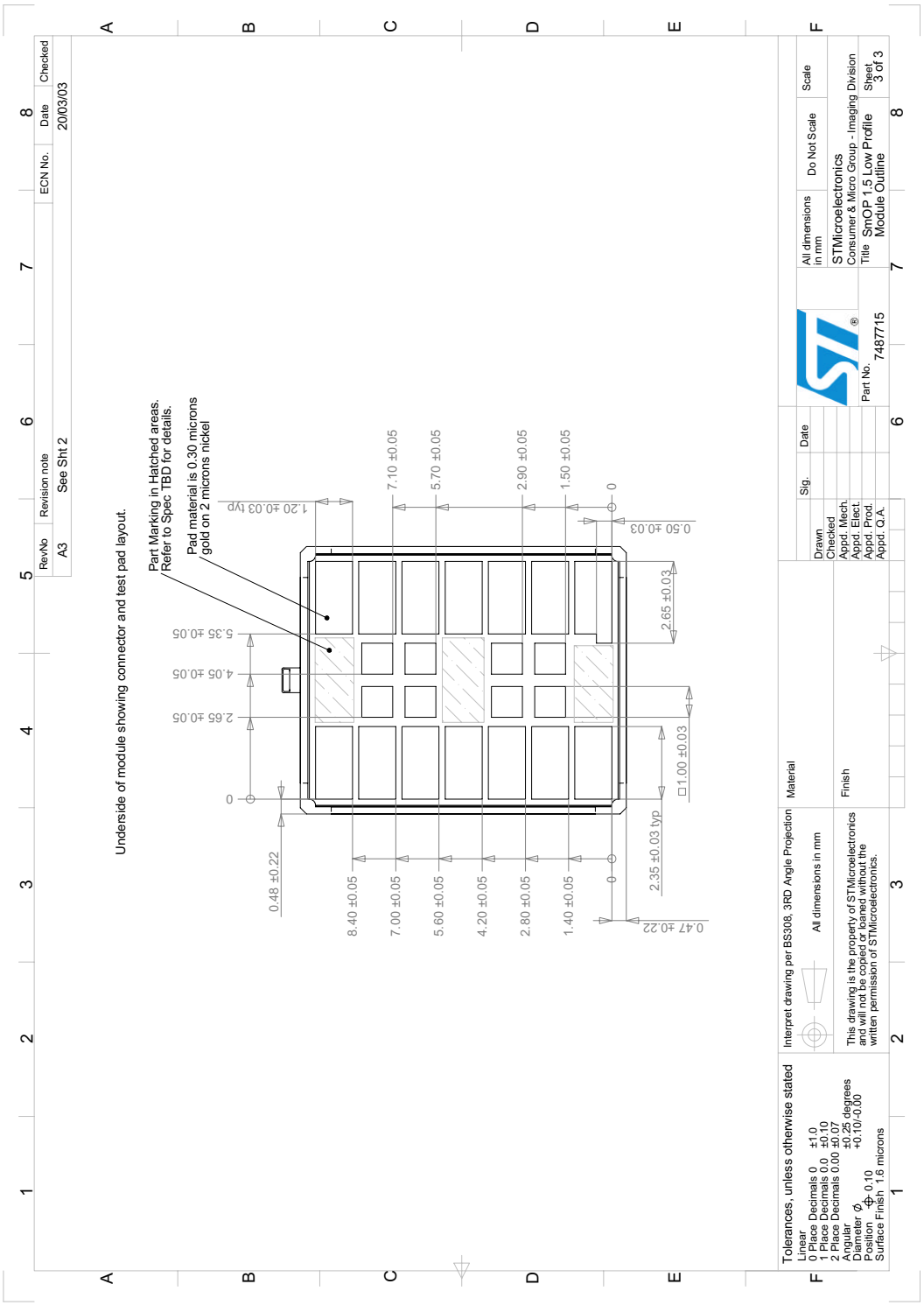
Figure 31: Contiguous pixels example



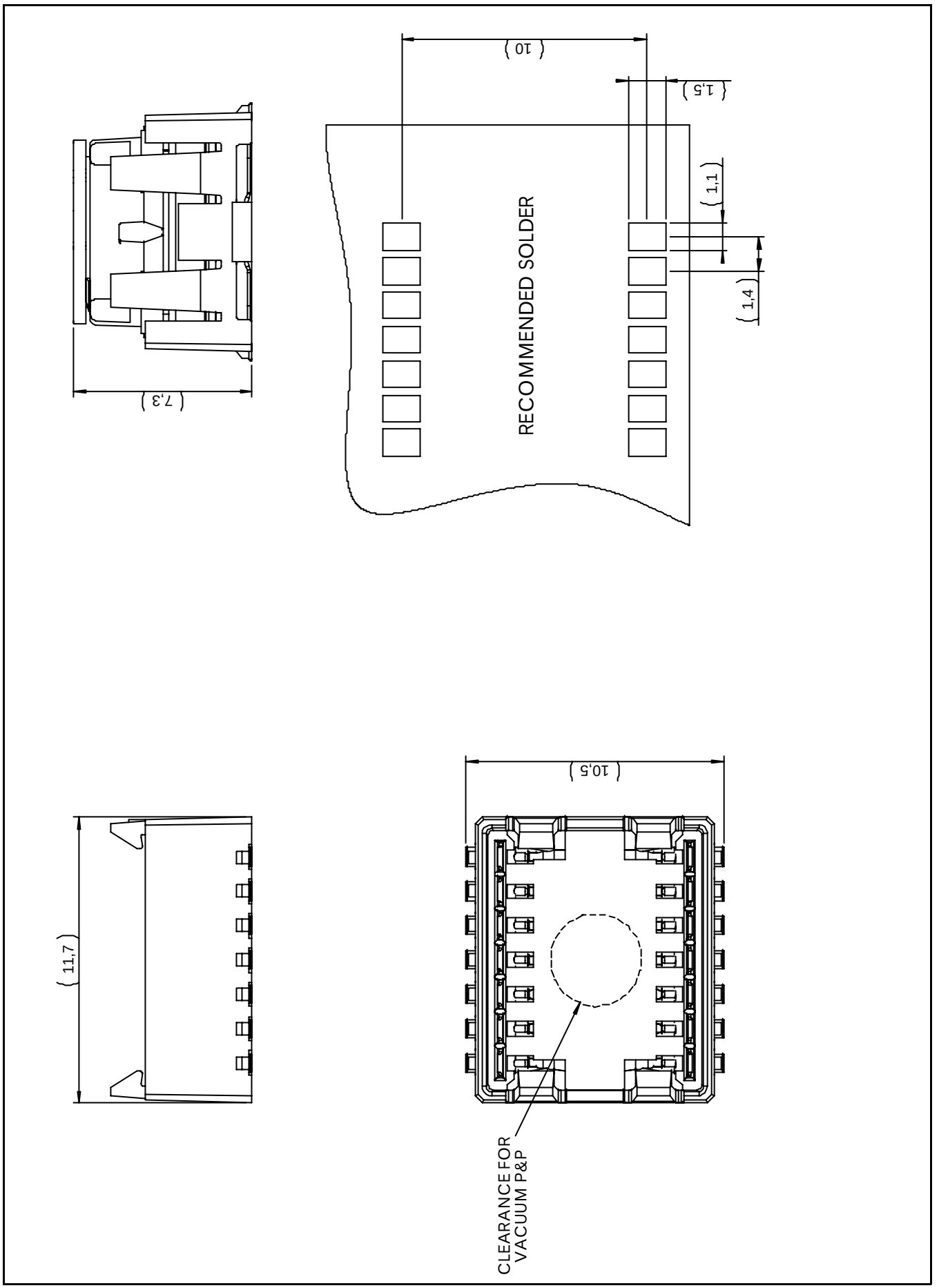
8 Package Mechanical Data




Noryl: HB1525
15% glass filled PPE
Colour Black
COP: Zeonex E48R
COP: Zeonex E48R
Noryl: HB1525
15% glass filled PPE
Colour Black
E Glass Coated with
IR Filter Material
Silicon
Ceramic: Alumina
Dark Grey
39° ref (pyramid)
D-D
E (16 : 1)
Note 10
1.40 min.
Sub flush gate posn
See Note 6
2.10 at datum B (pyramid)
50° ref (pyramid)
61° ref (cone)
2.70 at datum B (pyramid)
Field of View Data.
Edges of circular holes in customer's equipment
must not intrude into the Cone. Edges of rectangular
holes must not protrude into the Pyramid.
Pyramid
Cone
RevNo
Revision note
ECN No.
Date
Checked
A First Release 13/01/03
A1 Geometry of polarisation tab changed (see detail view E) 04/02/03
A2 Dim 0.25, det E, was 0.30 13/02/03
A3 Views and Datums re-labelled, FOV Data updated. 20/03/03
Tolerances, unless otherwise stated
Linear
0 Place Decimals 0 ±1.0
1 Place Decimals 0.0 ±0.10
2 Place Decimals 0.00 ±0.07
Angular ±0.25 degrees
Diameter Ø +0.10/-0.00
Position ⌖ 0.10
Surface Finish 1.6 microns
Interpret drawing per BS308, 3RD Angle Projection
All dimensions in mm
Material
Finish
This drawing is the property of STMicroelectronics
and will not be copied or loaned without the
written permission of STMicroelectronics.
Drawn
Checked
Appd. Mech.
Appd. Elect.
Appd. Prod.
Appd. Q.A.
Sig.
Date
Part No. 7487715
All dimensions in mm
Do Not Scale
Scale
STMicroelectronics
Consumer & Micro Group - Imaging Division
Title SmOP 1.5 Low Profile module Outline
Sheet 2 of 3


Underside of module showing connector and test pad layout.
Part Marking in Hatched areas. Refer to Spec TBD for details.
Pad material is 0.30 microns gold on 2 microns nickel
1.20 ±0.03 typ
7.10 ±0.05
5.70 ±0.05
2.90 ±0.05
1.50 ±0.05
0
0.50 ±0.03
2.65 ±0.03
□1.00 ±0.03
5.35 ±0.05
4.05 ±0.05
2.65 ±0.05
0
0.48 ±0.22
8.40 ±0.05
7.00 ±0.05
5.60 ±0.05
4.20 ±0.05
2.80 ±0.05
1.40 ±0.05
0
2.35 ±0.03 typ
0.47 ±0.22
RevNo A3
Revision note See Sht 2
ECN No.
Date 20/03/03
Checked
Tolerances, unless otherwise stated
Linear
0 Place Decimals ±1.0
1 Place Decimals 0.0 ±0.10
2 Place Decimals 0.00 ±0.07
Angular ±0.25 degrees
Diameter Ø ⊕ 0.10 +0.10/-0.00
Position ⊕ 0.10
Surface Finish 1.6 microns
Interpret drawing per BS308, 3RD Angle Projection
All dimensions in mm
This drawing is the property of STMicroelectronics and will not be copied or loaned without the written permission of STMicroelectronics.
Material
Finish
Sig.
Date
Drawn
Checked
Appd. Mech.
Appd. Elect.
Appd. Prod.
Appd. Q.A.
Part No. 7487715
All dimensions in mm
Do Not Scale
Scale
STMicroelectronics
Consumer & Micro Group - Imaging Division
Title SmOP 1.5 Low Profile Module Outline
Sheet 3 of 3

9 Socket Mechanical Data



10 Evaluation Hardware

There is no ‘sensor only’ evaluation kit for the VS6502, however the daughtercard may be used with the evaluation kit for the SVTV676 and STVC674 coprocessors

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Table 39: Evaluation Hardware

Part Number	Description
VS6502V015	Sensor module only
XS0015/TR	Socket
STV-6502V-D01	VS6502 daughter card compatible with the following two EVKs
STV-674/100T-E01	EVK for STV0674 coprocessor
STV-676-E01	EVK for STV0676

Revision History

Revision	Date	Changes
A	April 2004	First version.
B	8th June 2004	Major changes. Second internal review and approval cycle via ADCS

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