VS6552

VGA Color CMOS Image Sensor Module

FEATURES

- Small physical size
- Ultra low power standby mode
- SmOP (Small Optical Package) technology featuring integrated lens
- Class leading low light performance
- VGA resolution sensor
- Compatible with STV0974 companion mobile processor
- High frame rate to minimize image distortion
- Low EMI link (VisionLink) to STV0974
- On-chip 10-bit ADC
- Automatic dark calibration
- I^2C communications
- On-chip PLL

DESCRIPTION

The VS6552 is a VGA resolution SmOP sensor module. SmOP technology combines the image sensor and fixed focus lens system in a single module. This approach provides a number of advantages:

- SmOP technology is suitable for high volume manufacturing
- SmOP can be plugged into a PCB mounted flow soldered socket
- SmOP can be mounted close to noisy RF source as differential signalling used to transmit data has good immunity from radio interference.

The sensor outputs raw Bayer colorized data to the STV0974 companion mobile processor. STV0974 then performs all color processing and exposure control functions before outputting the data in an appropriate interface format like YCbCr, RGB or JPEG.

VS6552 offers an ultra low power standby mode that consumes less than 15 µW.

The SmOP lens has been designed to combine class leading low light performance with good depth of field to ensure excellent overall optical performance. The lens is a 2 element moulded plastic design.

The output data and qualification clock are transmitted over low noise, low voltage and fully differential links. VS6552 configuration registers are controlled via a private I^2C interface to STV0974.

APPLICATIONS

- Mobile phone embedded camera system
- PDA embedded camera or accessory camera
- Wireless security camera

Table 1. Technical Specifications

Pixel resolution	644 x 484 (VGA)
Pixel size	5.6 µm x 5.6 µm
Exposure control	+81 dB
Analog gain	+24 dB (max)
Dynamic range	60 dB (Typical)
Signal to noise at 50cd.m^2	37 dB (Typical)
Supply voltage	2.8 V (analog supply) 1.8 V (digital supply)
Power consumption	<75 mW (@30 frame/s) <15 µW (standby mode)
Package size	10.7mm x 8.7mm x 6mm:SmOP1.5 9.5mm x 8.5mm x 6.1mm :SmOP2
Lens	45^o HFOV, f# 2.8
Package type	14 pad SmOP
System attach	Socket or flexible circuit

Table 2. Order Codes

Part Number	Operating Temperature	Package
VS6552V015/T2	[-25; +55] °C	SmOP1.5
VS6552V02C/T2	[-25; +55] °C	SmOP2M
VS6552V02D/T2	[-25; +55] °C	SmOP2ME

TABLE OF CONTENT

1 OVERVIEW

1.1 Sensor Overview

The VS6552 VGA image sensor produces raw VGA digital video data at up to 30 frames per second. The image data is digitized using an internal 10-bit column ADC. The resulting 10-bit output data includes embedded codes for synchronization. The data is formatted and transmitted over a fully differential link. The data is accompanied by a qualifying clock that is transmitted over an identical fully differential link.

The sensor is fully configurable using an I^2C interface.

The sensor is optimized for high volume mobile applications

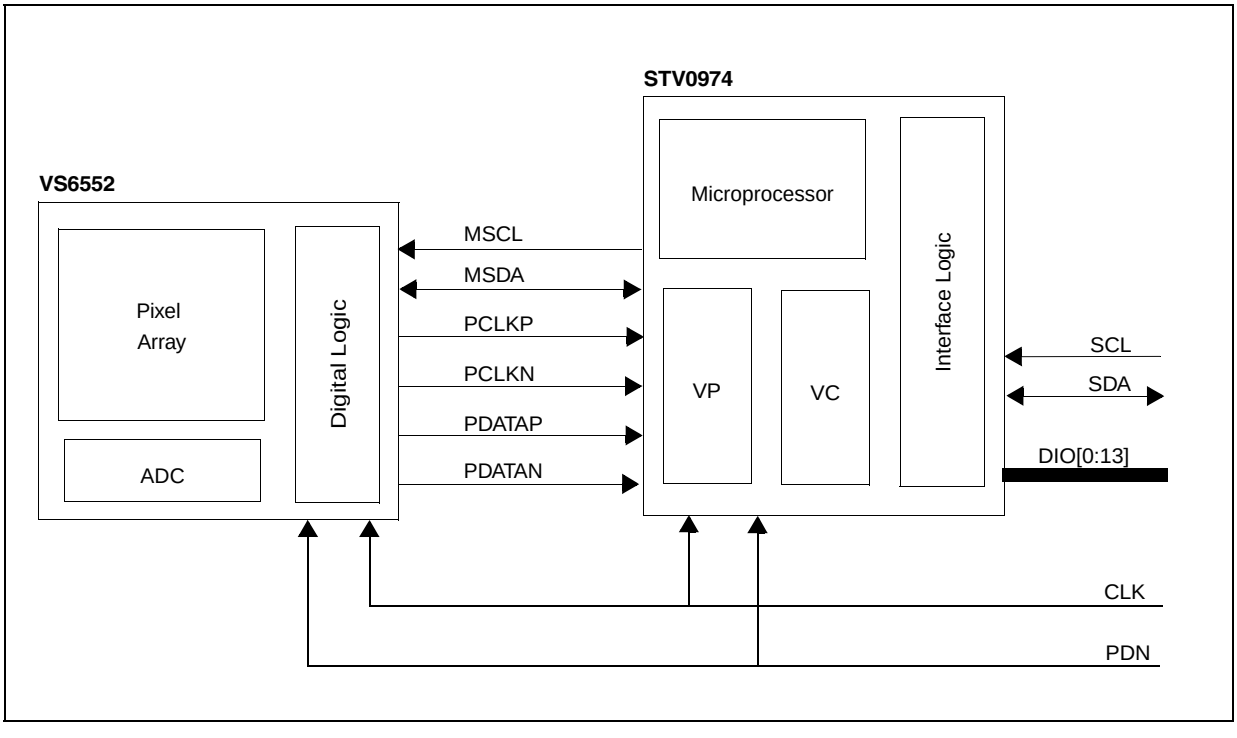
1.1.1 Typical Application - Mobile Application

The VS6552 is an image sensor, it should be used in conjunction with the STMicroelectronics STV0974 companion processor. The coprocessor and the sensor together form a complete imaging system.

The sensors main function is to convert the viewed scene into a data stream. The companion processor function is to manage the sensor so that it can produce the best possible data and to process the data stream into a form which is easily handled by up stream mobile baseband or MMP chipsets.

The sensor supplies high speed clock signal to the processor and provides the embedded control sequences which allow the co processor to synchronize with the frame and line level timings. The processor then performs the color processing on the raw image data from the sensor before supplying the final image data to the host.

Figure 1. Camera System Using STV0974



2 SIGNAL DESCRIPTION

Table 3. Signal Description

Pad Number	Pad Name	I/O Type	Description
Power supplies			
1	CEXT	PWR	Connection to capacitor[a]
2	AGND	PWR	Analog ground
3	AVDD	PWR	Analog power
8	GND	PWR	Digital ground
11	VDD	PWR	Digital power
System			
4	PDN	I	Power down control[b]
5	CLK	I	System clock input
Control			
6	MSCL	I	Serial communication clock
7	MSDA	I/O	Serial communication data
Data			
9	PCLKN	vLVDS output	Output qualifying clock
10	PCLKP	vLVDS output	Output qualifying clock
12	PDATAN	vLVDS output	Serial output data
13	PDATAP	vLVDS output	Serial output data
Not connected			
14	Not connected		
NC	Not connected		

a.Internally generated voltage that needs to be externally decoupled with a 100 nF, 5 V capacitor

b.Signal is active low

Note: The physical position of the signals on the package can be found by refering to the pinout information in Chapter 7: Package Mechanical Data.

3 FUNCTIONAL DESCRIPTION

The first sections of this chapter detail the main blocks in the device:

- Analog video block
- Digital video block

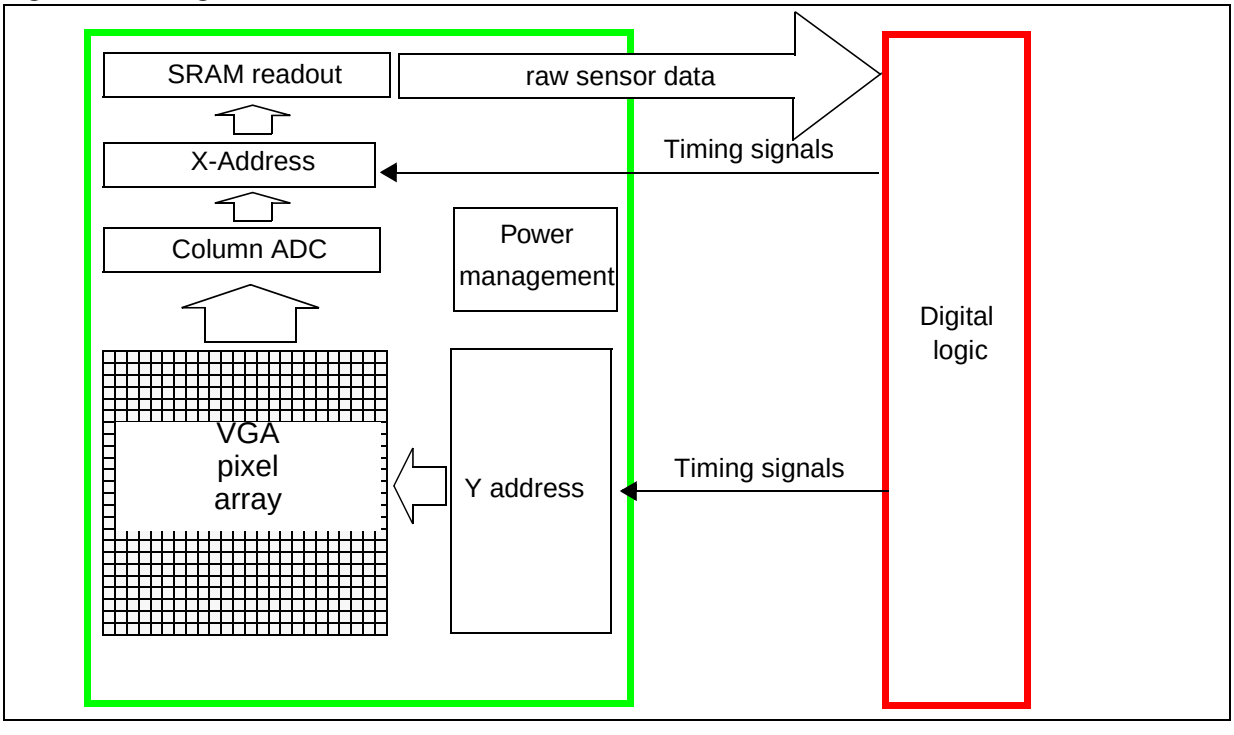
The later sections of this chapter describe other functional aspects of the device. Device level operating modes, including suspend, are detailed

3.1 Analog Video Block

3.1.1 Features

- ADC: 10-bit A/D converter - SRAM readout
- Dynamic range 60 dB (typical)
- SNR 37 dB @ 50 cd.m^2 (typical)

Figure 2. Analog Video Block



3.1.2 Analogue Block Diagram

The analog video block from Figure 4, consists of a VGA resolution pixel array, power management circuitry. The digital block provides all timing signals to drive the analog block.

Pixel voltage values are read out and digitized using the address decoders and column ADC

3.2 Digital Video Block

3.2.1 Features

- Frame rate: 30 frame/s max. (VGA) can be reduced down to less than 3 frame/s (VGA)
- Automatic dark calibration to ensure consistent video level over varying scenes
- Fixed pattern noise (FPN) data gathering
- Line and frame statistics gathering
- On-chip Power-On-Reset cell
- Single video output format: VGA 640 x 480
- H - Scaler function to aid software only viewfinder implementations

3.2.2 Dark Calibration Algorithm

VS6552 runs a dark calibration algorithm on the raw image data to control the video offsets caused by dark current. This ensures that a high quality image is output over a range of operating conditions. First frame dark level is correctly calibrated, for subsequent frames the adjustment of the dark level is damped by a leaky integrator function to avoid possible frame to frame flicker.

3.2.3 Image Statistics

VS6552 generates image statistics which can be used by STV0974 as an input to an auto exposure controller (AEC), automatic gain controller (AGC) and automatic white balance (AWB). .

3.3 Device Operating Modes

3.3.1 Standby

This is the lowest power consumption mode. I^2C communications to STV0974 are not supported in this mode. The clock input pad, PLL and the video blocks are powered down.

3.3.2 Sleep Mode

Sleep mode preserves the contents of the I^2C register map. I^2C communications to STV0974 are supported in this mode. The sleep mode is selected via a serial interface command sent by STV0974. The data pads go high at the end of the current frame. At this point the video block and PLL power down. The internal video timing is reset to the start of a video frame in preparation for the enabling of active video. The values of the serial interface registers like exposure and gain are preserved. The system clock must remain active to allow communication with the sensor.

3.3.3 Clock Active Mode

This mode is similar to ‘sleep mode’ except that the PLL is now powered up to permit a PCLKP/PCLKN signal to be delivered to STV0974. The PDATAP/PDATAN pads remain inactive. The video block is powered down.

3.3.4 Idle Mode

VCAP is generated. The analog video block is now powered up but the array is held in reset and the output PDATAP/PDATAN pads remain high.

3.3.5 Video

The VS6552 streams live video to the STV0974.

Table 4. VS6552 Power-up Sequence

Mode	Design block powered down					Video data inhibit
	I2C	Digital	PLL & CLK pins[a b]	Output pins	Analog	
Standby (PDN low)	Yes	Yes	Yes	Yes	Yes	Yes
Sleep	No	Yes	Yes	Yes	Yes	Yes
Clock active	No	No	No	Yes	Yes	Yes
Idle	No	No	No	No	No	Yes
Video	No	No	No	No	No	No

a.PLL (Phase Locked Loop) generates fast system clock for STV0974
b.PLL, PCLKP and PCLKN pins

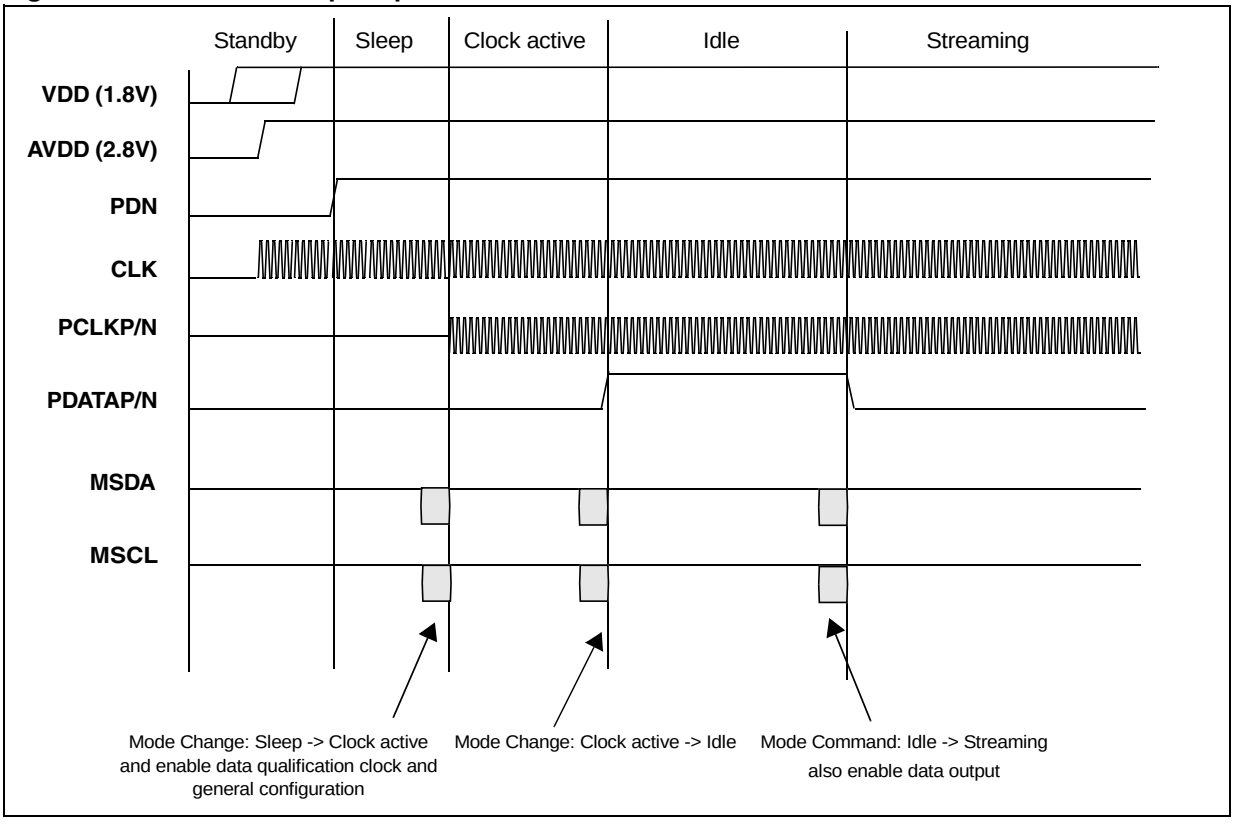
3.4 Power Management

VS6552 requires a dual power supply. The analog circuits are powered by a nominal 2.8 V supply while the digital logic and digital I/O are powered by a nominal 1.8 V supply.

3.4.1 Power-up, Power-down Procedures

The power up and power down procedures are detailed in the following Figure 3.

Figure 3. VS6552 Power-up Sequence



3.4.2 Active Signals with Unpowered VS6552

All signals going into the VS6552 must be either at a low state or high impedance when power is removed from the device. The exceptions to this rule are the I^2C lines which may be at a low or high state and the clock which can be active.

3.5 Clock and Frame Rate Timing

3.5.1 Video Frame Rate Control

The output frame rate of VS6552 can be reduced by extending the frame length. The extension is achieved by adding 'blank' video lines to act as timing padding. This is advantageous as it does not reduce the pixel readout rate and therefore does not introduce unwanted motion distribution effects to the image. The frame rate can be reduced from the default 30 frame/s at VGA resolution to less than 3 frame/s at VGA resolution.

3.5.2 PLL and Clock Input

A PLL IP block is embedded. This block generates all necessary internal clocks from an input range defined in Table 5. The input clock pad accepts up to 26 MHz signals.

Table 5. System Input Clock Frequency Range

System clock frequency[a]	
Min. (MHz)	**Max. (MHz)**
6.5	26

a. The standard supported input frequencies (in MHz) are as follows: 6.5, 8.4, 9, 9.6, 9.72, 12,13, 16.8, 18, 19.2, 19.44, 26.

3.5.3 Clock Input Type

VS6552 can receive the following clock types:

- Single ended CMOS
- Single ended Sine wave
- Clock can be AC or DC coupled

The clock is fail-safe.

3.6 Control and Video Interface Formats

3.6.1 Overview

Data is transferred from VS6552 to STV0974 via a high speed serial link (VisionLink). The serial data link comprises of two pairs of wires. The serial control data is transferred between the VS6552 to STV0974 via a private I^2C bus.

3.6.2 VisionLink Physical Layer

Data signals (PDATAP and PDATAN) and clock signals (PCLKP and PCLKN) are transferred from VS6552 to STV0974 via 2 pairs of balanced 100 Ω impedance transmission lines.

The transmission line pairs and custom transmitters/receivers realize a very low voltage differential (vLVDS) signalling scheme that can transfer information in a potentially noisy environment. As implemented in VS6552, VisionLink supports the transmission of raw Bayer data at VGA resolution up to 30 frame/s.

3.6.3 Serial I2C Control Bus

The internal registers in VS6552 can be configured by STV0974 via a private I^2C bus. STV0974 is the bus master and VS6552 is the single slave. VS6552 sends and receives commands over this bus at up to 400 kHz.

4 ELECTRICAL CHARACTERISTICS

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Values	Unit
VDIG	Digital power supply	-0.5 to 3.0	V
VANA	Analog power supply	-0.5 to 3.6	V
MSCL, MSDA	CCI Signals	-0.3 to VDIG + 0.3	V
PDN, CLK	Power Down Control, System Clock Input	-0.3 to VDIG + 0.3	V
T_{STO}	Storage temperature	-40 to + 85	^oC

Note: **Caution:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Operating Conditions

Symbol	ParTyp.ameter	Min.	Typ.	Max.	Unit
Voltage					
V_{DD}	Digital power supply voltage	1.7	-	1.9	V
AV_{DD}	Analog power supply voltage	2.5	-	3.3	V
Temperature					
T_{AF}	Temperature (functional operating)	-30	-	+70	°C
T_{AN}	Temperature (normal operating)	-25	-	+55	°C
T_{AO}	Temperature (optimal operating)	+5	-	+30	°C

Note: 1. **Storage temperature:** Camera has no permanent degradation
2. **Functional operating temperature:** Camera is electrically functional
3. **Normal operating temperature:** Camera produces ‘acceptable’ images
4. **Optimum performance temperature:** Camera produces optimal optical performance

4.1 DC Electrical Characteristics

Note: Typical values quoted for nominal voltage and temperature. Maximum values quoted for worse case operating conditions unless otherwise specified.

Table 8. Power Supply VDIG, VANA

Parameter	Typ.	Max.	Typ.	Max.	Unit
	Digital		Analogue		
Standby	1	5	NM[a]	<2	µA
Video, 30fps	15	20	9	15	mA

a.Not Measurable - current is below the minimum calibrated measurement capabilities of the test system (1µA)

Table 9. System Clock

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Leakage current		8[a]	29[b]	µA

a.With DC coupled square wave clock
b.With DC 1V9 signal level applied

Table 10. I2C Interface - MSDA, MSCL

Symbol	Parameter description	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage		-	0.3 VDIG	V
V_{IH}	High level input voltage	0.7 VDIG[a]	-		V
V_{OL}	Low level output voltage[b,c]		-	0.2 VDIG	V
I_{IL}	Low level input current		-	-10	µA
I_{IH}	High level input current		-	10	µA
f	Operating frequency range	0	-	400[d]	kHz

a.For positive electrostatic discharges above 500 V, a shift of V_{IH} may happen. However, the device remains fully functional even for a stress up to 2000 V included, and VIH<0.9 V_{DIG}. Refer to the STV0974 datasheet for recommendations on MSCL/MSDA usage.
b.V_{OH} not valid for CCI
c.1 mA drive strength
d.For external clock frequencies <19.2MHz Max limit is 200KHz

4.2 AC Electrical Characteristics

Table 11. System Clock

Symbol	Parameter description	Min.	Typ.	Max.	Unit
V_{CL}	DC coupled square wave (low level)		-	0.3 VDIG	V
V_{CH}	DC coupled square wave (high level)	0.7 VDIG			V
V_{CAC}	AC coupled sine wave[a]	0.5	1.0	1.2	V

Symbol	Parameter description	Min.	Typ.	Max.	Unit
f_{CLK}	Clock frequency input[a]	6.5 - 1%[a]	-	26 + 1%[b]	MHz

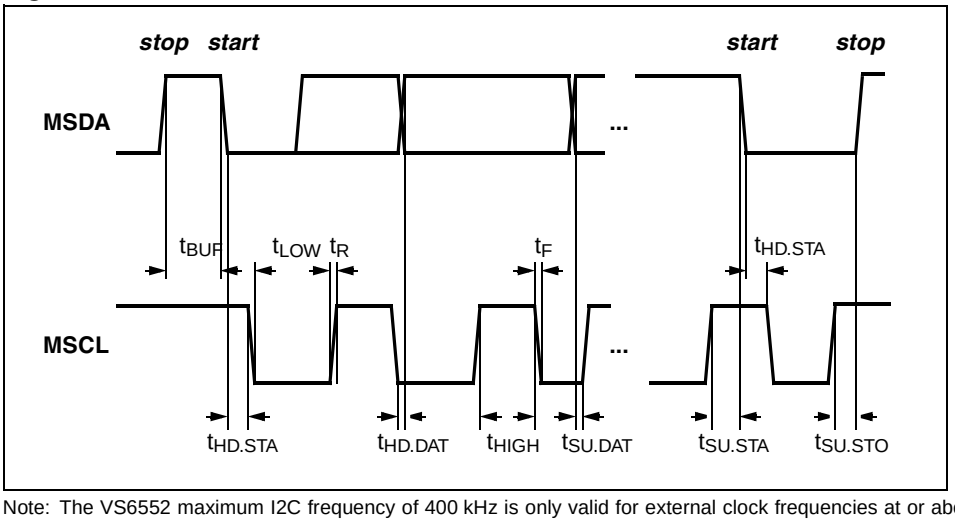
a.Nominal frequencies are 6.5 to 26MHz with a 1% center frequency tolerance

Table 12. Timing Characteristics

Symbol	Parameter description	Min.	Max.	Unit
t_{MSCL}	MSCL clock frequency	0	400	kHz
t_{LOW}	Clock pulse width low	1.3		µs
t_{HIGH}	Clock pulse width high	0.6		µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	0	50	ns
t_{BUF}	Bus free time between transmissions	1.3		µs
$t_{HD.STA}$	Start hold time	0.6		µs
$t_{SU.STA}$	Start set-up time	0.6		µs
$t_{HD.DAT}$	Data in hold time	0	0.9	µs
$t_{SU.DAT}$	Data in set-up time	100		ns
t_R	MSCL/MSDA rise time	$20+0.1C_b$[a]	300	ns
t_F	MSCL/MSDA fall time	$20+0.1\ C_b$	300	ns
$t_{SU.STO}$	Stop set-up time	0.6		µs
Ci/o	Input / Output capacitance (MSDA)		8	pF
Cin	Input capacitance (MSCL)		6	pF

a.Cb = total capacitance on the lines

Figure 4. CCI AC characteristics



Note: The VS6552 maximum I2C frequency of 400 kHz is only valid for external clock frequencies at or above 19.2 MHz. Due to a design issue, for external clock frequencies below 19.2MHz, the maximum guaranteed I2C frequency is limited to 200 kHz.

Table 13. vLVDS Interface AC Electrical Characteristics

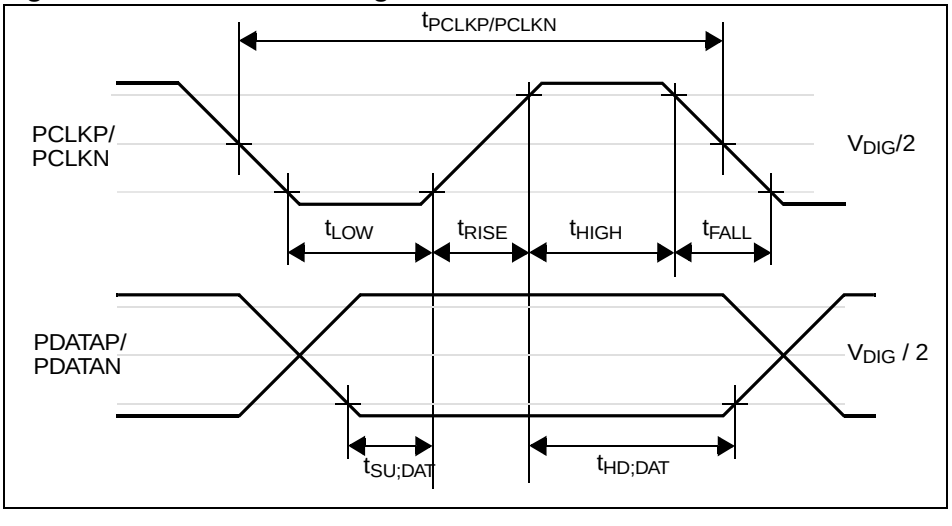
Symbol	Parameter description	Min.	Typ.	Max.	Unit
V_{od}	Differential voltage swing[a,b]	100	150	200	mV
V_{cm}	Common mode voltage (self biasing)	0.8	0.9	1.0	V
R_O	Output Impedance	40		140	W
I_{DR}	Drive current range (internally set by bias circuit)	0.5	1.5	2	mA

a.Supplies of VDIG = 1.8 V and VANA = 2.8 V, Temperature = 25 °C
b.Measured over a 100 Ohm load

Table 14. vLVDS TIming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
$f_{PCLKP/PCLKN}$	PCLKP/PCLKN clock frequency	-	-	120	MHz
$t_{PCLKP/PCLKN}$	PCLKP/PCLKN clock period	8.3	-	100	ns
	PCLKP/PCLKN duty cycle	26	-	74	%
t_{LOW}	Low period of PCLKP/PCLKN	1.66	-		ns
t_{HIGH}	High period of PCLKP/PCLKN	1.66	-		ns
t_{RISE}	Rise time of PDATAP/PDATAN, PCLKP/PCLKN	0.3	-	0.5	ns
t_{FALL}	Fall time of PDATAP/PDATAN, PCLKP/PCLKN	0.3	-	0.5	ns
$t_{HD;DAT}$	Data hold time	3	-	-	ns
$t_{SU;DAT}$	Data set-up time	1	-	-	ns

Figure 5. VisionLink AC timing



4.3 ESD Handling Characteristics

Table 15. ESD Handling Limits

Test	Method	Criteria
ESD Human Body Model	JESD22 A114A	2kV
ESD Machine Model	JESD22 A115A	200V
Latch Up	JESD78	1.5 * Vddmax, 150mA

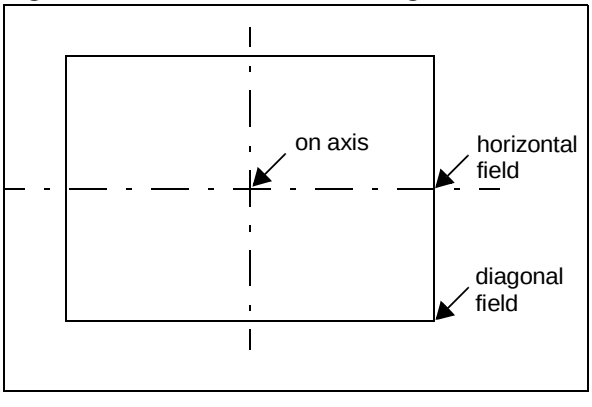
5 OPTICAL SPECIFICATION

The small amount of lens relative illumination effects (field darkening) is corrected by the STV0974.

Table 16. Optical Specifications

Parameter	Value
Effective Focal Length	4 mm ± 0.15 mm
Aperture	F2.8 aperture
Horizontal Field of View	$45^{o} \pm 2^{o}$
TV Distortion (pin,cushion & barrel)	-3% to 3%
MTF (*Figure 6.*) @ 60 cm @ 45 cycle/mm	– On axis: 45 % – Horizontal field: 30% – Diagonal field: 30%

Figure 6. MTF Points on the Image Field



6 DEFECT CATEGORIZATION

6.1 Pixel Defects

A packaged CMOS image sensor will display visual imperfections caused either by electrical faults or optical blemishes which can be introduced in the product at various stages of the manufacturing process. These impurities can result in pixel defects, that is a pixel whose output is not consistent with the level of incident light falling on the image sensor. The ability to identify and correct these defects is central to both the design requirements and quality certification, via test of STMicroelectronics sensor products.

The STMicroelectronics STV0974 co-processor implements defect correction algorithms which screens the presence of these defects in the final images. The defect correction algorithms ensure that the VS6552 sensor in conjunction with the STV0974 co-processor will produce a high quality final image.

7 PACKAGE MECHANICAL DATA

7.1 SmOP1.5 Module Outline

– Figure 7
– Figure 8
– Figure 9

7.2 SmOP2 M Module Outline

– Figure 10
– Figure 11
– Figure 12

7.3 SmOP2 ME Module Outline

– Figure 13
– Figure 14
– Figure 15

Figure 7. SmOP1.5 Module Outline

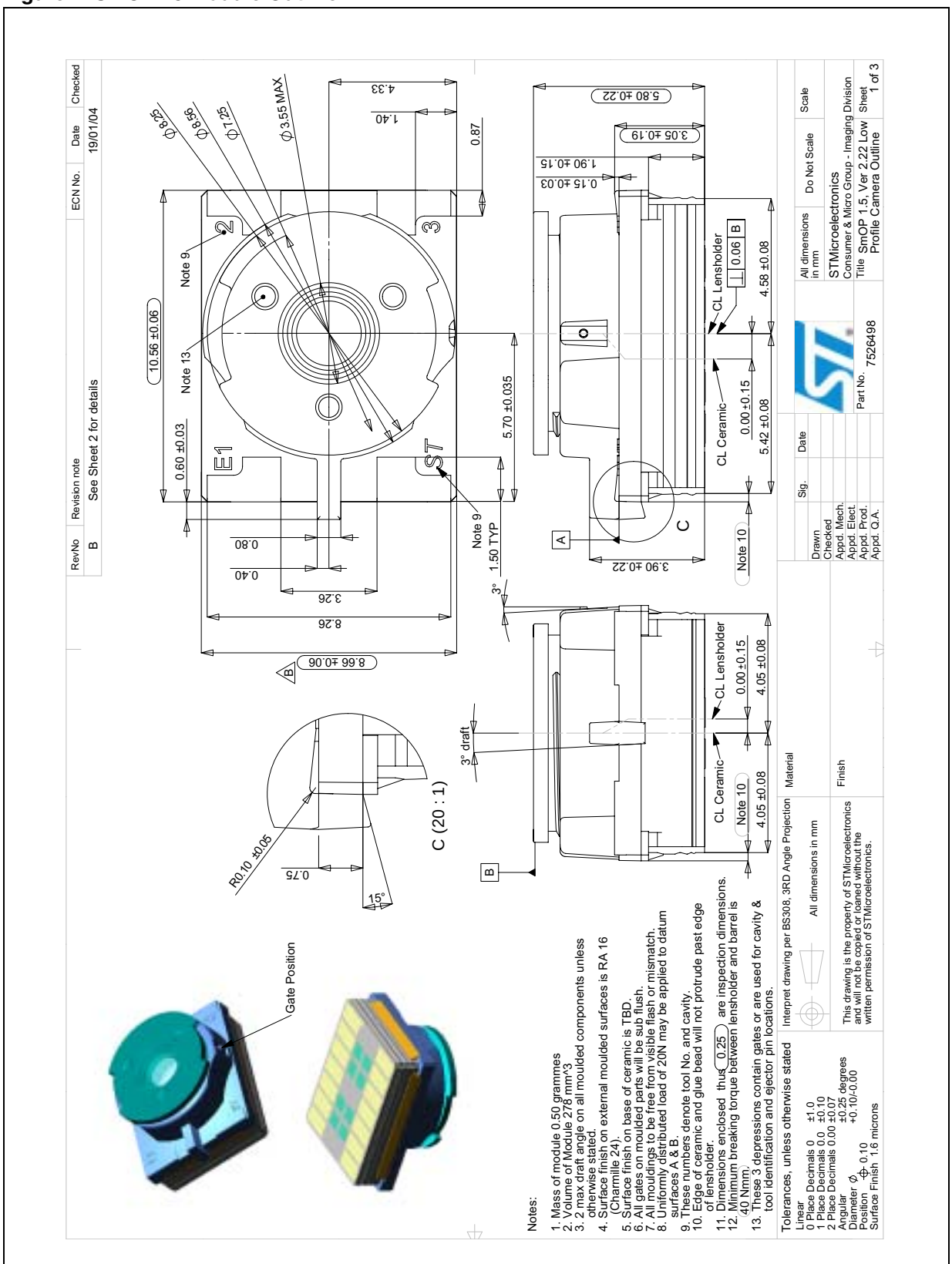


Figure 8. SmOP1.5 Module Outline

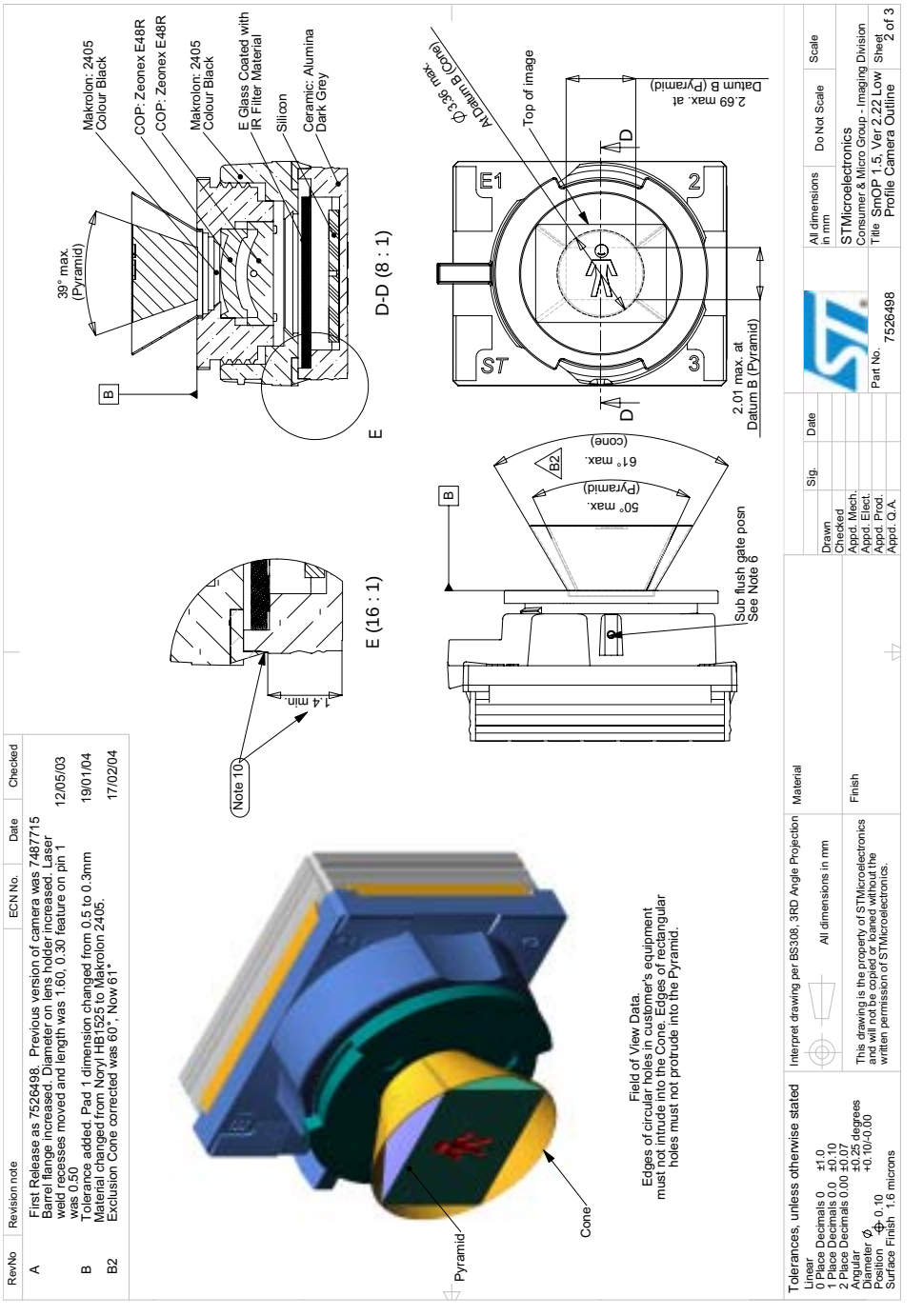


Figure 9. SmOP1.5 Module Outline

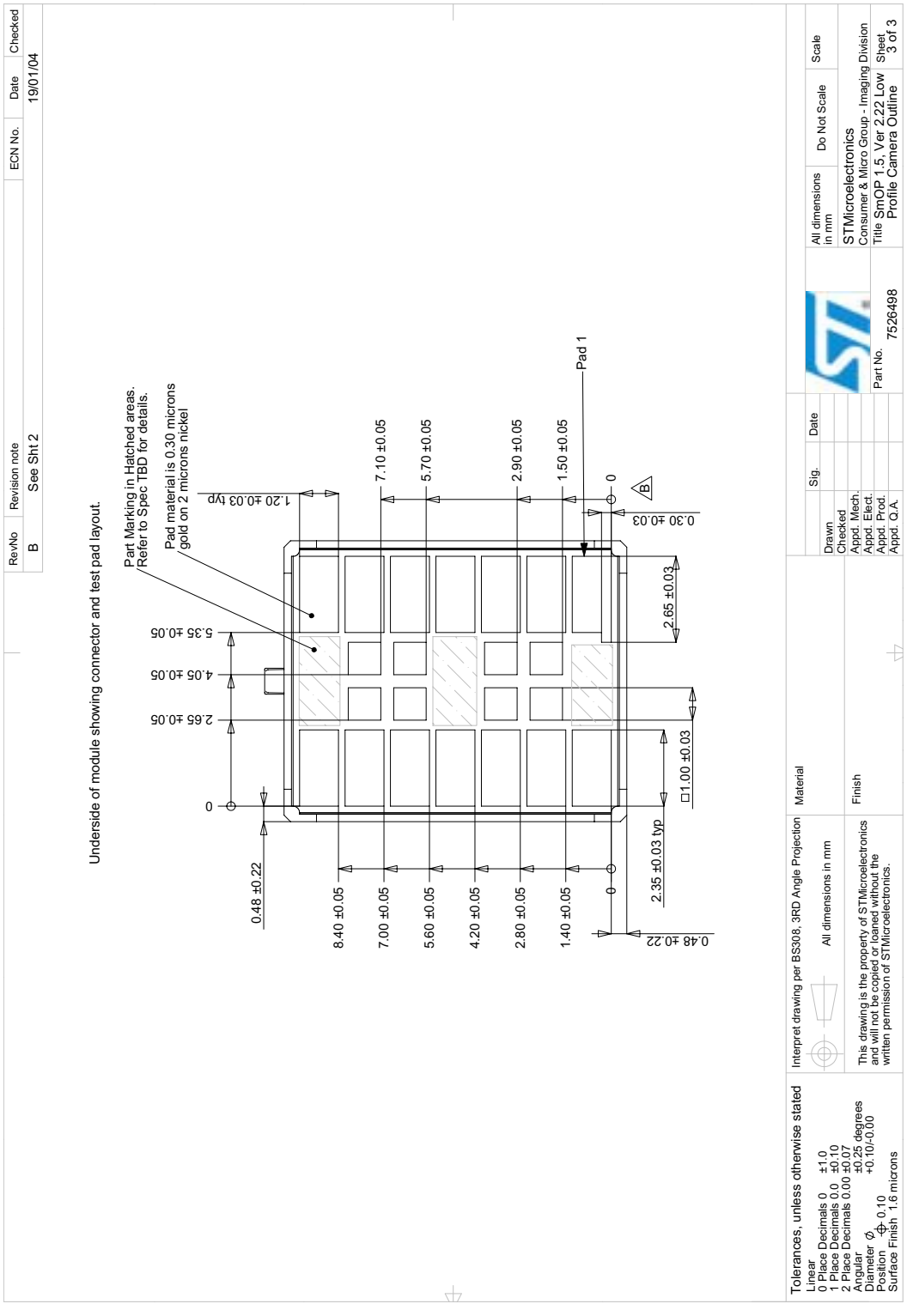


Figure 10. Module Outline (SmOP 2M)

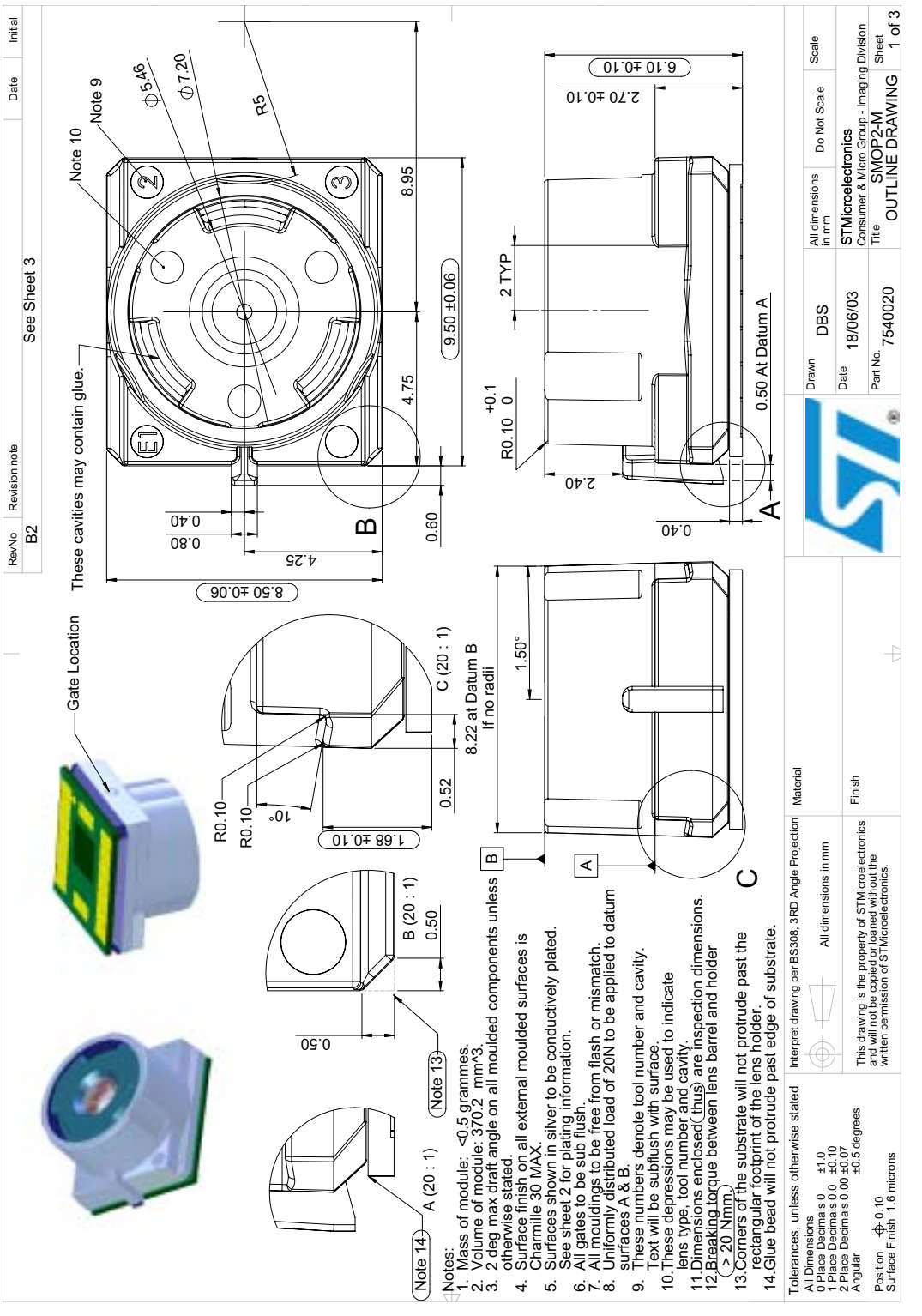


Figure 11. SmOP2 Module Outline

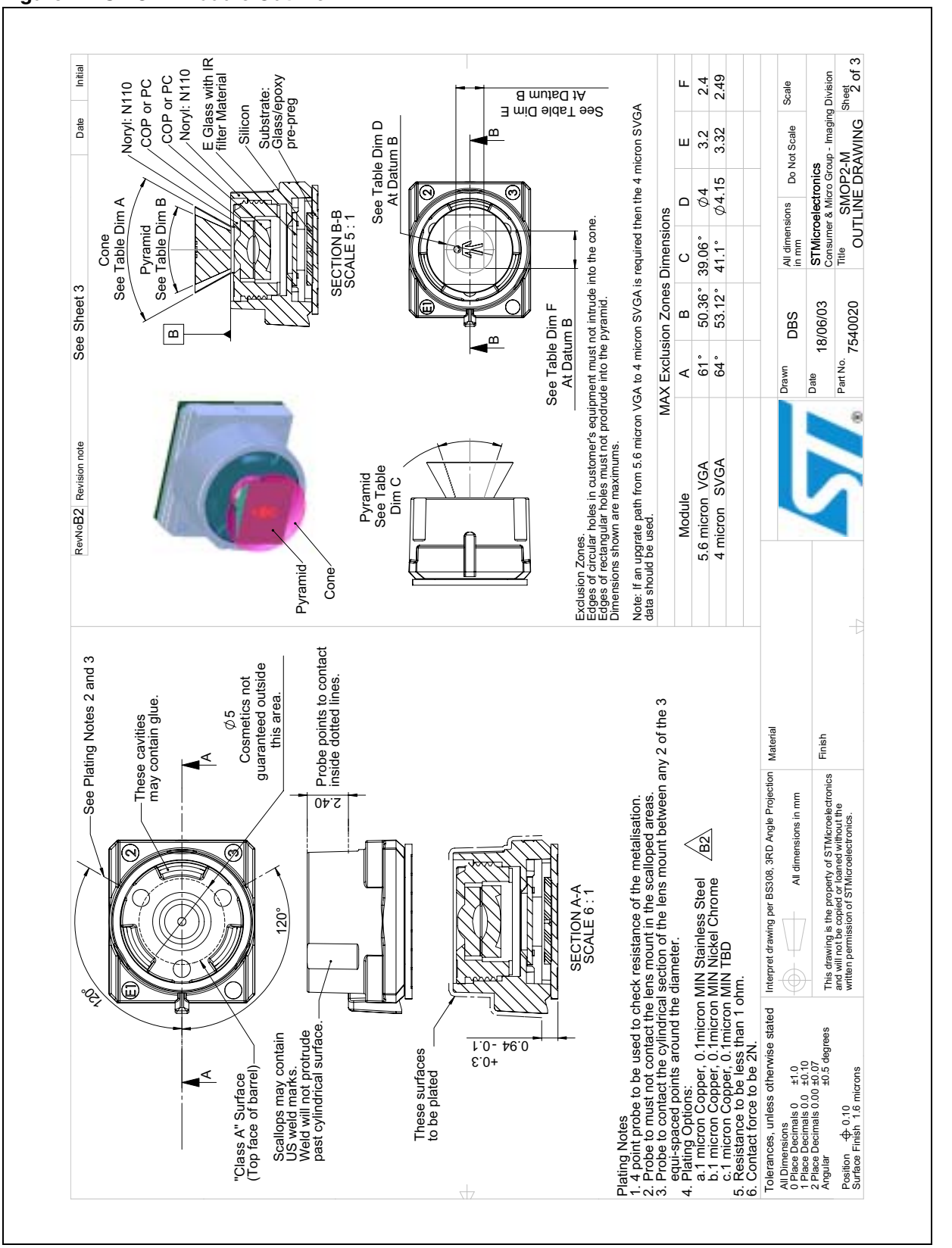


Figure 12. SmOP2 Module Outline

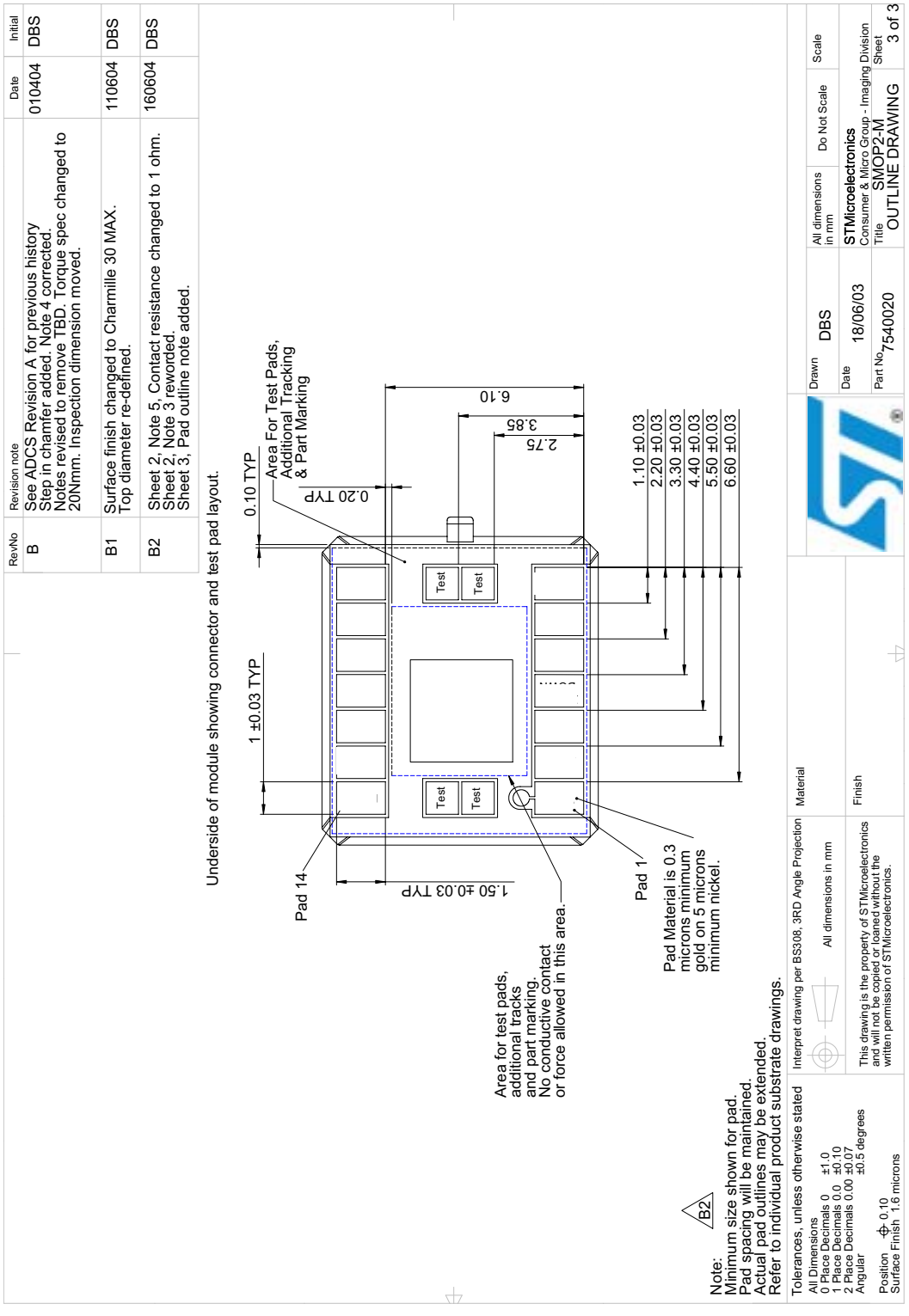


Figure 13. SmOP2 Module Outline

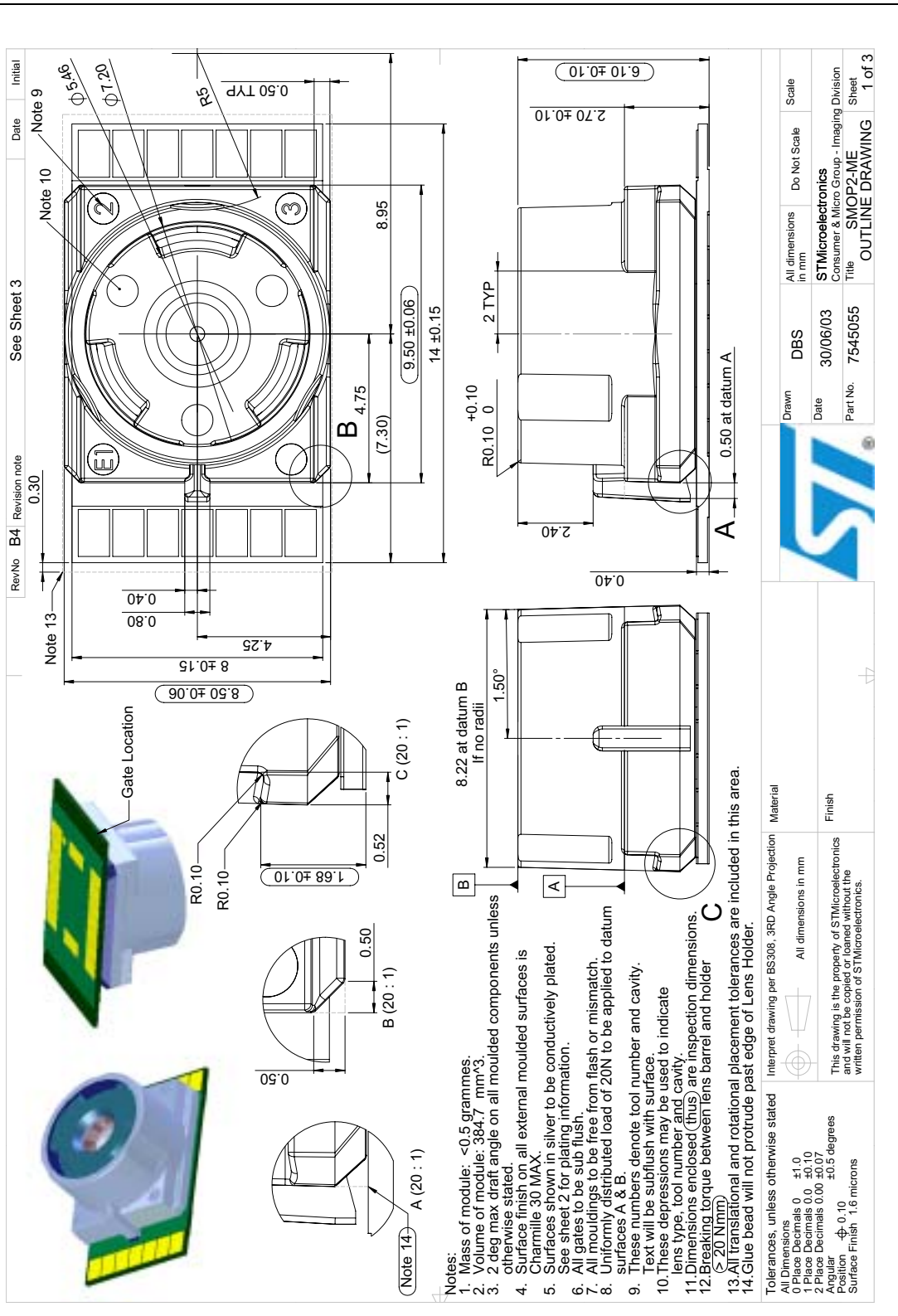


Figure 14. SmOP2 Module Outline

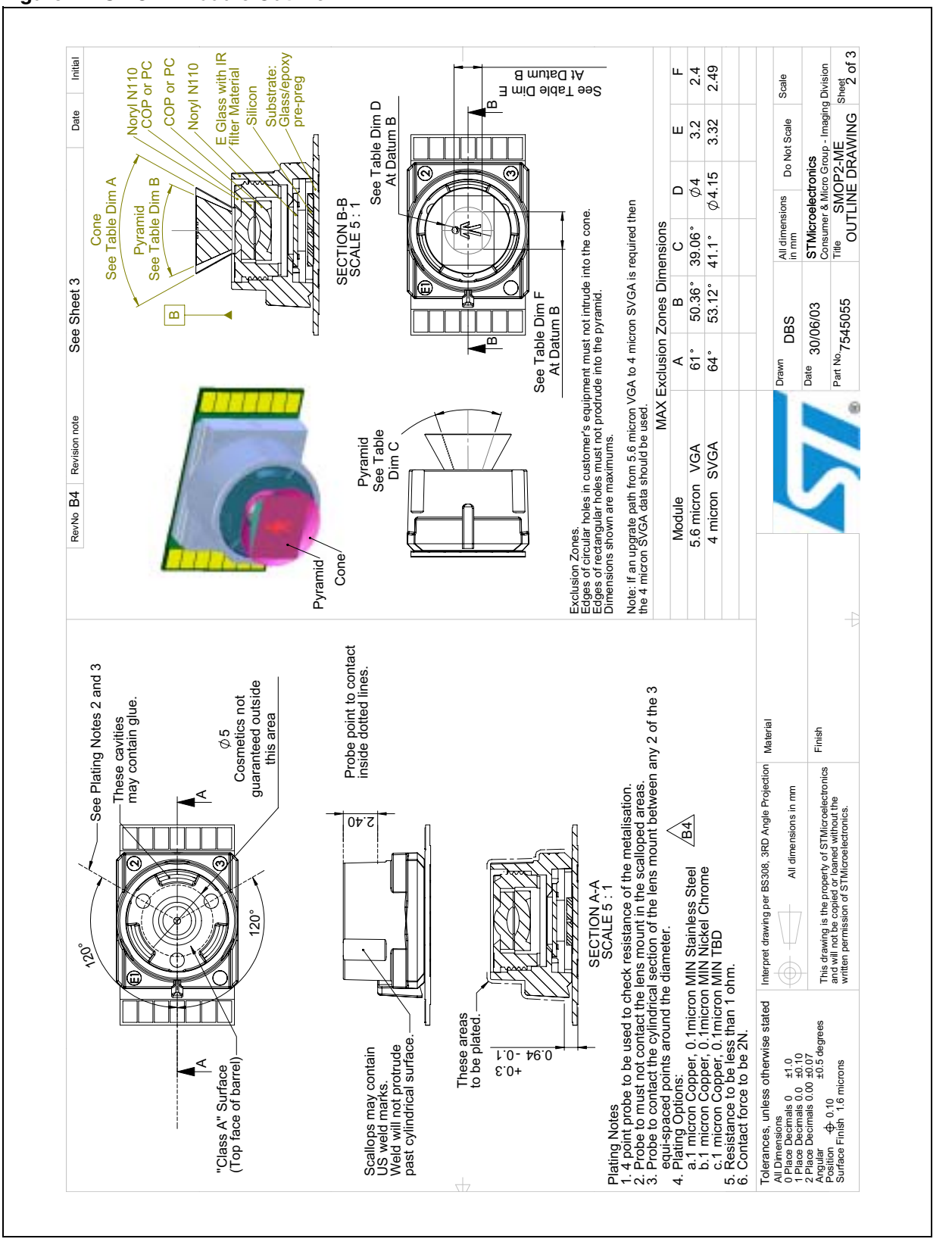
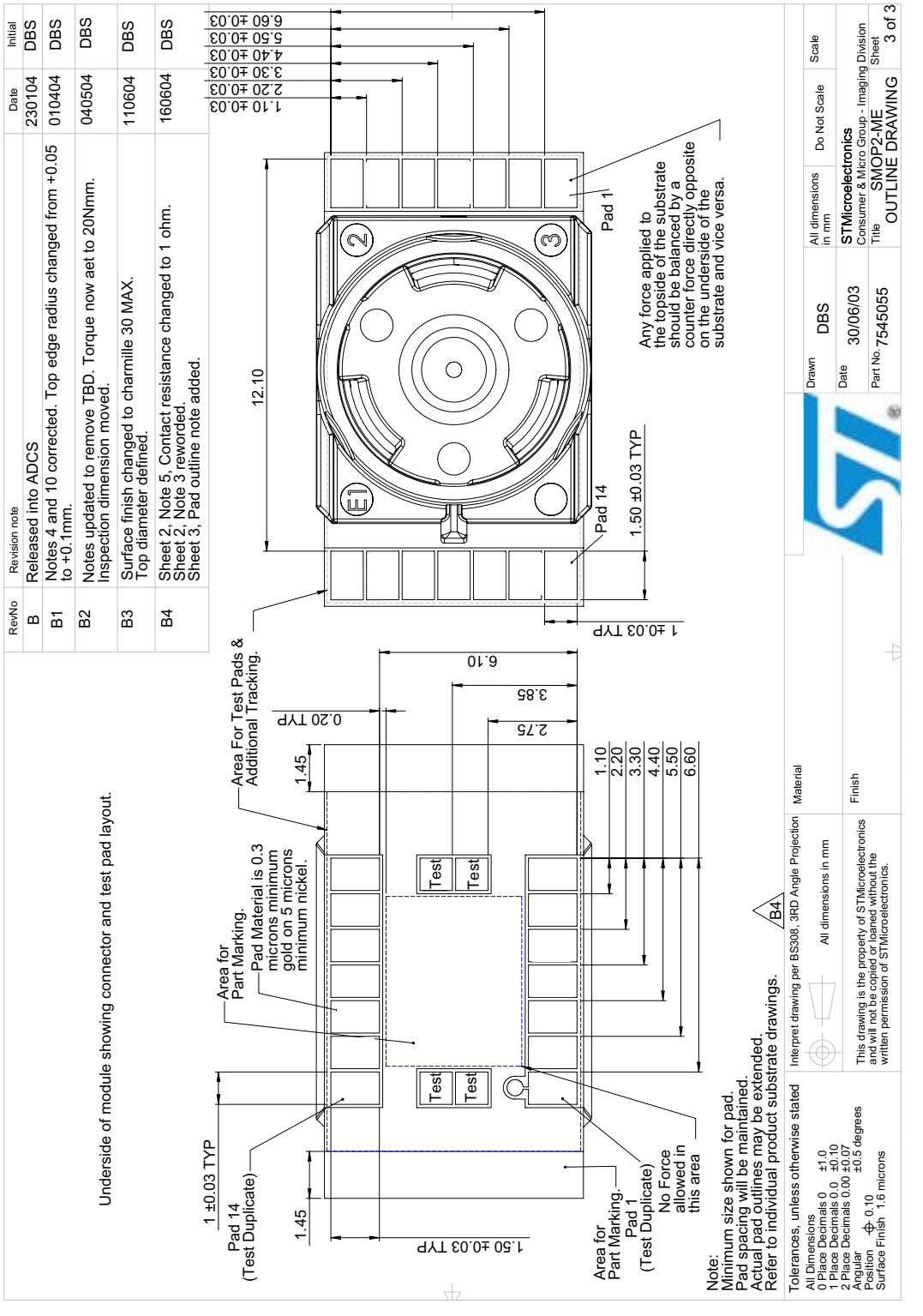


Figure 15. SmOP2 Module Outline



8 APPLICATION INFORMATION

8.1 Socket

ST has developed a low-profile socket for the SmOP 1.5 package, which is suitable for reflow soldering and manual / automatic insertion of the camera module. The socket has been designed to withstand mobile phone grade reliability tests (temperature, shocks, vibration, salt mist).

Please contact ST for details on ST P/N XS0015.

See Figure 16 for recommended PCB layout and mechanical footprint of the XS0015 socket.

8.2 EMC and Shielding

The VS6552 is a low noise device and is highly tolerant of high levels of radio frequency (RF) radiation. However if this device is closely mounted to a sensitive receiver it is recommended that the VS6552 is shielded to prevent reducing the sensitivity or channel masking of the receiver.

Recommended maximum field strength: 1kV/m.

Maximum radiated power transferred from the VS6552 into a GSM monopole antenna mounted 15 mm away from the VS6552 has peaks of interference at around -90 dBm. This is dependent on system design and layout.

To minimized the coupling between the GSM antenna and the sensor the following guide lines should be observed.

Camera should be positioned as far away from the GSM antenna as possible. The distance between the low frequency (below 1GHz) resonant antenna elements and the camera should also be maximized.

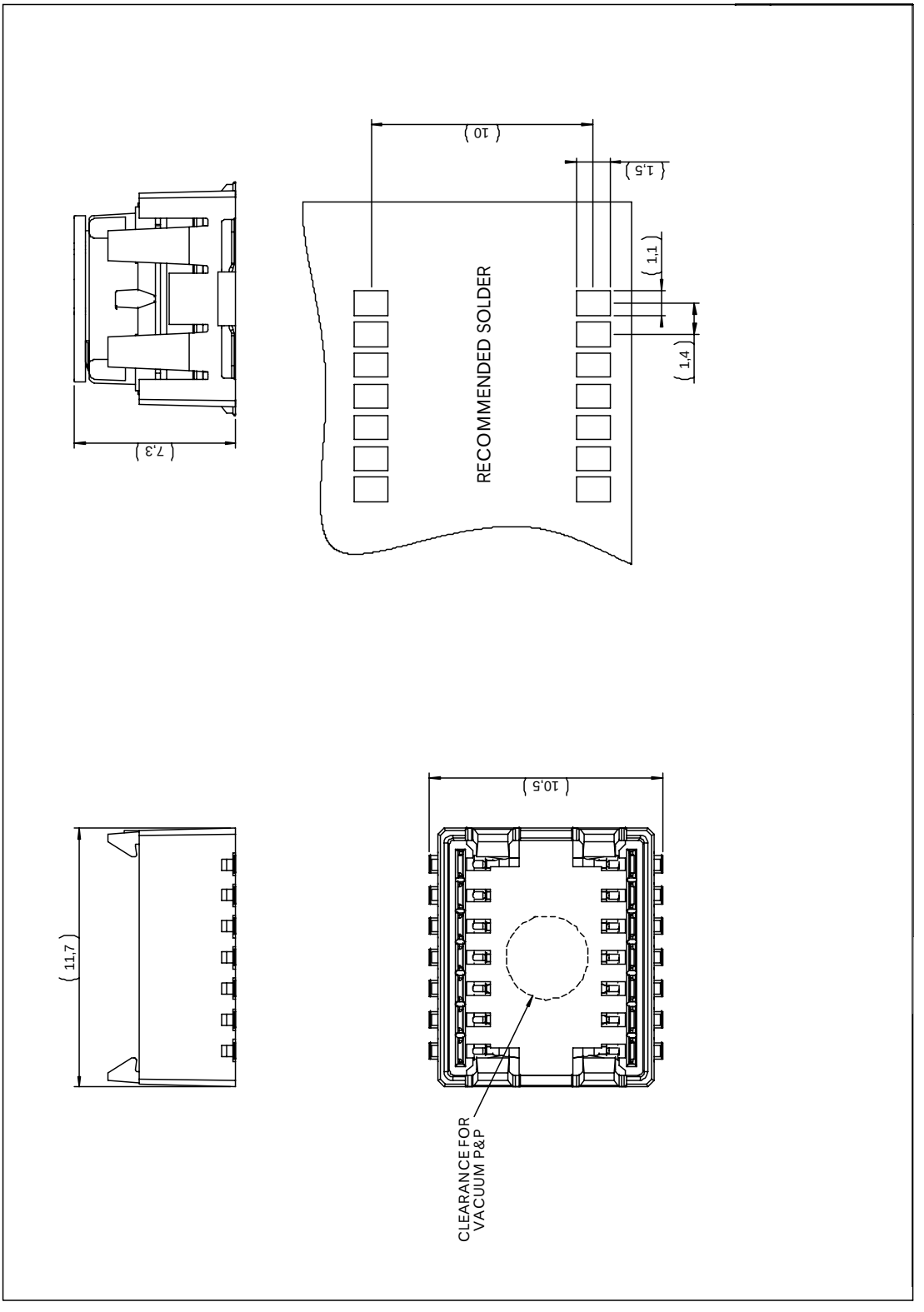
The VS6552 and its associated decoupling capacitors should NOT be connected together using the antenna reference ground. The ground connections in the sub circuit should be connected either:

- by a dedicated ground trace network, that is connected by a single point to the main ground of the system
- by an internal ground plane, which is entirely covered and single point connected to a protective ground.

The PCLKP and PCLKN lines can be filtered to reduce the induced noise.

The protective ground should be flooded around the sensor socket pads to reduce the radiation aperture in the protective ground plane.

Figure 16. SmOP1.5 Socket Mechanical Data



9 REVISION HISTORY

Table 17. Revision History

Date	Revision	Description of Changes
May 2004	1	First Release of Product Preview
21 October 2004	2	Second Release - Document status changed to datasheet. to reflect the product maturity level. Changes applied in Electrical Characteristics and Package Information with the addition of two packages (SmOP2M and SmOP2ME).