Vanguard Semiconductor

VS6606GE

65V/70A N-Channel Advanced Power MOSFET

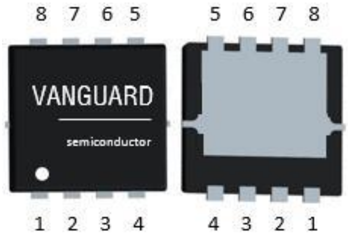
V_{DS}	65	V
$R_{DS(on),TYP}$@ V_{GS}=10V	5	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5V	8	mΩ
I_D	70	A

Features

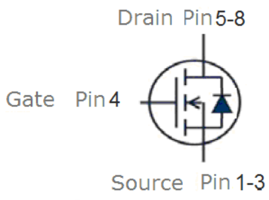
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- VitoMOS® Ⅱ Technology
- Fast Switching and High efficiency
- Pb-free lead plating; RoHS compliant; Halogen free

Pb-Free RoHS HF Halogen-Free

PDFN3333



Part ID	Package Type	Marking	Tape and reel information
VS6606GE	PDFN3333	6606GE	5000pcs/Reel



Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		65	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C =25°C	70	A
I_D	Continuous drain current @V_{GS}=10V	T_C =25°C	70	A
		T_C =100°C	44	A
I_{DM}	Pulse drain current tested ①	T_C =25°C	280	A
I_{DSM}	Continuous drain current @V_{GS}=10V	T_A=25°C	20	A
		T_A=70°C	16	A
EAS	Avalanche energy, single pulsed ②		36	mJ
PD	Maximum power dissipation	T_C =25°C	42	W
		T_C =100°C	17	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	3.6	W
		T_A=70°C	2.3	W
T_{STG},T_J	Storage and junction temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	35	°C/W

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Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	65	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=60V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃)	V_{DS}=60V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.3	1.9	2.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=20A	--	5	7	mΩ
		Tj=100℃	--	6.2	--	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=4.5V, I_D=10A	--	8	11	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	1620	1910	2200	pF
Coss	Output Capacitance		745	875	1005	pF
Crss	Reverse Transfer Capacitance		25	35	45	pF
Rg	Gate Resistance	f=1MHz	--	2.0	--	Ω
Qg (10V)	Total Gate Charge	V_{DS}=30V,I_D=20A, V_{GS}=10V	--	28	--	nC
Qg (4.5V)	Total Gate Charge		--	13	--	nC
Qgs	Gate-Source Charge		--	6	--	nC
Qgd	Gate-Drain Charge		--	3.5	--	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=30V, I_D=20A, R_G=3Ω, V_{GS}=10V	--	8.4	--	ns
Tr	Turn-on Rise Time		--	32	--	ns
Td(off)	Turn-Off Delay Time		--	22	--	ns
Tf	Turn-Off Fall Time		--	9	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=20A,V_{GS}=0V	--	0.8	1.2	V
Trr	Reverse Recovery Time	T_j=25℃,I_{sd}=20A, V_{GS}=0V di/dt=100A/μs	--	39	--	ns
Qrr	Reverse Recovery Charge		--	27	--	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 12A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{θJA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

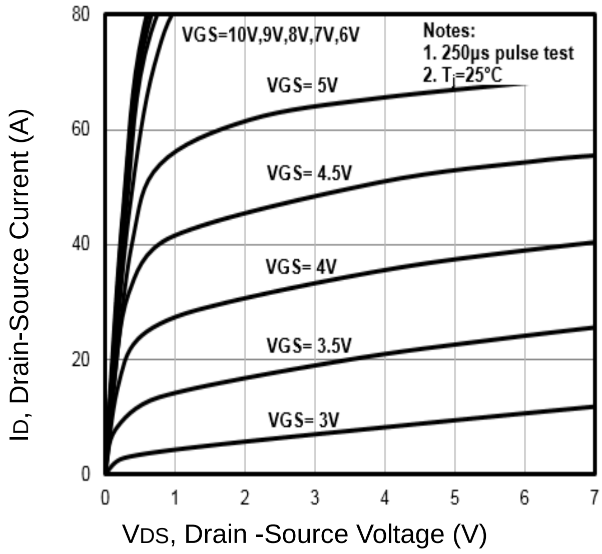

Fig1. Typical Output Characteristics

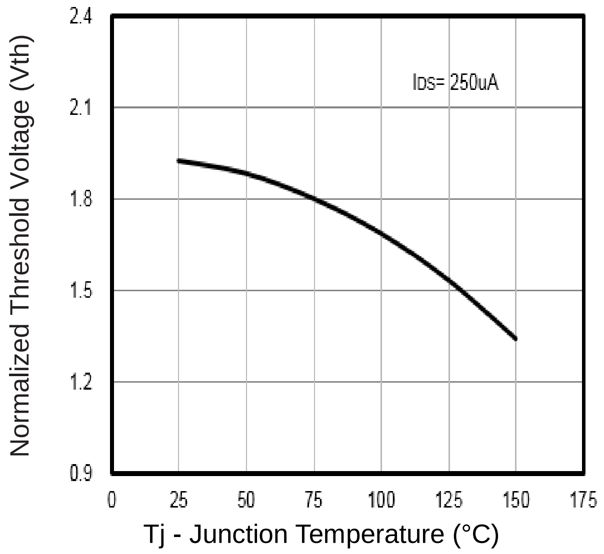

Fig2. Normalized Threshold Voltage Vs. Temperature

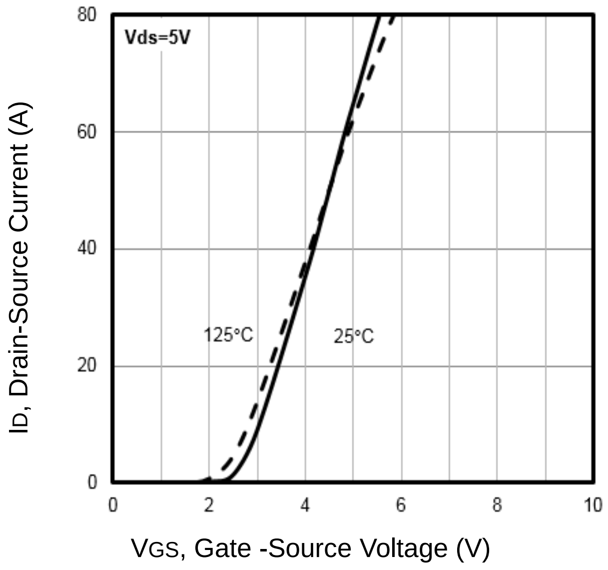

Fig3. Typical Transfer Characteristics

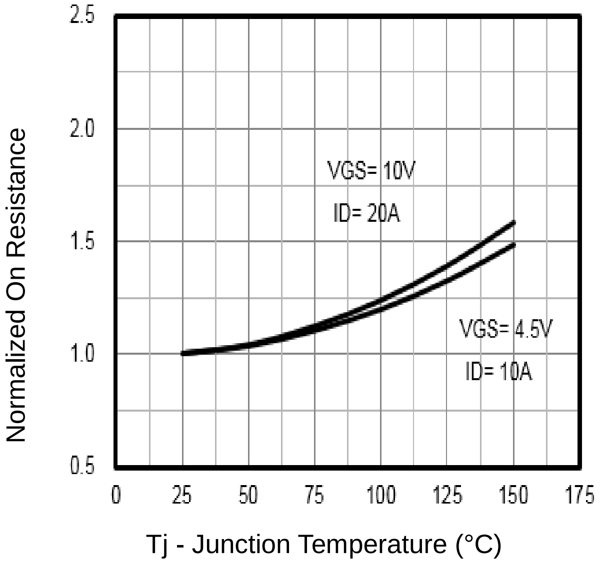

Fig4. Normalized On-Resistance Vs. Temperature

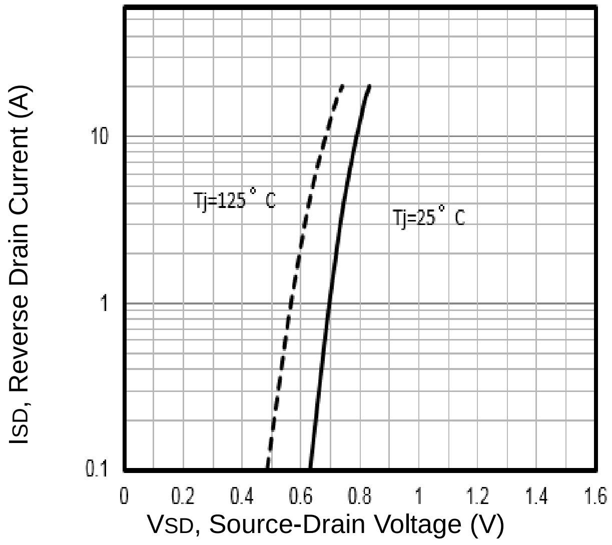

Fig5. Typical Source-Drain Diode Forward Voltage

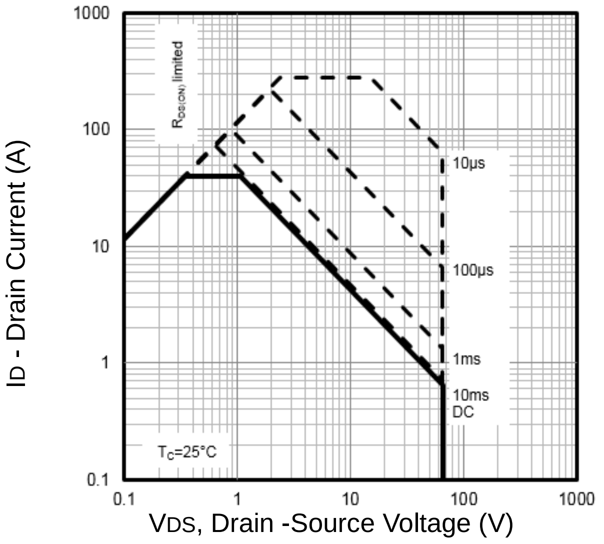

Fig6. Maximum Safe Operating Area

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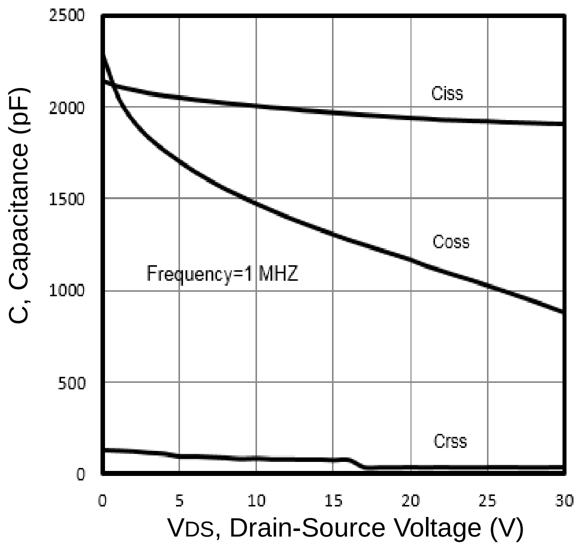
Typical Characteristics



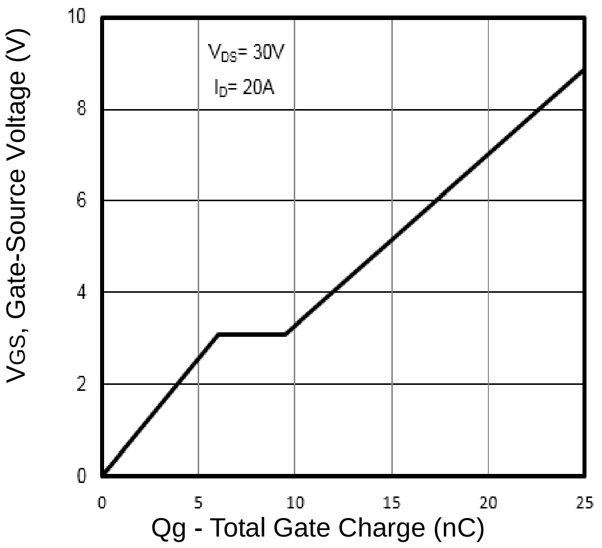


Fig7. Typical Capacitance Vs. Drain-Source Voltage

Fig8. Typical Gate Charge Vs. Gate-Source

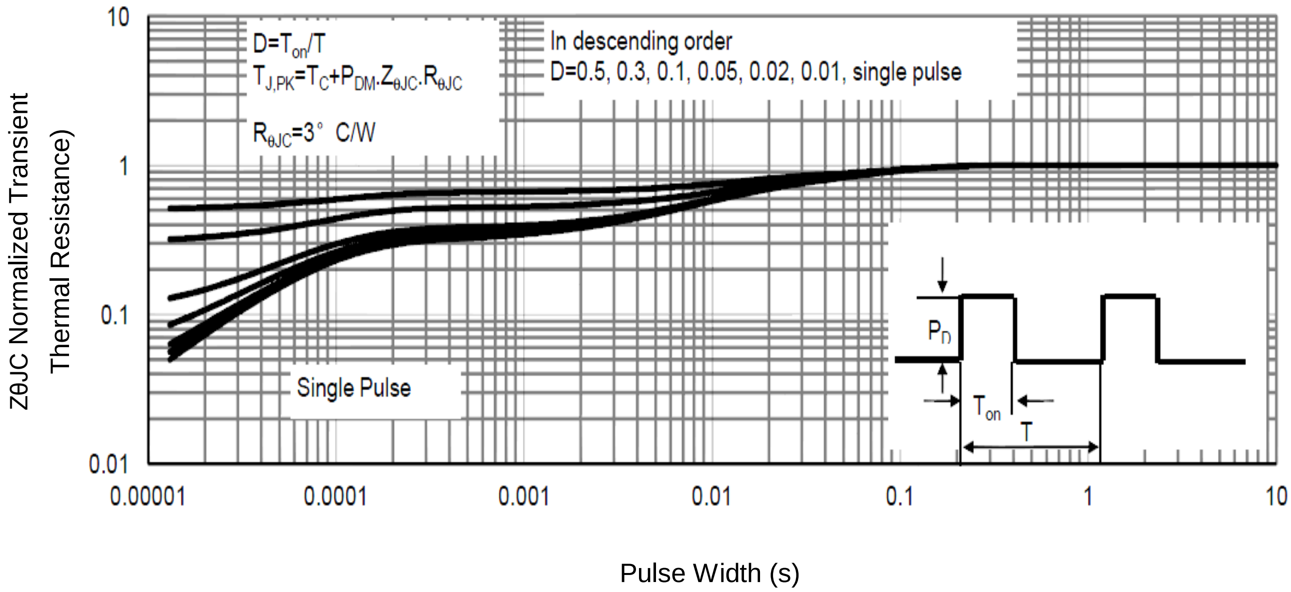
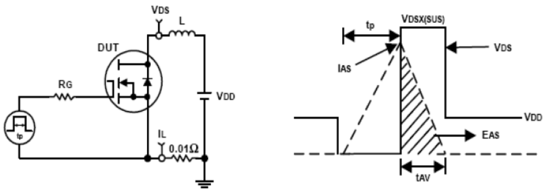


Fig9. Normalized Maximum Transient Thermal Impedance



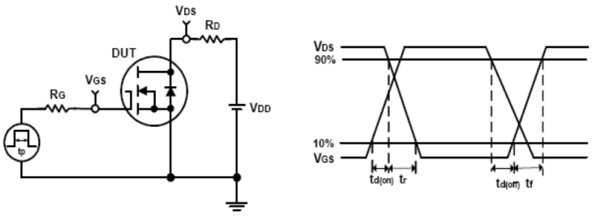
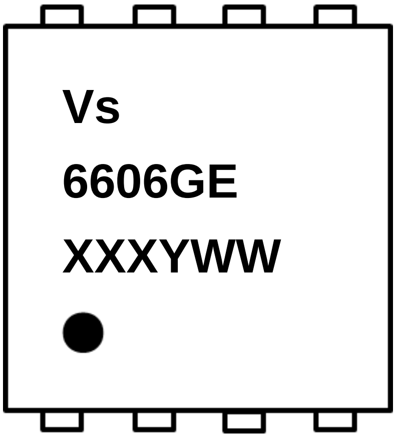


Fig10. Unclamped Inductive Test Circuit and waveforms

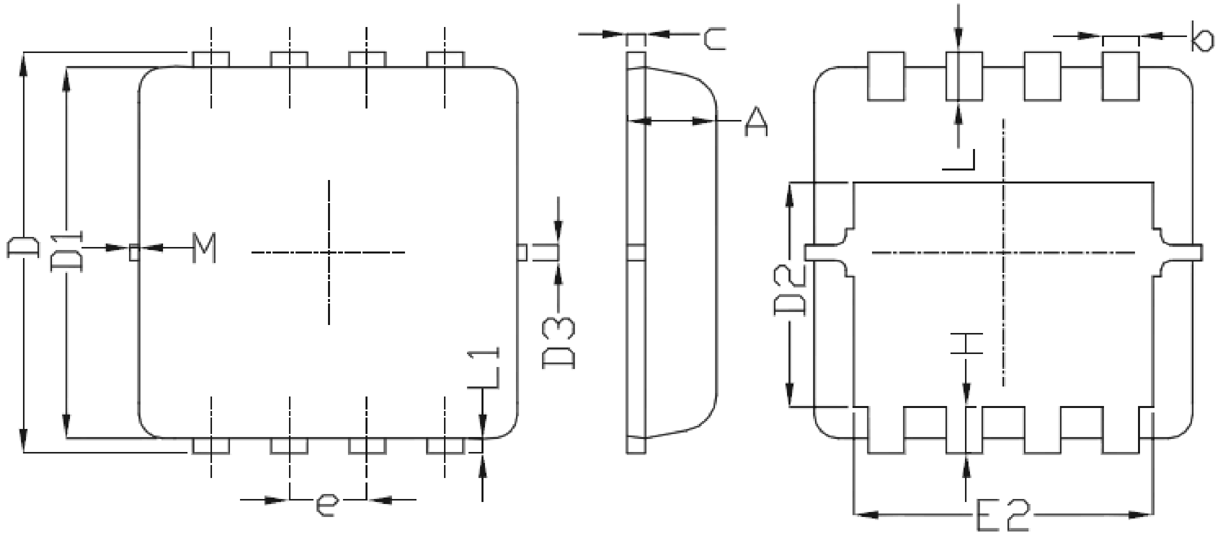
Fig11. Switching Time Test Circuit and waveforms

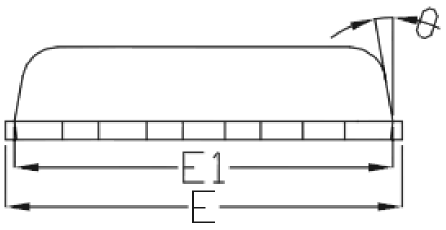
Marking Information

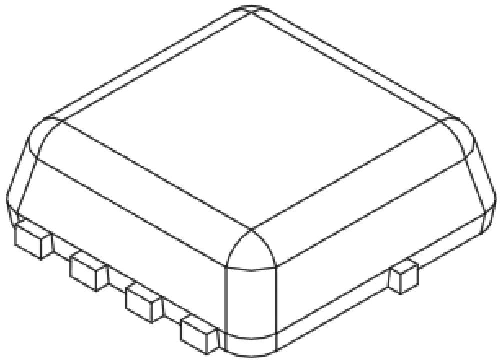


1st line：Vanguard Code（Vs）
2nd line：Part Number（6606GE）
3rd line：Date code （XXXYWW）
  XXX：Wafer Lot Number Code , code changed with Lot Number
  Y：Year Code (e.g. E=2017, F=2018, G=2019, H=2020, etc)
  WW：Week Code (01 to 53)

PDFN3333 Package Outline Data







Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.7	0.75	0.8
b	0.25	0.3	0.35
C	0.1	0.15	0.25
D	3.25	3.35	3.45
D1	3	3.1	3.2
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.2	3.3	3.4
E1	3	3.15	3.2
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.3	0.39	0.5
L	0.3	0.4	0.5
L1	--	0.13	--
θ	--	10°	12°
M	*	*	0.15

* Not specified

Notes:

1. Follow JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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