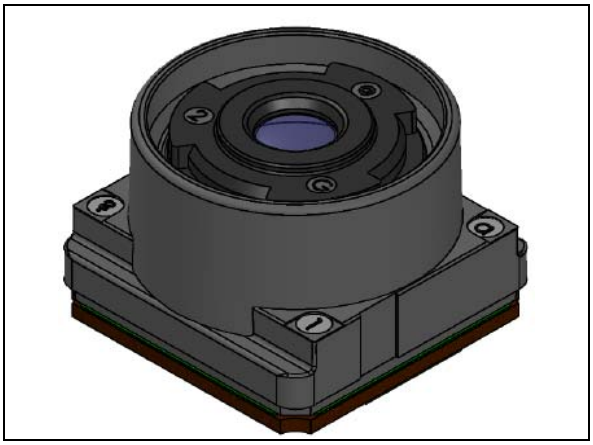
VS6955CA

5.0 megapixel fixed-focus camera module

Datasheet - production data



Features

- 5.0 megapixel resolution sensor (2600 x 1952) inclusive of 4 border pixels each sides
- SMIA Profile 1 compliant
- compact size 6.5 mm x 6.5 mm x 4.6 mm
- MIPI CSI-2 single lane interface (up to 1Gbps)
- CCI command interface, supports up to 400 kHz
- 2.8V analog and 1.8V digital operation
- supports 2 x 2 and 4 x 4 pixel binning
- integrated 8-kbit OTP memory
- ultra low power standby mode
- on board couplet correction
- Flex compatible

Description

The VS6955CA is a high performance 5.0 megapixel fixed-focus camera module. It is designed for use across a range of mobile phone handsets and accessories. The sensor supports high quality still camera functions as well as video modes.

The VS6955CA is compliant with the MIPI CSI-2 specification. It is capable of generating raw Bayer 5.0 megapixel images up to 23 fps with a single CSI-2 lane. The VS6955CA offers an ultra low power consumption hardware standby mode.

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VS6955CAQ05I/1	SMIA65	Tape and reel

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1 Overview

The VS6955CA image sensor produces raw digital video data at up to 23 frames per second. The sensor supports horizontal flip and vertical mirroring. Output frequency can be derated as defined in the specification for power saving. Higher frame rate can be achieved through analog binning and subsampling modes.

The image data is digitized using an internal 10-bit column ADC. The resulting pixel data is output together with checksums and embedded codes for synchronization. The interface conforms to MIPI CSI-2 interface standards.

The sensor is fully configurable through a CCI serial interface. Both the CSI-2 and CCI interfaces are specified in a separate document: *MIPI alliance standard for camera serial interface 2 (CSI-2)*.

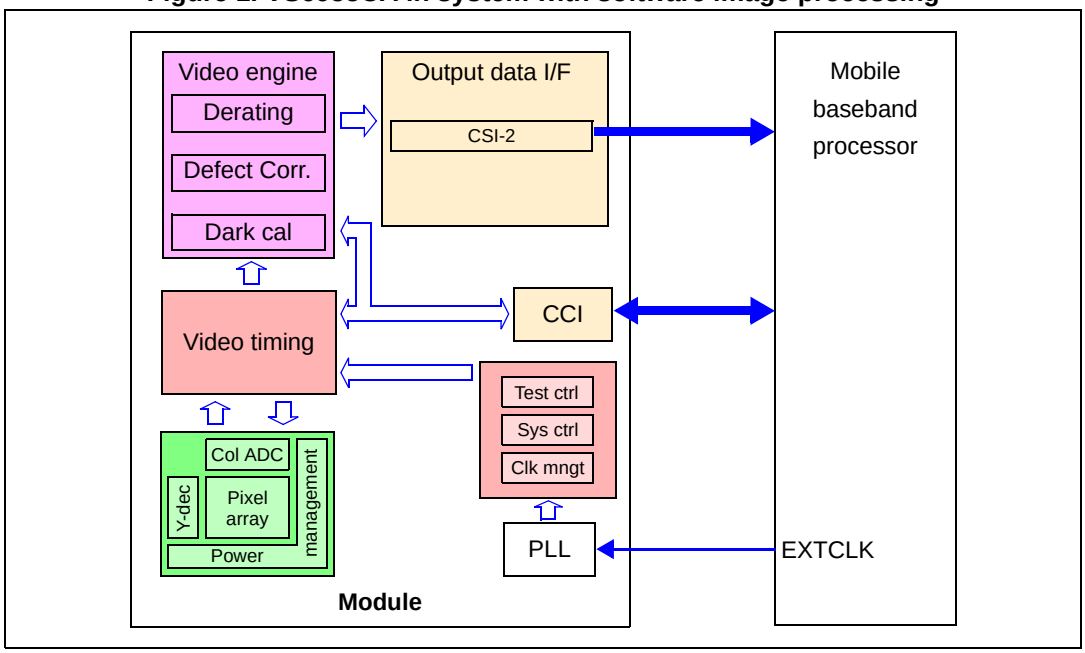
Table 2. Technical specification

Feature	Detail
Pixel resolution	2600 x 1952 with border pixels
Sensor technology	ST IMG140 FSI Gen2 based CMOS imaging process
Pixel size	1.4 µm x 1.4 µm
Analog gain	+ 24 dB
Digital gain	+ 6 dB
Dynamic range	60 dB
Signal to noise	36 dB (@ 100 lux)
Supply voltages	Analog: 2.6 to 2.9V Digital: 1.7 to 1.9 V
Typical power consumption 15 fps	100 mA (typical)
Operating temperature	-30°C to +70°C
Storage temperature	-40°C to +85°C
Average dark current (60C)	25 e/s
Shading (60C)	12 e/s

VS6955CA interface

The VS6955CA image sensor can be directly connected to a baseband or multimedia processor. The image processing is done in software or hardware within the baseband processor.

Figure 1. VS6955CA in system with software image processing



2 Module specification

Figure 2 shows the position of the pins on the module and *Table 3* provides the signal descriptions.

Figure 2. VS6955CA module pinout (viewed from bottom of camera module)

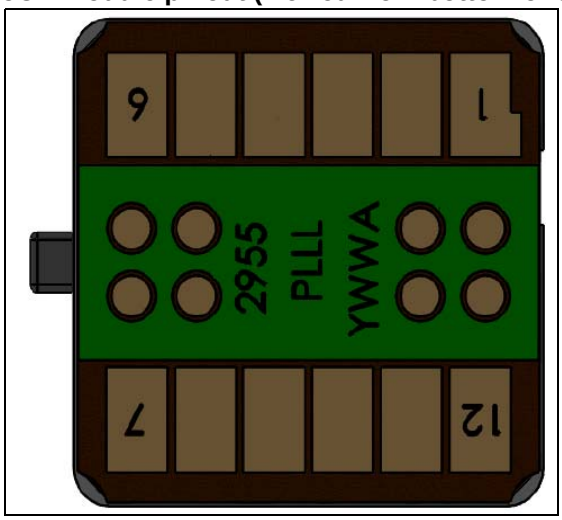


Table 3. Pin description

Pad number	Pad name	I/O type	Description
Power supplies			
1	GND	PWR	Ground (combined)
7	GND	PWR	Ground (combined)
2	VANA	PWR	Analog power
10	VDIG	PWR	Digital power
System			
3	XSHUTDOWN	I	Power down control(1)
4	EXTCLK	I	System clock input
Control			
5	SCL	I	Serial communication clock
6	SDA	I/O	Serial communication data
Data			
8	CLK-	SubLVDS output	Output qualifying clock
9	CLK+	SubLVDS output	Output qualifying clock
11	DATA-	SubLVDS output	Serial output data
12	DATA+	SubLVDS output	Serial output data
ST test			
TP		ST test pins	Do not connect(2)

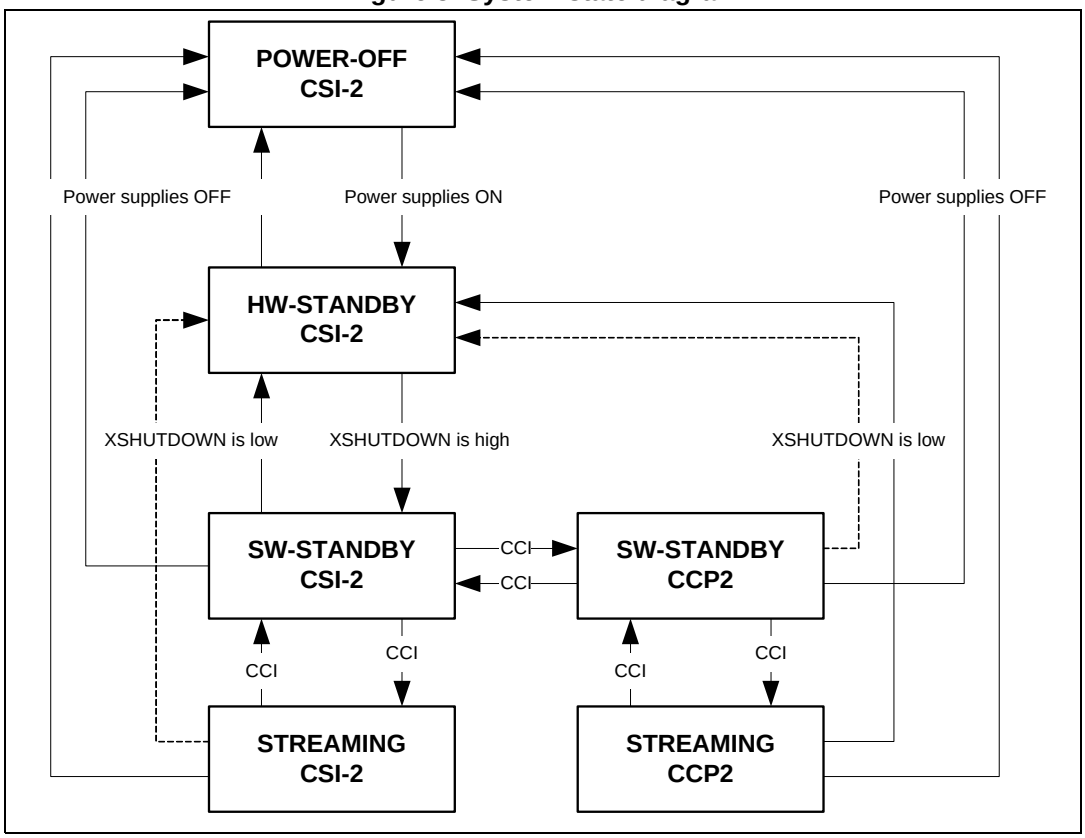
1. Signal is active low.
2. Test pins are not floating.

3 Functional description

3.1 Device operating modes

The mode changes in VS6955CA are shown in *Figure 3*. Further details are provided in *Section 3.2.1* to *Section 3.2*.

Figure 3. System state diagram



3.1.1 Power off

The power off state is defined as either or both of the digital and analog supplies not present.

3.1.2 Hardware standby

This is the lowest power consumption mode. CCI communications are not supported in this mode. The PLL and the video blocks are powered down. This state is entered by pulling the control pin XSHUTDOWN down (active low). All registers are returned to their default values

3.1.3 Software standby

Software standby mode preserves the contents of the CCI register map. CCI communications are supported in this mode. The software standby mode is selected using a serial interface command. If this state is entered from hardware standby, the data pads

remain at LP-00. If this state is entered from streaming then the data pads go to LP-11 at the end of the current frame. The internal video timing is reset to the start of a video frame in preparation for the enabling of active video. The values of the serial interface registers such as exposure and gain are preserved. The system clock must remain active when communicating with the sensor.

This state is entered by releasing the device from hard reset by writing 0x00 to the mode control register (0x0100) or commanding a soft reset by writing 0x01 to the software reset register (0x0103).

Note: After a soft reset or the transition of XSHUTDOWN to high, all registers are returned to their default values.

3.1.4 Streaming

The VS6955CA streams live video. This mode is entered by writing 0x01 to the mode control register (0x0100).

3.2 Power management

3.2.1 Power-up procedure

The digital and analog supply voltages can be powered up in any order, for example, VDIG then VANA or VANA then VDIG.

On power-up the on-chip power-on reset cell ensures that the CCI register values are initialized correctly to their default values.

The EXTCLK clock can either be initially low and then enabled during software standby mode or EXTCLK can be a free running clock.

The power-up sequence timing constraints are shown in *Table 4*.

Table 4. Power-up sequence timing constraints

Symbol	Parameter	Min.	Max.	Units
t0	VANA rising – VDIG rising	VANA and VDIG may rise in any order. The rising separation can vary from 0 ns to indefinite.		ns
t1	VDIG rising – VANA rising			ns
t2	VDIG / VANA rising – XSHUTDOWN rising	XSHUTDOWN must rise later than or coincident with the later rising supply (VDIG or VANA)		µs
t3	XSHUTDOWN – First I^2C transaction	28,500		EXTCLK cycles
t4	Minimum number of EXTCLK cycles prior to the first I^2C transaction	28,500		EXTCLK cycles
t5	PLL start up/lock time	-	1	ms
t6	Entering streaming mode – First frame start sequence (fixed part)	-	10	ms
t7	Entering streaming mode – First frame start sequence (variable part) = Integration time	fine_integration_time_min		

Figure 4. VS6955CA power-up sequence for CCP2

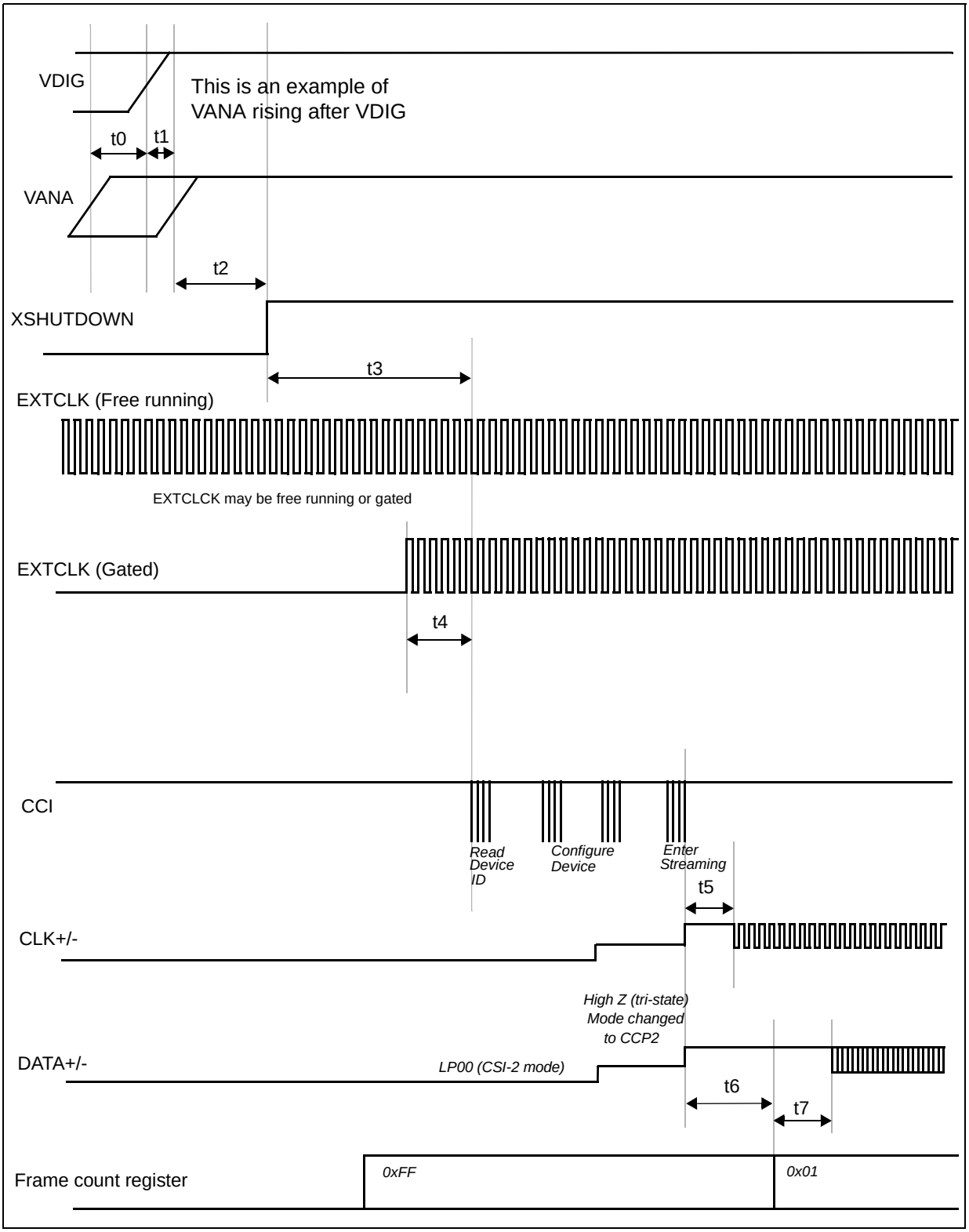
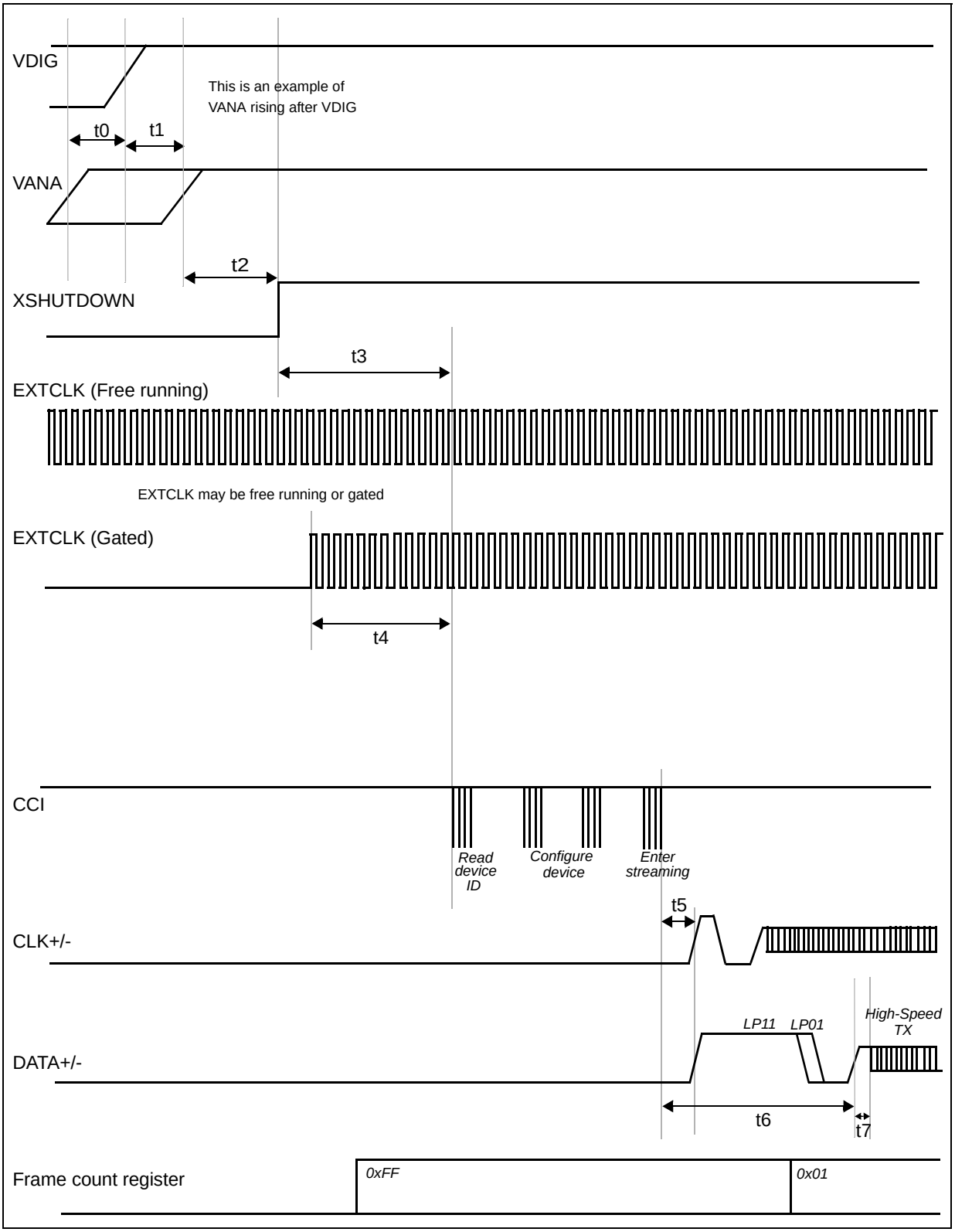


Figure 5. VS6955CA power-up sequence for CSI-2 mode



3.2.2 Power-down procedure

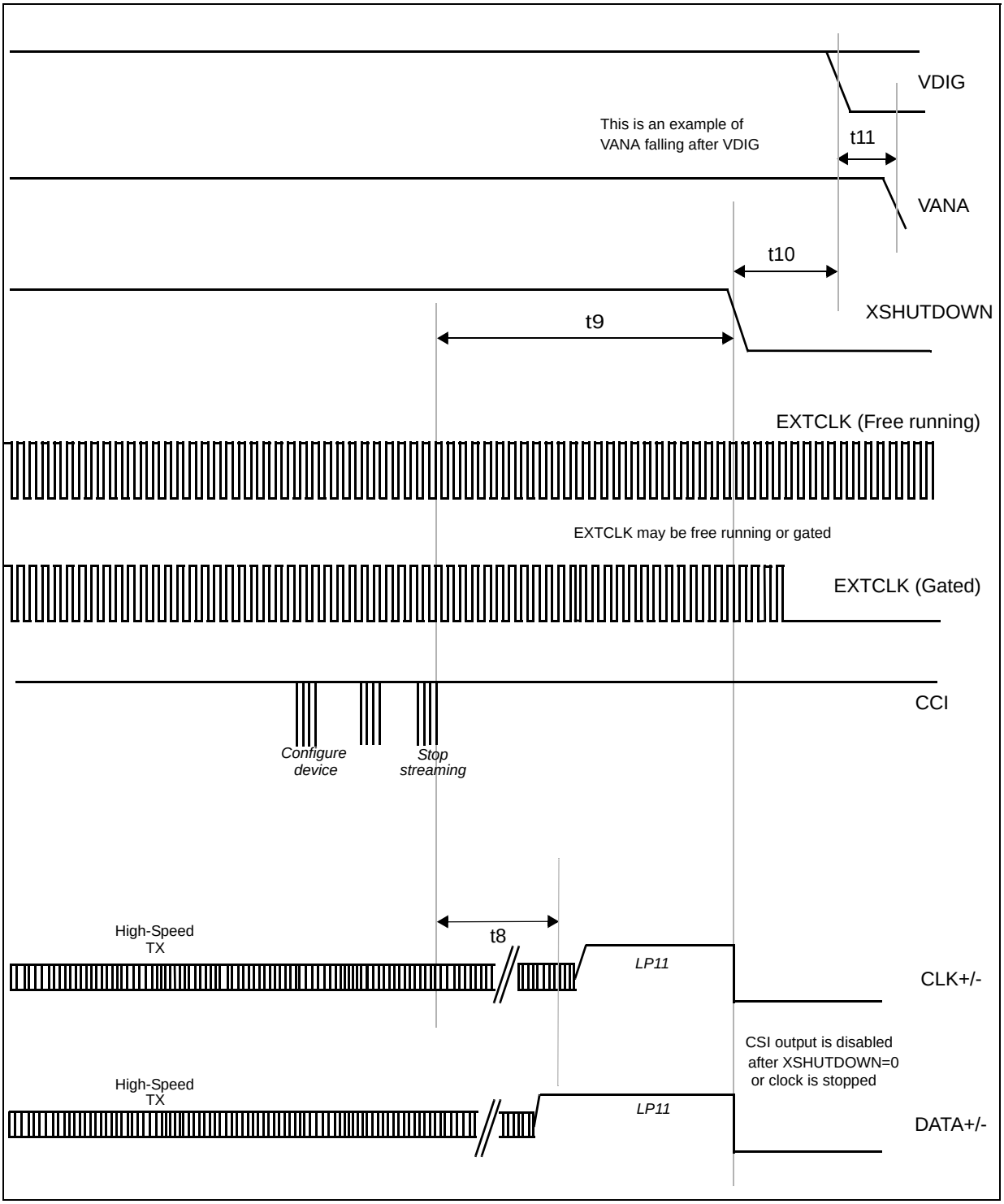
The power-down sequence timing constraints are shown in *Table 5*.

Table 5. Power-down sequence timing constraints for CSI2 communications

Symbol	Parameter	Min.	Max.	Units
t8	Last I^2C transaction to software standby(1)	-	1 frame	
t9	Last I^2C transaction or MIPI frame end to XSHUTDOWN falling	512	-	clock cycles
t10	XSHUTDOWN to VANA/VDIG falling	XSHUTDOWN must fall at the same time as, or earlier than, both power supplies (VDIG and VANA)		
t11	VANA to VDIG or VDIG to VANA falling	VANA and VDIG may fall in any order, the rising separation can vary from 0 ns to indefinite		

1. If fast standby is enabled, then the power down sequence will not wait for the frame to end.

Figure 6. VS6955CA power-down sequence for CSI-2 mode

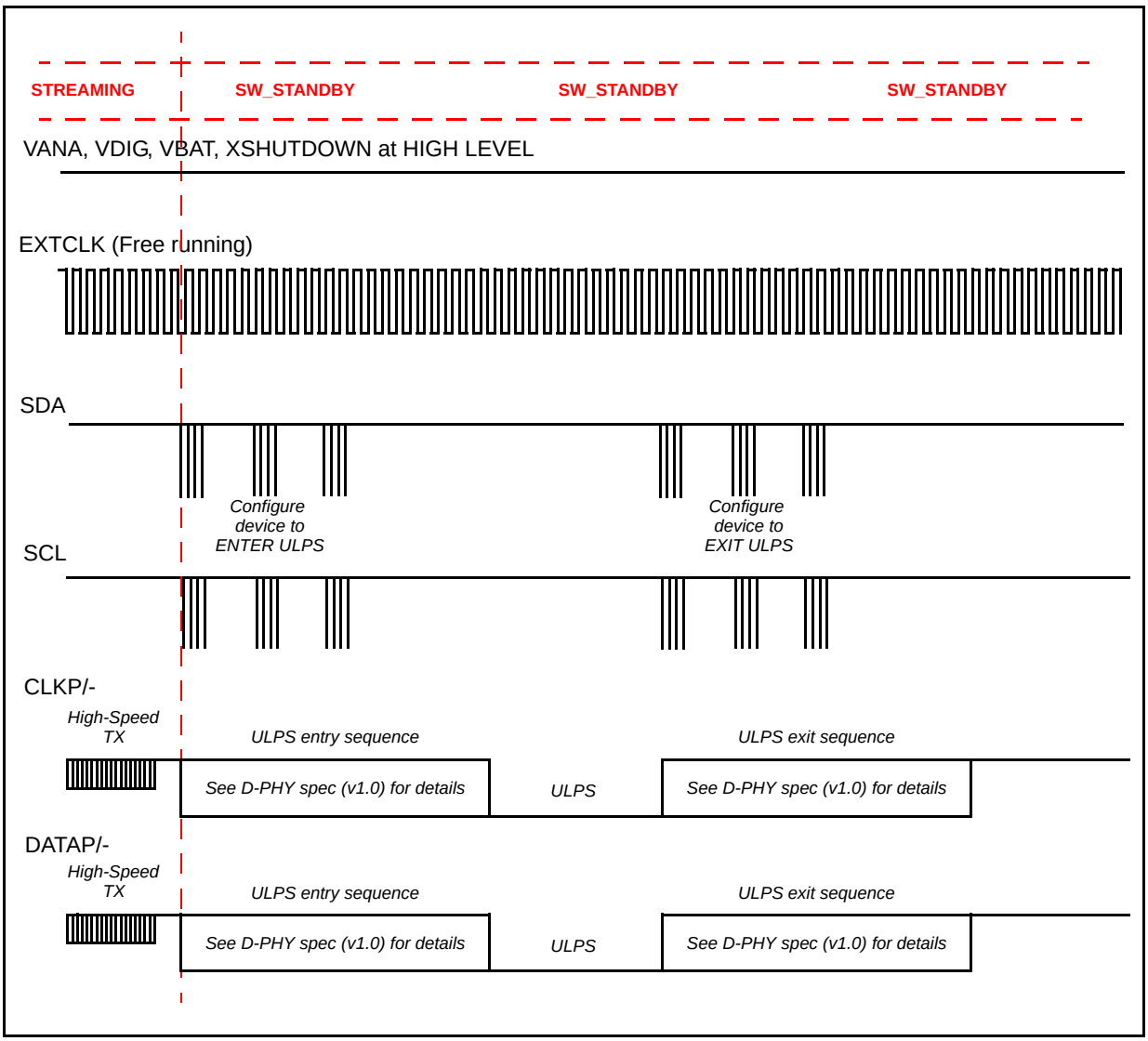


3.3 Ultra low power mode option (only for CSI-2)

It is possible to reduce the power consumption of the system while the camera is not being used while allowing it to be restarted at any time with a short time to streaming mode. This can be achieved using the ultra low power standby (ULPS) mode.

ULPS mode can be entered and exited from software standby only. To enter ULPS, the user needs to write to the sensor a specific list of settings through CCI. ST will provide the list of CCI commands to enter or exit ULPS upon demand.

Figure 7. ULPS sequence for CSI-2 mode



3.4 Internal power-on reset (POR)

The VS6955CA internally performs a power-on reset (POR) when the 1V2 VDD digital supply rises through the trigger level, Vtrig_rising. Similarly, if the 1V2 VDD digital power supply falls through the trigger level, Vtrig_falling, then the power-on reset also triggers.

Definitions

Rise threshold voltage (VTRIGR)	This is the supply voltage level that is recognized by the POR as voltage “HIGH”. Only after the supply reaches this level does the output of POR change to high level if it is off, after a specified amount of delay.
Fall threshold voltage (VTRIGF)	This is the supply voltage level that is recognized by the POR as voltage “LOW”. Only after the supply reaches this level does the output of POR change to low (ground) level if it is on.
Burst width (pw)	Burst is the negative pulse riding the supply signal. The burst width is measured as the amount of duration for which the supply signal dropped beyond the threshold levels.
Delay duration (TPOR)	Delay duration is defined as the time duration for which POR stays off before re-powering. Each reset of POR imparts a specified delay duration before POR re-powers.

Figure 8. POR timing

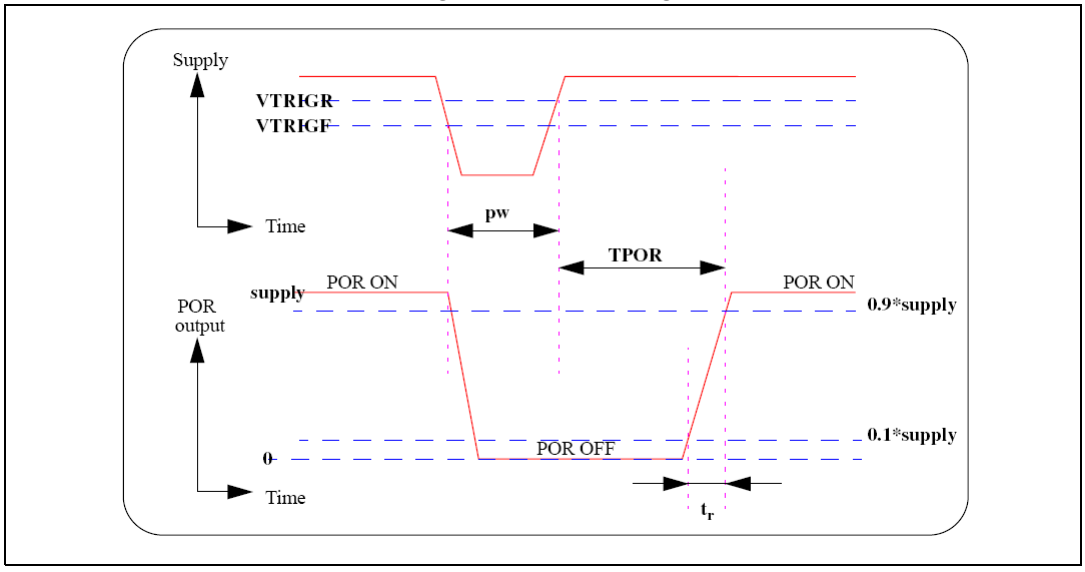


Table 6. POR cell characteristics

Symbol	Constraint	Minimum	Typical	Maximum	Units
VTRIGR	POR rise voltage detection			0.95	V
VTRIGF	POR fall voltage detection	0.4			V
Tburst (pw)	Burst filter		2	8	µs
Tpor	Delay duration		20	45	µs

3.5 External clock

3.5.1 PLL and clock input

The VS6955CA has an embedded PLL block. This block generates all necessary internal clocks from an input range defined in *Table 7*.

Table 7. System input clock frequency range

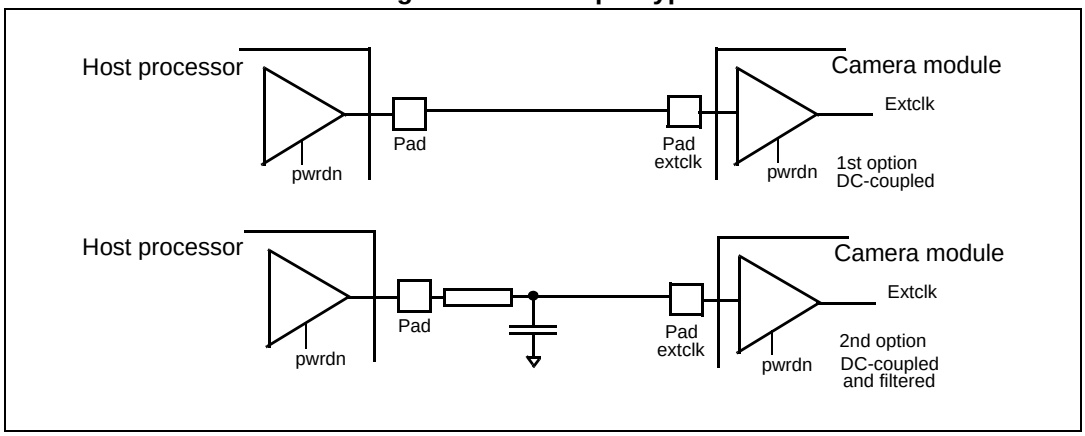
Minimum (MHz)	Maximum (MHz)
6	27

The value of the external clock frequency must be written to the register 0x0136 (extclk_frequency_mhz).

3.5.2 Clock input type

The external clock provided by the host to the VS6955CA must be a DC coupled square wave and may also be RC-filtered.

Figure 9. Clock input types



3.6 Control and video interface formats

Image data is transferred from the VS6955CA using a high speed subLVDS serial link.The serial control data is transferred to and from the VS6955CA using a CCI bus.

3.6.1 CCP/CSI-2 serial data link

Data signals (DATA+ and DATA-) and clock signals (CLK+ and CLK-) are transferred from VS6955CA using two pairs of balanced 100 Ω impedance transmission lines.

The transmission line pairs and custom transmitters/receivers realize a very low voltage differential (subLVDS) signalling scheme that can transfer information in a potentially noisy environment.

For the CCP link or CSI-2 single lane interface, the VS6955CA supports the transmission of raw Bayer data at 5.0 Mpixel resolution up to 23 fps in RAW8 or 10-8 bit format.

3.6.2 CCI serial control bus

The internal registers in VS6955CA can be configured by a master device via a CCI bus (SDA, SCL). VS6955CA sends and receives commands over this bus at up to 400 Kbits/s.

4 Camera control interface (CCI)

This chapter specifies the camera control interface (CCI). The I^2C-type interface uses 1.8 V I/O with two signals: serial data line (SDA) and serial clock line (SCL). CCI is used for control data transfer. Clock signal (SCL) generation is performed by the master device (the camera module is a slave device). The master device initiates data transfer. The CCI bus on the camera module has a maximum speed of 400 Kbits/s and has a software switchable device address. The default device address is 0x20.

Any internal register that can be written to, can also be read from. There are also read only registers that contain device status information, for example, design revision details. A read instruction from an unused register location returns the value 0x00. A read instruction from a reserved address may return any value. A write instruction to a reserved or unused register location is illegal and the effect of such a write is undefined. It is the responsibility of the host system to only write to register locations which have been defined.

4.1 Valid register data types

The contents of the registers can represent a number of different data types (see *Table 8*). The register map uses this coding to help with the interpretation of the contents of each register.

Table 8. Valid register data types

Data type	Name	Range	Description
8UI	8-bit unsigned integer	0 to 255	-
8SI	8-bit signed integer	-128 to 127	Two’s complement notation
16UI	16-bit unsigned integer	0 to 65535	-
16SI	16-bit signed integer	-32768 to 32767	Two’s complement notation
16UR	16-bit unsigned iReal	0 to 255.99609375	08.08 fixed point number. 8 integer bits (MS Byte), 8 fractional bits (LS Byte)
16SR	16-bit signed iReal	-128 to 127.9960375	Two’s complement notation, 8 fractional bits
32UR	32-bit unsigned iReal	0 to 65535.99998474	16.16 fixed point number. 16 integer bits (MS 2 Bytes), 16 fractional bits (LS 2 Bytes)
32SF	32-bit IEEE floating-point number	As per IEEE 754	As per IEEE 754. 1 sign bit, 8 exponent bits, 23 fractional bits
8C or 16C	8-bit or 16-bit coded	-	This indicates that the value is decoded to select one of several functions or modes.
8B or 16B	8 or 16 bits	-b	Each bit represents a specific function or mode.

4.2 Register default values

The registers default values are expressed as hexadecimal numbers.

4.2.1 Status registers [0x0000 to 0x001F]

Table 9. Status registers [0x0000 to 0x001F]

Index	Byte	Register name	Data type	Default	Type	Comment
0000	Hi	module_model_id	16UI	0B	RO	2955 Camera model identification number. Default values depend on NVM content.
0001	Lo			8B		
0002		revision_number_major	8UI	00	RO	Revision identifier of the camera for DCC change.
0003		manufacturer_id	8UI	01	RO	Module manufacturer number. Default value depends on NVM content.
0004		smia_version	8UI	0A	RO	SMIA version that sensor complies with 10 - Version 1.0
0005		frame_count	8UI	FF	RW	Frame count register. Increments from 1 to 254 when streaming. Reports 255 when idle.
0006		pixel_order	8UI	00	RO	Color pixel readout order. Changes with mirror and flip (register 0x0101). 0x00 - GR/BG normal. 0x01 - RG/GB horizontal mirror. 0x02 - BG/GR vertical flip. 0x03 - GB/RG vertical flip and horizontal mirror.
0008	Hi	data_pedestal	16UI	00	RO	Offset applied to the video data.
0009	Lo			40		
000C		pixel_depth	8UI	0A	RO	Pixel depth resolution of the sensor.
0010		revision_number_minor	8UI	00	RO	Revision identifier of the camera for minor changes. Default value depends on NVM content. 1: TS 2: ES 3: CS 4: MP
0011		additional_spec_ver	8UI	08	RO	Additional specification identifier.
0012		module_date_year	8UI	00	RO	Last digit of manufacturing year. Default value depends on NVM content.

Table 9. Status registers [0x0000 to 0x001F] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0013		module_date_month	8UI	00	RO	Manufacturing month. Default value depends on NVM content.
0014		module_date_day	8UI	00	RO	Manufacturing day. Default value depends on NVM content.
0015		module_date_phase	8UI	01	RO	Manufacturing phase identification. Default value depends on NVM content.
0016		sensor_model_id	16UI	03	RO	Silicon identification number. This may not be the same as the module identification number, for example, in the case where the same silicon is used in two different modules.
0017				BB		
0018		sensor_nvm_revision_id	8UI	00	RO	Bits 3:0 Silicon NVM revision number. Default value depends on NVM content.
		sensor_mask_set_revision_id		01	RO	Bits 7:4 Silicon mask revision code.
0019		sensor_manufacturer_id	8UI	01	RO	Silicon manufacturer number - ST Microelectronics.
001A		sensor_firmware_version	8UI	11	RO	Silicon firmware version with format “[7:4].[3:0]”, for example 0x11 = “1.1”.
001C	Hi	serial_number	32UI	00	RO	Sequential number starting at 0 and incrementing by 1. Specification identifier. Default value depends on NVM content.
001D	3rd			00		
001E	2nd			00		
001F	Lo			00		

4.2.2 Frame format description registers [0x0040 to 0x0049]

For a full description of the frame format description refer to *Section 6.1: Frame format on page 49*.

Table 10. Frame format description registers [0x0040 to 0x0049]

Index	Byte	Register name	Data type	Default	Type	Comment
0040		frame_format_model_type	8UI	01	RO	Generic frame format.
0041		frame_format_model_ subtype	8UI	22	RO	Contains the number of 2-byte data format descriptors used. The upper nibble defines the number of column descriptors. The lower nibble defines the number of row descriptors.
0042	Hi	frame_format_descriptor_0_ req	16UI	5A	RO	number of visible columns.
0043	Lo			28		
0044	Hi	frame_format_descriptor_1	16UI	20	RO	8 dummy columns.
0045	Lo			08		
0046	Hi	frame_format_descriptor_2	16UI	10	RO	3 embedded rows (SOF).
0047	Lo			03		
0048	Hi	frame_format_descriptor_3_ req	16UI	57	RO	number of visible rows
0049	Lo			A0		

4.2.3 Analogue gain description registers [0x0080 to 0x0093]

For a full description of the analogue gain description registers refer to *Section 7.5.1: Analogue gain model on page 66*.

Table 11. Analogue gain description [0x0080 to 0x0093]

Index	Byte	Register name	Data type	Default	Type	Comment
0080	Hi	analogue_gain_capability	16UI	00	RO	Analogue gain capability - single global gain only.
0081	Lo			00		
0084	Hi	analogue_gain_code_min	16UI	00	RO	Minimum recommended analogue gain code.
0085	Lo			00		
0086	Hi	analogue_gain_code_max	16UI	00	RO	Maximum recommended analogue gain code.
0087	Lo			F0		
0088	Hi	analogue_gain_code_step	16UI	00	RO	Analogue gain code step size.
0089	Lo			10		
008A	Hi	analogue_gain_type	16UI	00	RO	Analogue gain type.
008B	Lo			00		
008C	Hi	analogue_gain_m0	16UI	00	RO	Analogue gain constant M0.
008D	Lo			00		
008E	Hi	analogue_gain_c0	16UI	01	RO	Analogue gain constant C0.
008F	Lo			00		
0090	Hi	analogue_gain_m1	16UI	FF	RO	Analogue gain constant M1.
0091	Lo			FF		
0092	Hi	analogue_gain_c1	16UI	01	RO	Analogue gain constant C1.
0093	Lo			00		

4.2.4 Data format description registers [0x00C0 to 0x00C9]

Table 12. Data format description registers [0x00C0 to 0x00C9]

Index	Byte	Register name	Data type	Default	Type	Comment
00C0		data_format_model_type	8UI	01	RO	2-byte generic data format model type
00C1		data_format_model_ subtype	8UI	04	RO	Number of data format descriptors.
00C2	Hi	data_format_descriptor_0	16UI	08	RO	RAW8 mode - transmit top 8 bits of pixel data.
00C3	Lo			08		
00C4	Hi	data_format_descriptor_1	16UI	0A	RO	RAW10 mode - transmit top 10 bits of pixel data.
00C5	Lo			0A		
00C6	Hi	data_format_descriptor_2	16UI	0A	RO	10-8 compressed mode - transmit top 10 bits of pixel data, compressed to 8 bits.
00C7	Lo			08		
00C8	Hi	data_format_descriptor_3	16UI	0A	RO	10-6 compressed mode - transmit top 10 bits of pixel data, compressed to 6 bits.
00C9	Lo			06		

4.2.5 Setup registers [0x0100 to 0x0137]

Table 13. Setup registers [0x0100 to 0x0137]

Index	Byte	Register name	Data type	Default	Type	Comment
0100		mode_select	8UI	00	RW	Mode select. 0 = Software standby. 1 = Streaming.
0101		image_orientation	8B	00	RW	Image orientation Bit0: 0 - No mirror, 1 - horizontal mirror enable Bit1:0 = No flip, 1- vertical flip enable
0103		soft_reset	8UI	00	RW	Software reset returns the sensor to its power-on defaults. 0 = Normal operation. 1 = Software reset enabled.
0104		grouped_parameter_hold	8UI	00	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters. 0 = Consume values as normal. 1 = Do not consume values whilst set high.
0105		mask_corrupted_frames	8UI	00	RW	Setting this register to 1 prevents the sensor out-putting frames that have been corrupted by video timing parameter changes. 0 = Output as normal. 1 = Mask corrupted frames.
0106		fast_standby_ctrl	8UI	00	RW	SMIA fast standby control 0 = Frame completes before SW-STBY mode entry. 1 = Frame may be truncated before SW-STBY mode entry.
0107		cci_addr	8UI	20	RW	Device address.
0108		second_i2c_if_control	8UI	00	RW	Bit0: 0 - 2nd_cci_if_disable 1 - 2nd_cci_if_enable Bit1: 0 - 2nd_cci_if_ack_disable 1 - 2nd_cci_if_ack_enable
0109		cci_2nd_addr	8UI	20	RW	Additional device address that can be responded to.
0110		csi_channel_identifier	8UI	00	RW	The DMA (CCP2) or virtual (CSI2) channel identifier. Valid range = 0 to 7 for CCP2. Valid range = 0 to 3 for CSI2.

Table 13. Setup registers [0x0100 to 0x0137] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0111		csi_signalling_mode	8UI	02	RW	Determines which transmission signalling mode is to be used. 0 = CCP2 data-clock signalling. 1 = CCP2 data-strobe signalling. 2 = CSI2.
0112	Hi	csi_data_format	16UI	0A	RW	The value of this register contains the pixel width of the uncompressed pixel data. Valid values are 0xA and 0x8.
0113	Lo			0A		The value of this register contains the pixel width of the compressed pixel data. Valid values are 0xA and 0x8.
0114		csi_lane_mode	8UI	01	RW	Number of data lanes in use. 0 = 1-lane. 1 = 2-lane. Note: This register must be set to 0.
0115		csi2_10_to_8_dt	8UI	30	RW	CSI-2 data type for 10-to-8 compression.
0117		csi2_10_to_6_dt	8UI	31	RW	CSI-2 data type for 10-to-6 compression.
0120		gain_mode	8UI	00	RO	Global gain mode - this device only supports 0x00.
0130	Hi	vana_voltage	16UR	02	RW	Typical supplied VANA voltage.
0131	Lo			CC		
0132	Hi	vdig_voltage	16UR	01	RW	Typical supplied VDIG voltage.
0133	Lo			CC		
0134	Hi	vio_voltage	16UR	01	RW	Typical IO voltage.
0135	Lo			CC		
0136	Hi	ext_clkfreq	16UR	06	RW	8.8 fixed-point representation of the external clock-frequency, in MHz.
0137	Lo			00		

4.2.6 Integration and gain registers [0x0200 to 0x0215]

These registers are used to control the image exposure. See *Section 7.5: Exposure and gain control on page 65* for more information.

Table 14. Integration and gain registers [0x0200 to 0x0215]

Index	Byte	Register name	Data type	Default	Type	Comment
0200	Hi	fine_exp_req	16UI	02	RW	Fine integration time in pixels.
0201	Lo			AE		
0202	Hi	coarse_exp_req	16UI	00	RW	Coarse integration time in lines.
0203	Lo			00		
0204	Hi	gain_req	16UI	00	RW	Gain code for all channels.
0205	Lo			00		
020e	Hi	digital_gain_greenR	16UR	01	RW	Green (red row) channel digital gain value
020f	Lo			00		
0210	Hi	digital_gain_red	16UR	01	RW	Red channel digital gain value
0211	Lo			00		
0212	Hi	digital_gain_blue	16UR	01	RW	Blue channel digital gain value
0213	Lo			00		
0214	Hi	digital_gain_greenB	16UR	01	RW	Green (blue row) channel digital gain value.
0215	Lo			00		

4.2.7 Video timing registers [0x0300 to 0x0387]

For a full description of the video timing registers refer to *Chapter 6: Video data interface on page 49*.

Table 15. Video timing registers [0x0300 to 0x0387]

Index	Byte	Register name	Data type	Default	Type	Comment
0300	Hi	vt_pix_clk_div	16UI	00	RW	Video timing pixel clock divider.
0301	Lo			0A		
0302	Hi	vt_sys_clk_div	16UI	00	RW	Video timing system clock divider. Note: This value must be even for single lane modules
0303	Lo			01		
0304	Hi	pre_pll_div	16UI	00	RW	Pre-PLL clock divider value.
0305	Lo			01		
0306	Hi	pll_mult	16UI	00	RW	PLL multiplier value. Odd and even values can be used, but odd values result in the nearest lower even value being used (for example, 133 becomes 132).
0307	Lo			85		
0308	Hi	op_pix_clk_div	16UI	00	RW	Output timing pixel clock divider.
0309	Lo			0A		
030A	Hi	op_sys_clk_div	16UI	00	RW	Output timing system clock divider. Note: This value must be even for single lane modules
030B	Lo			01		
0340	Hi	frame_length_req	16UI	08	RW	Length of the video frame in lines.
0341	Lo			24		
0342	Hi	line_length_req	16UI	0A	RW	Length of a line of video in pixels.
0343	Lo			BE		
0344	Hi	x_start_req	16UI	00	RW	X pixel address of the top left corner of the visible pixel data.
0345	Lo			00		
0346	Hi	y_start_req	16UI	00	RW	Y line address of the top left corner of the visible pixel data.
0347	Lo			00		
0348	Hi	x_end_req	16UI	0A	RW	X pixel address of the bottom right corner of the visible pixel data.
0349	Lo			27		
034A	Hi	y_end_req	16UI	07	RW	Y line address of bottom right corner of the visible pixel data.
034B	Lo			9F		
034C	Hi	x_op_size_req	16UI	0A	RW	Width in pixels of the output image from the sensor.
034D	Lo			28		
034E	Hi	y_op_size_req	16UI	07	RW	Height in lines of the output image from the sensor.
034F	Lo			A0		

Table 15. Video timing registers [0x0300 to 0x0387] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0380	Hi	x_even_inc_req	16UI	00 01	RW	X address increment for even pixels.
0381	Lo					
0382	Hi	x_odd_inc_req	16UI	00 01	RW	X address increment for odd pixels.
0383	Lo					
0384	Hi	y_even_inc_req	16UI	00 01	RW	Y address increment for even lines.
0385	Lo					
0386	Hi	y_odd_inc_req	16UI	00 01	RW	Y address increment for odd lines.
0387	Lo					

4.2.8 Scaler and digital crop registers [0x0400 to 0x040F]

Table 16. Scaler and digital crop registers [0x0400 to 0x040F]

Index	Byte	Register name	Data type	Default	Type	Comment
0400	Hi	scale_mode_req	16UI	00 00	RW	Scaling mode 0 = No scaling 1 = Horizontal scaling
0401	Lo					
0402	Hi	scale_cosite_req	16UI	00 00	RW	Spatial sampling 0 = Bayer sampling 1 = Co-sited (2- or 4-component) 2 = Co-sited (3-component)
0403	Lo					
0404	Hi	scale_m_req	16UI	00 10	RW	Down scale factor. M component.
0405	Lo					
0406	Hi	scale_n	16UI	00	RO	Down scale factor. N component.
0407	Lo			10		
0408	Hi	digital_crop_x_offset	16UI	00	RW	Offset from X-address of the top left corner of the visible pixel data after analog crop, bin and subsample. Even numbers only (pixels).
0409	Lo			00		
040A	Hi	digital_crop_y_offset	16UI	00	RW	Offset from Y-address of the top left corner of the visible pixel data after analog crop, bin and subsample. Even numbers only (lines).
040B	Lo			00		
040C	Hi	digital_crop_image_width	16UI	0A	RW	Image width after digital crop. Even numbers only (pixels).
040D	Lo			28		
040E	Hi	digital_crop_image_height	16UI	07	RW	Image height after digital crop. Even numbers only (lines).
040F	Lo			A0		

4.2.9 Compression setup registers [0x0500]

Table 17. Compression setup registers [0x0500]

Index	Byte	Register name	Data type	Default	Type	Comment
0500 0501		compression_algorithm	16UI	00 01	RO	Compression algorithm is DPCM/PCM.

4.2.10 Test pattern registers [0x0600 to 0x0611]

Table 18. Test pattern registers [0x0600 to 0x0611]

Index	Byte	Register name	Data type	Default	Type	Comment
0600		man_spec_patt_req	8UI	00	RW	Enables maufacturer-specific test patterns. 0 = Enable SMIA test patterns. 1 = Enable manufacturer-specific test patterns.
0601		test_pattern_req	8UI	00	RW	SMIA test pattern selector. Note that the PN9 test pattern replaces data at output TX stage. bit0 = No pattern bit1 = Solid color bit2 = 100% color bars bit3 = Fade-to-grey color bars bit4 = Pseudo random-PN9
0602	Hi	test_data_red	16UI	00	RW	Test data used to replace Red pixel data - range 0 to 1023.
0603	Lo			00		
0604	Hi	test_data_greenr	16UI	00	RW	Test data used to replace Green pixel data on lines that also have Red pixels - range 0 to 1023.
0605	Lo			00		
0606	Hi	test_data_blue	16UI	00	RW	Test data used to replace Blue pixel data - range 0 to 1023.
0607	Lo			00		
0608	Hi	test_data_greenb	16UI	00	RW	Test data used to replace Green pixel data on lines that also have Blue pixels - range 0 to 1023.
0609	Lo			00		
060A	Hi	test_hcur_width	16UI	00	RW	Defines the width in pixels of the horizontal cursor.
060B	Lo			00		
060C	Hi	test_hcur_posn	16UI	00	RW	Defines the position of the top edge of the horizontal cursor.
060D	Lo			00		
060E	Hi	test_vcur_width	16UI	00	RW	Defines the width in pixels of the vertical cursor.
060F	Lo			00		
0610	Hi	test_vcur_posn	16UI	00	RW	Defines the left hand edge of the vertical cursor The value can be set to 0xFFFF which enables an automatic mode whereby the cursor advances every frame. Can be used to visually check the frame count.
0611	Lo			00		

4.2.11 CSI2 registers [0x808]

Table 19. CSI2 registers [0x808]

Index	Byte	Register name	Data type	Default	Type	Comment
0808		dphy_ctrl	8UI	00	RW	CSI2 DPHY control 1 = Use UI control. 2 = Use register control.

4.2.12 DPHY registers [0x820 to 0x823]

Table 20. DPHY registers [0x820 to 0x823]

Index	Byte	Register name	Data type	Default	Type	Comment
0820	Hi	dphy_channel_mbps_for_ui	32UR	00.00 00.00	RW	CSI2 DPHY requested (target) channel rate in Mbps (16.16 fixed-point representation) This is used to calculate the DPHY unit-interval (UI) value. It does not control the sensor clock setup, but should normally correspond to those settings. 0 = Sensor automatically calculates UI from host-programmed EXTCLK and clock divider values and reports in MAN_SPEC_DPHY__CLKLANE_UIX4 register. 80-1000 = Sensor calculates UI from Mbps value.
0821	3rd					
0822	2nd					
0823	Lo					

4.2.13 Binning registers [0x900 to 0x902]

Table 21. Binning registers [0x900 to 0x902]

Index	Byte	Register name	Data type	Default	Type	Comment
0900		binning_mode	8UI	00	RW	Binning mode. 0 = Disabled 1 = Enabled
0901		binning_type	8UI	00	RW	High-nibble = Column binning factor. High-nibble = Row binning factor.
0902		binning_weighting	8UI	00	RW	Binning weighting type: 0 = Averaged.

4.2.14 Data transfer registers [0x0A00 to 0x0A43]

Table 22. Data transfer registers [0x0A00 to 0x0A43]

Index	Byte	Register name	Data type	Default	Type	Comment
0A00		data_xfer_if1_ctrl	8UI	00	RW	bit0: 0 = Disable Xfer IF1. 1 = Enable Xfer IF1. bit1: 0 = Read enable on IF1 1 = Write enable on IF1 bit2: 0 = Disabled 1 = Clear error bits on IF1
0A01		data_xfer_if1_status	8UI	00	RO	bit0: Read IF ready bit1: Write IF ready. bit2: Data corrupt. bit3: Improper IF usage.
0A02		data_xfer_if1_page_select	8UI	00	RW	Select RW Pages from 0 to 255 for IF1.
0A04		DataXfer_Data0	8UI	00	RW	Data Xfer Interface - DataLoc0
--		--				--
0A43		DataXfer_Data63	8UI	00	RW	Data Xfer Interface - DataLoc63

4.2.15 Ideal raw registers [0x0B04 to 0x0B05]

Table 23. Ideal raw registers [0x0B04 to 0x0B05]

Index	Byte	Register name	Data type	Default	Type	Comment
0B04		black_level_correction_ enable	8UI	01	RW	Black level correction. 0 = Disabled 1 = Enabled
0B05		mapped_couplet_correct_ enable	8UI	01	RW	Mapped couplet correction enable. 0 = Disabled 1 = Enabled

4.2.16 Bracketing LUT registers [0x0E00 to 0x0E55]

Table 24. Bracketing LUT registers [0x0E00 to 0x0E55]

Index	Byte	Register name	Data type	Default	Type	Comment
0E00		bracketing_lut_ctrl	8UI	00	RW	Bracketing LUT Ctrl. 1-n - Bracketing over n frames
0E01		bracketing_lut_mode	8UI	00	RW	Bit[0] - Bracketing LUT Mode: 0 = return to SW standby after bracketing. 1 = continue in streaming after bracketing
0E02	Hi	bracketing_lut_entry_control	16UI	00	RW	Bracketing LUT entry control (Reserved).
0E03	Lo			00		
0E10	Hi	bracketing_lut_frame_a_coarse_int_time	16UI	00	RW	Bracketing LUT frame A coarse integration time
0E11	Lo			00		
0E12	Hi	bracketing_lut_frame_a_analog_gain_code	16UI	00	RW	Bracketing LUT frame A analog gain code
0E13	Lo			00		
0E14	Hi	bracketing_lut_frame_a_digital_gain_gr	16SR	00	RW	Bracketing LUT frame A digital gain GR
0E15	Lo			00		
0E16	Hi	bracketing_lut_frame_a_digital_gain_r	16SR	00	RW	Bracketing LUT frame A digital gain R
0E17	Lo			00		
0E18	Hi	bracketing_lut_frame_a_digital_gain_b	16SR	00	RW	Bracketing LUT frame A digital gain B
0E19	Lo			00		
0E1A	Hi	bracketing_lut_frame_a_digital_gain_gb	16SR	00	RW	Bracketing LUT frame A digital gain GB
0E1B	Lo			00		
0E1C	Hi	bracketing_lut_frame_a_bracketing_lut_entry	16UI	00	RW	Bracketing LUT frame A bracketing LUT entry
0E1D	Lo			00		
0E1E	Hi	bracketing_lut_frame_b_coarse_int_time	16UI	00	RW	Bracketing LUT frame B coarse integration time
0E1F	Lo			00		
0E20	Hi	bracketing_lut_frame_b_analog_gain_code	16UI	00	RW	Bracketing LUT frame B analog gain code
0E21	Lo			00		
0E22	Hi	bracketing_lut_frame_b_digital_gain_gr	16SR	00	RW	Bracketing LUT frame B digital gain GR
0E23	Lo			00		
0E24	Hi	bracketing_lut_frame_b_digital_gain_r	16SR	00	RW	Bracketing LUT frame B digital gain R
0E25	Lo			00		
0E26	Hi	bracketing_lut_frame_b_digital_gain_b	16SR	00	RW	Bracketing LUT frame B digital gain B
0E27	Lo			00		

Table 24. Bracketing LUT registers [0x0E00 to 0x0E55] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0E28	Hi	bracketing_lut_frame_b_ digital_gain_gb	16SR	00	RW	Bracketing LUT frame B digital gain GB
0E29	Lo			00		
0E2A	Hi	bracketing_lut_frame_b_ bracketing_lut_entry	16UI	00	RW	Bracketing LUT frame B bracketing LUT entry
0E2B	Lo			00		
0E2C	Hi	bracketing_lut_frame_c_ coarse_int_time	16UI	00	RW	Bracketing LUT frame C coarse integration time
0E2D	Lo			00		
0E2E	Hi	bracketing_lut_frame_c_ analog_gain_code	16UI	00	RW	Bracketing LUT frame C analog gain code
0E2F	Lo			00		
0E30	Hi	bracketing_lut_frame_c_ digital_gain_gr	16SR	00	RW	Bracketing LUT frame C digital gain GR
0E31	Lo			00		
0E32	Hi	bracketing_lut_frame_c_ digital_gain_r	16SR	00	RW	Bracketing LUT frame C digital gain R
0E33	Lo			00		
0E34	Hi	bracketing_lut_frame_c_ digital_gain_b	16SR	00	RW	Bracketing LUT frame C digital gain B
0E35	Lo			00		
0E36	Hi	bracketing_lut_frame_c_ digital_gain_gb	16SR	00	RW	Bracketing LUT frame C digital gain GB
0E37	Lo			00		
0E38	Hi	bracketing_lut_frame_c_ bracketing_lut_entry	16UI	00	RW	Bracketing LUT frame C bracketing LUT entry
0E39	Lo			00		
0E3A	Hi	bracketing_lut_frame_d_ coarse_int_time	16UI	00	RW	Bracketing LUT frame D coarse integration time
0E3B	Lo			00		
0E3C	Hi	bracketing_lut_frame_d_ analog_gain_code	16UI	00	RW	Bracketing LUT frame D analog gain code
0E3D	Lo			00		
0E3E	Hi	bracketing_lut_frame_d_ digital_gain_gr	16SR	00	RW	Bracketing LUT frame D digital gain GR
0E3F	Lo			00		
0E40	Hi	bracketing_lut_frame_d_ digital_gain_r	16SR	00	RW	Bracketing LUT frame D digital gain R
0E41	Lo			00		
0E42	Hi	bracketing_lut_frame_d_ digital_gain_b	16SR	00	RW	Bracketing LUT frame D digital gain B
0E43	Lo			00		
0E44	Hi	bracketing_lut_frame_d_ digital_gain_gb	16SR	00	RW	Bracketing LUT frame D digital gain GB
0E45	Lo			00		
0E46	Hi	bracketing_lut_frame_d_ bracketing_lut_entry	16UI	00	RW	Bracketing LUT frame D bracketing LUT entry
0E47	Lo			00		
0E48	Hi	bracketing_lut_frame_e_ coarse_int_time	16UI	00	RW	Bracketing LUT frame E coarse integration time
0E49	Lo			00		

Table 24. Bracketing LUT registers [0x0E00 to 0x0E55] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0E4A	Hi	bracketing_lut_frame_e_ analog_gain_code	16UI	00	RW	Bracketing LUT frame E analog gain code
0E4B	Lo			00		
0E4C	Hi	bracketing_lut_frame_e_ digital_gain_gr	16SR	00	RW	Bracketing LUT frame E digital gain GR
0E4D	Lo			00		
0E4E	Hi	bracketing_lut_frame_e_ digital_gain_r	16SR	00	RW	Bracketing LUT frame E digital gain R
0E4F	Lo			00		
0E50	Hi	bracketing_lut_frame_e_ digital_gain_b	16SR	00	RW	Bracketing LUT frame E digital gain B
0E51	Lo			00		
0E52	Hi	bracketing_lut_frame_e_ digital_gain_gb	16SR	00	RW	Bracketing LUT frame E digital gain GB
0E53	Lo			00		
0E54	Hi	bracketing_lut_frame_e_ bracketing_lut_entry	16UI	00	RW	Bracketing LUT frame E bracketing LUT entry
0E55	Lo			00		

4.2.17 Integration and gain limit registers [0x1000 to 0x1089]

Table 25. Integration and gain limit registers [0x1000 to 0x1089]

Index	Byte	Register name	Data type	Default	Type	Comment
1000	Hi	integration_capability	16UI	00	RO	This device supports coarse and smooth (1 pixel) integration.
1001	Lo			01		
1004	Hi	min_coarse	16UI	00	RO	Minimum coarse integration time (in line periods).
1005	Lo			00		
1006	Hi	coarse_margin	16UI	00	RO	Current frame length - current max coarse exposure (in line periods).
1007	Lo			09		
1008	Hi	min_fine	16UI	02	RO	Minimum fine integration time (in pixels).
1009	Lo			AE		
100a	Hi	fine_margin	16UI	08	RO	Current line length - maximum fine exposure (pixel periods).
100b	Lo			02		
1080	Hi	digital_gain_capability	16UI	00	RO	This device supports digital gain.
1081	Lo			01		
1084	Hi	digital_gain_min	16UI	00	RO	Minimum supported digital gain value.
1085	Lo			08		
1086	Hi	digital_gain_max	16UI	01	RO	Maximum supported digital gain value
1087	Lo			F8		
1088	Hi	digital_gain_step_size	16UI	00	RO	Digital gain step size.
1089	Lo			08		

4.2.18 Video timing limit registers [0x1100 to 0x11C7]

Table 26. Video timing limit registers [0x1100 to 0x11C7]

Index	Byte	Register name	Data type	Default	Type	Comment
1100	Hi	min_ext_clk_freq	32UI	40	RO	Minimum external clock frequency.
1101	3rd			C0		
1102	2nd			00		
1103	Lo			00		
1104	Hi	max_ext_clk_freq	32UI	41	RO	Maximum external clock frequency.
1105	3rd			D8		
1106	2nd			00		
1107	Lo			00		
1108	Hi	min_pre_pll_clk_div	16UI	00	RO	Minimum value of pre-PLL clock divider.
1109	Lo			01		
110A	Hi	max_pre_pll_clk_div	16UI	00	RO	Maximum value of pre-PLL clock divider.
110B	Lo			04		
110C	Hi	min_pll_ip_freq	32UI	40	RO	Minimum input clock frequency to the PLL.
110D	3rd			C0		
110E	2nd			00		
110F	Lo			00		
1110	Hi	max_pll_ip_freq	32UI	41	RO	Maximum input clock frequency to the PLL.
1111	3rd			40		
1112	2nd			00		
1113	Lo			00		
1114	Hi	min_pll_multiplier	16UI	00	RO	Minimum PLL multiplier value.
1115	Lo			4C		
1116	Hi	max_pll_multiplier	16UI	01	RO	Maximum PLL multiplier value.
1117	Lo			4C		
1118	Hi	min_pll_op_freq	32UI	44	RO	Minimum PLL output frequency.
1119	3rd			61		
111A	2nd			00		
111B	Lo			00		
111C	Hi	max_pll_op_freq	32UI	44	RO	Maximum PLL output frequency.
111D	3rd			FA		
111E	2nd			00		
111F	Lo			00		

Table 26. Video timing limit registers [0x1100 to 0x11C7] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
1120	Hi	min_vt_sys_clk_div	16UI	00	RO	Minimum video timing system clock divider value. Note: This value should be 2 for single lane modules.
1121	Lo			01		
1122	Hi	max_vt_sys_clk_div	16UI	00	RO	Maximum video timing system clock divider value.
1123	Lo			04		
1124	Hi	min_vt_sys_clk_freq	32UI	43	RO	Minimum video timing system clock frequency.
1125	3rd			61		
1126	2nd			00		
1127	Lo			00		
1128	Hi	max_vt_sys_clk_freq	32UI	44	RO	Maximum video timing system clock frequency. 2000Mhz Note: This value should be 1000Mhz
1129	3rd			FA		
112A	2nd			00		
112B	Lo			00		
112C	Hi	min_vt_pix_clk_freq	32UI	41	RO	Minimum video timing pixel clock frequency.
112D	3rd			F0		
112E	2nd			00		
112F	Lo			00		
1130	Hi	max_vt_pix_clk_freq	32UI	43	RO	Maximum video timing pixel clock frequency.
1131	3rd			28		
1132	2nd			00		
1133	Lo			00		
1134	Hi	min_vt_pix_clk_div	16UI	00	RO	Minimum video timing pixel clock divider value.
1135	Lo			04		
1136	Hi	max_vt_pix_clk_div	16UI	00	RO	Maximum video timing pixel clock divider value.
1137	Lo			0A		
1140	Hi	min_frame_length	16UI	00	RO	Minimum frame length in lines.
1141	Lo			D9		
1142	Hi	max_frame_length	16UI	FF	RO	Maximum frame length in lines.
1143	Lo			FF		
1144	Hi	min_line_length	16UI	0A	RO	Minimum line length in pixel clocks.
1145	Lo			BE		
1146	Hi	max_line_length	16UI	3F	RO	Maximum line length in pixel clocks.
1147	Lo			FF		

Table 26. Video timing limit registers [0x1100 to 0x11C7] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
1148	Hi	min_line_blanking	16UI	00	RO	Minimum line blanking in pixel clocks.
1149	Lo			86		
114A	Hi	min_frame_blanking	16UI	00	RO	Minimum frame blanking in lines.
114B	Lo			16		
114C	Hi	min_line_length_pck_ step_size	16UI	00	RO	Minimum step size of line length pck.
114D	Lo			01		
1160	Hi	min_op_sys_clk_div	16UI	00	RO	Minimum output timing system clock divider value. Note: This value should be 2 for single lane modules.
1161	Lo			01		
1162	Hi	max_op_sys_clk_div	16UI	00	RO	Maximum output timing system clock divider value.
1163	Lo			14		
1164	Hi	min_op_sys_clk_freq	32UI	42	RO	Minimum output timing system clock frequency.
1165	3rd			34		
1166	2nd			00		
1167	Lo			00		
1168	Hi	max_op_sys_clk_freq	32UI	44	RO	Maximum output timing system clock frequency.2000MHz Note: This value should be 1000Mhz
1169	3rd			FA		
116A	2nd			00		
116B	Lo			00		
116C	Hi	min_op_pix_clk_div	16UI	00	RO	Minimum output timing pixel clock divider value.
116D	Lo			06		
116E	Hi	max_op_pix_clk_div	16UI	00	RO	Maximum output timing pixel clock divider value.
116F	Lo			0A		
1170	Hi	min_op_pix_clk_freq	32UI	40	RO	Minimum output timing pixel clock frequency.
1171	3rd			90		
1172	2nd			00		
1173	Lo			00		
1174	Hi	max_op_pix_clk_freq	32UI	43	RO	Maximum output timing pixel clock frequency.
1175	3rd			28		
1176	2nd			00		
1177	Lo			00		
1180	Hi	x_addr_min	16UI	00	RO	Minimum XADDR value.
1181	Lo			00		

Table 26. Video timing limit registers [0x1100 to 0x11C7] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
1182	Hi	y_addr_min	16UI	00	RO	Minimum YADDR value.
1183	Lo			00		
1184	Hi	x_addr_max	16UI	0A	RO	Maximum XADDR value.
1185	Lo			27		
1186	Hi	y_addr_max	16UI	07	RO	Maximum YADDR value.
1187	Lo			9F		
1188	Hi	x_op_size_min	16UI	01	RO	Minimum X output size in pixels.
1189	Lo			00		
118A	Hi	y_op_size_min	16UI	00	RO	Minimum Y output size in lines.
118B	Lo			C0		
118C	Hi	x_op_size_max	16UI	0A	RO	Maximum X output size in pixels.
118D	Lo			28		
118E	Hi	y_op_size_max	16UI	07	RO	Maximum Y output size in lines.
118F	Lo			A0		
11C0	Hi	even_inc_min	16UI	00	RO	Minimum even increment used in subsampling.
11C1	Lo			01		
11C2	Hi	even_inc_max	16UI	00	RO	Maximum even increment used in subsampling.
11C3	Lo			01		
11C4	Hi	odd_inc_min	16UI	00	RO	Minimum odd increment used in subsampling.
11C5	Lo			01		
11C6	Hi	odd_inc_max	16UI	00	RO	Maximum odd increment used in subsampling.
11C7	Lo			13		

4.2.19 Scaling limit registers [0x1200 to 0x120F]

Table 27. Scaling limit registers [0x1200 to 0x120F]

Index	Byte	Register name	Data type	Default	Type	Comment
1200	Hi	scaling_capability	16UI	00	RO	VS6955CA supports horizontal digital scaling
1201	Lo			01		
1204	Hi	scale_m_min	16UI	00	RO	Minimum M value for downscale.
1205	Lo			10		
1206	Hi	scale_m_max	16UI	00	RO	Maximum M value for downscale.
1207	Lo			A3		
1208	Hi	scale_n_min	16UI	00	RO	Minimum N value for downscale.
1209	Lo			10		
120A	Hi	scale_n_max	16UI	00	RO	Maximum N value for downscale.
120B	Lo			10		
120C	Hi	spatial_sampling_ capability	16UI	00	RO	Spatial sampling capability Bayer sampling supported 2 or 4 component co-sited supported
120D	Lo			03		
120E	Hi	digital_crop_capability	16UI	00	RO	Digital crop is supported. Note. This should be a 8 bit register. i.e. The value for 0x120E should be 01
120F	Lo			01		

4.2.20 Compression capability registers [0x1300]

Table 28. Compression capability registers [0x1300]

Index	Byte	Register name	Data type	Default	Type	Comment
1300	Hi	compression_capability	16UI	00	RO	Compression capability is DPCM/PCM.
1301	Lo			01		

4.2.21 Derate capability registers [0x1500 to 0x1502]

Table 29. Derate capability registers [0x1500 to 0x1502]

Index	Byte	Register name	Data type	Default	Type	Comment
1500	Hi	fifo_size_pixels	16UI	00	RO	FIFO size in pixels (derate sync RAM).
1501	Lo			00		
1502		fifo_support_capability	8UI	01	RO	VS6955CA supports derating

4.2.22 DPHY capability registers [0x1600 to 0x1604]

Table 30. DPHY capability registers [0x1600 to 0x1604]

Index	Byte	Register name	Data type	Default	Type	Comment
1600		dphy_ctrl_capability	8UI	03	RO	CSI2 DPHY control capability: Automatic DPHY control supported. UI based DPHY control supported.
1601		csi_lane_mode_capability	8UI	03	RO	1 and 2 lane supported. Note: This register should be 1 (Only 1 lane supported)
1602		csi_signalling_mode_ capability	8UI	07	RO	CCP2 data/clock supported. CCP2 data/strobe supported. CSI2 supported.
1603		fast_standby_capability	8UI	01	RO	Fast standby is supported for rolling shutter).
1604		cci_address_control_ capability	8UI	07	RO	VS6955CA supports: – SW changeable CCI address – 2nd CCI address. – 2nd SW changeable CCI address.

4.2.23 Bitrate limit registers [0x1608]

Table 31. Bitrate limit registers [0x1608]

Index	Byte	Register name	Data type	Default	Type	Comment
1608	Hi	max_per_lane_bitrate_1_ lane_mode_mbps	32UR	03	RO	Maximum bitrate for a 1 lane configuration.
1609	3rd			E8		
160A	2nd			00		
160B	Lo			00		

4.2.24 Binning capability registers [0x1700 to 0x1714]

Table 32. Binning capability registers [0x1700 to 0x1714]

Index	Byte	Register name	Data type	Default	Type	Comment
1700	Hi	min_frame_length_lines_bin	16UI	00	RO	Minimum frame length (lines) allowed in binning mode.
1701	Lo			D9		
1702	Hi	max_frame_length_lines_bin	16UI	FF	RO	Maximum possible number of lines per frame in binning mode.
1703	Lo			FF		
1704	Hi	min_line_length_pck_bin	16UI	0A	RO	Minimum line length (pixel clocks) allowed in binning mode.
1705	Lo			BE		
1706	Hi	max_line_length_pck_bin	16UI	3F	RO	Maximum possible number of pixel clocks per line in binning mode.
1707	Lo			FF		
1708	Hi	min_line_blanking_pck_bin	16UI	00	RO	Minimum line blanking time in pixel clocks in binning mode.
1709	Lo			86		
170A	Hi	fine_integration_time_min_bin	16UI	02	RO	Minimum fine integration time allowed in binning mode (in pixels).
170B	Lo			51		
170C	Hi	fine_integration_time_max_margin_bin	16UI	09	RO	Margin used to determine the maximum fine integration time allowed in binning mode (in pixels).
170D	Lo			D8		
1710		binning_capability	8UI	01	RO	Binning supported
1711		binning_weighting_capability	8UI	01	RO	Binning weighting capability: Averaged weighting supported
1712		binning_sub_types	8UI	02	RO	Number of binning subtypes available.
1713		binning_type_1	8UI	22	RO	Binning type is 2 x 2 (Col x Row).
1714		binning_type_2	8UI	44	RO	Binning type is 4 x 4 (Col x Row).

5 Optical specification

5.1 Lens characteristics

Table 33. Lens design characteristics for first source lens supplier

Parameter	Value					
Construction	4-element plastic lens					
F/number	2.4					
Effective focal length	3 mm (primary wavelength 530 nm used)					
Diagonal FOV	74° +/- 1°					
Distortion	TV: <|2%| Absolute: <|1.0%| across whole field (by design)					
Relative illumination (lens only)	40% at full image height, typical design value					
Spectral weighting: Wavlength (nm) Weight	656.28 151	587.56 318	546.07 312	486.13 157	435.84 49	404.66 13
Lateral chromatic aberration from 435 nm to 656 nm	<2.8um					
Coating reflectance - All surfaces are coated.	<1%					
Maximum chief ray angle	28.4°					
IR coating filter cut-off wavelength	670 nm +/-8 nm					

5.2 User precaution

As is common with many CMOS imagers, the camera should not be pointed at bright static objects for long periods of time as permanent damage to the sensor may occur.

6 Video data interface

The video stream output from the VS6955CA through the compact camera port (CCP) or camera serial interface (CSI) contains both video data and other auxiliary information. This section describes the frame formats.

The selection of the video data format is controlled using the following register: CSI_SIGNALLING_MODE (0x0111)

0 - CCP2 data/clock

1 - CCP2 data/strobe

2 - CSI-2 (default)

Changing the video data format must be performed when the sensor is in software standby.

- The VS6955CA supports maximum output data rate of 1.0 Gbps when operated in CSI-2 single lane mode.
- The VS6955CA CCP lane is capable of transmitting at 640 Mbps.
- The CSI-2 data lane transmitter supports:
  - unidirectional master
  - HS-TX
  - LP-TX (ULPS)
  - CIL-MUYN function
- The CSI-2 clock lane transmitter supports:
  - unidirectional master
  - HS-TX
  - LP-TX (ULPS)
  - CIL-MCNN function

6.1 Frame format

The frame format for the VS6955CA is described by the frame format description registers, see *Table 10 on page 25*. For CCP2 this results in a frame as shown in *Figure 10* and for CSI-2 it results in a frame as shown in *Figure 11*.

Figure 10. VS6955CA CCP2 frame format

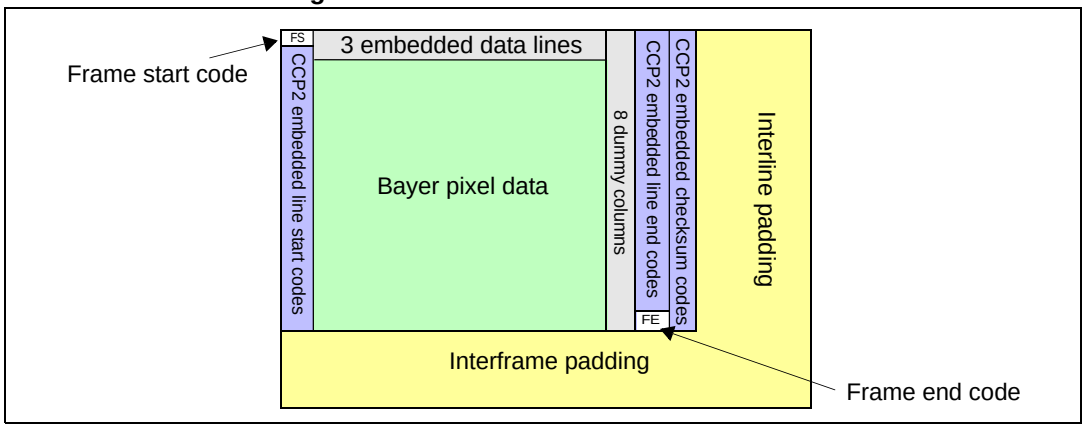
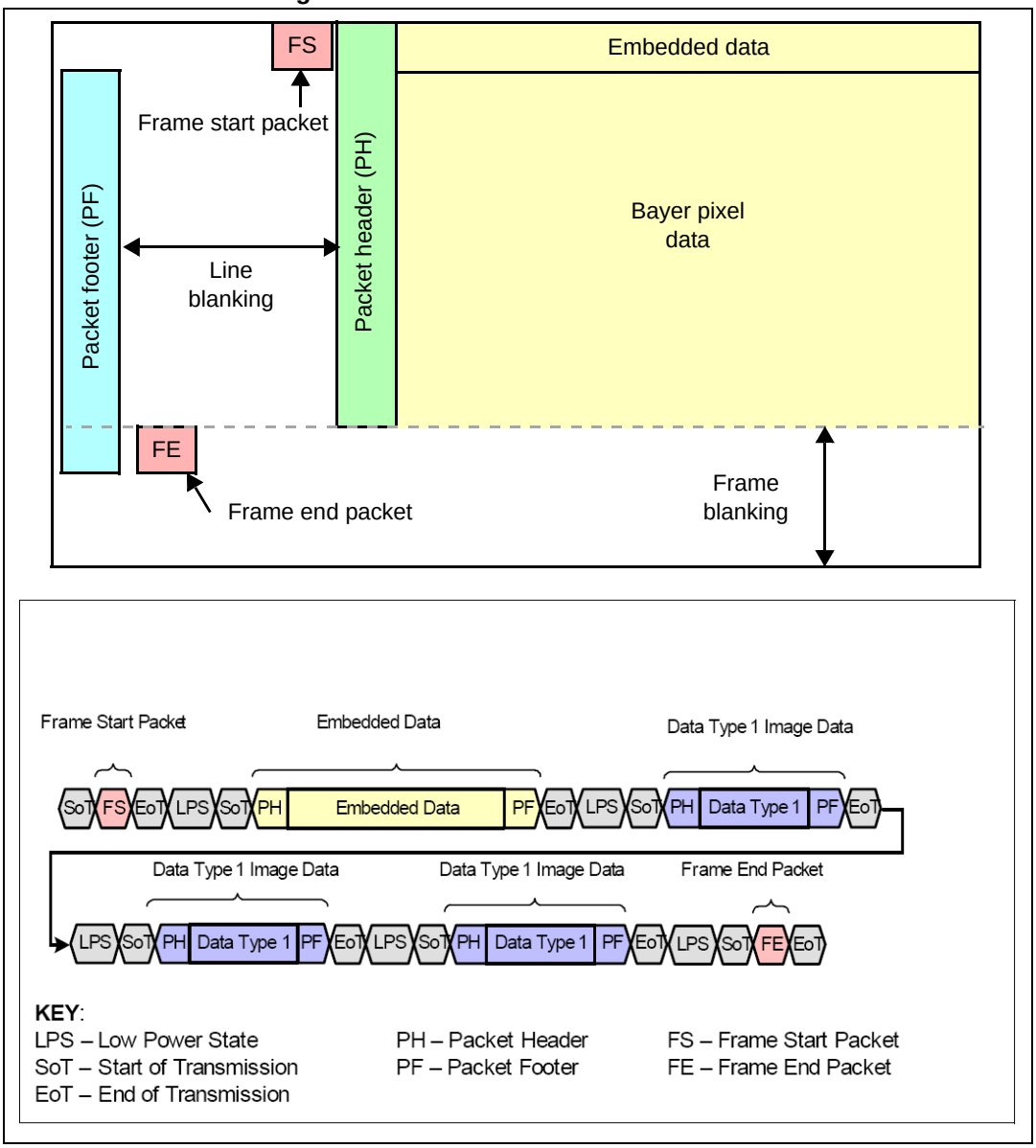


Figure 11. VS6955CA CSI-2 frame format



Embedded data lines

The embedded data lines provide a mechanism to embed non-image data such as sensor configuration details within the output data stream. The number of embedded data lines at the start and end of the frame is specified as part of the frame format description. VS6955CA has three embedded data lines.

Dummy pixel data

This is invalid pixel data. The receiver should always ignore dummy pixel data. The VS6955CA has eight dummy columns.

Visible pixel data

The visible pixels contain valid image data.The correct integration time and analog gain for the visible pixels is specified in the blank lines at the start of the frame.The number of visible pixels can be varied with the requested frame size.

Dark pixel data (light shielded pixels)

The VS6955CA has 0 dark pixels.

Black pixel data (zero integration time)

The VS6955CA has 0 black pixels.

Manufacturer specific pixel data

The VS6955CA has 0 manufacturer specific pixels.

Interline padding/line blanking

During interline padding all bits in the data stream in a CCP2 frame are set to 1.

In a CSI-2 frame there is no concept of line blanking being transmitted, the sensor simply spends a longer time in the LP state between active line data.

Interframe padding/frame blanking

During interframe padding all bits in the data stream in a CCP2 frame are set to 1.

In a CSI-2 frame there is no concept of frame blanking being transmitted, the sensor simply spends a longer time in the LP state at the end of the active data for a frame.

7 Video timing

This section specifies the timing for the image data that is read out from the pixel array and the output image data. These are not necessarily the same size.

The application of all of the video timing read/write parameters must be re-timed to the start of the frame boundary to ensure that the parameters are consistent within a frame.

The video stream which is output from the VS6955CA contains both video data and other auxiliary information.

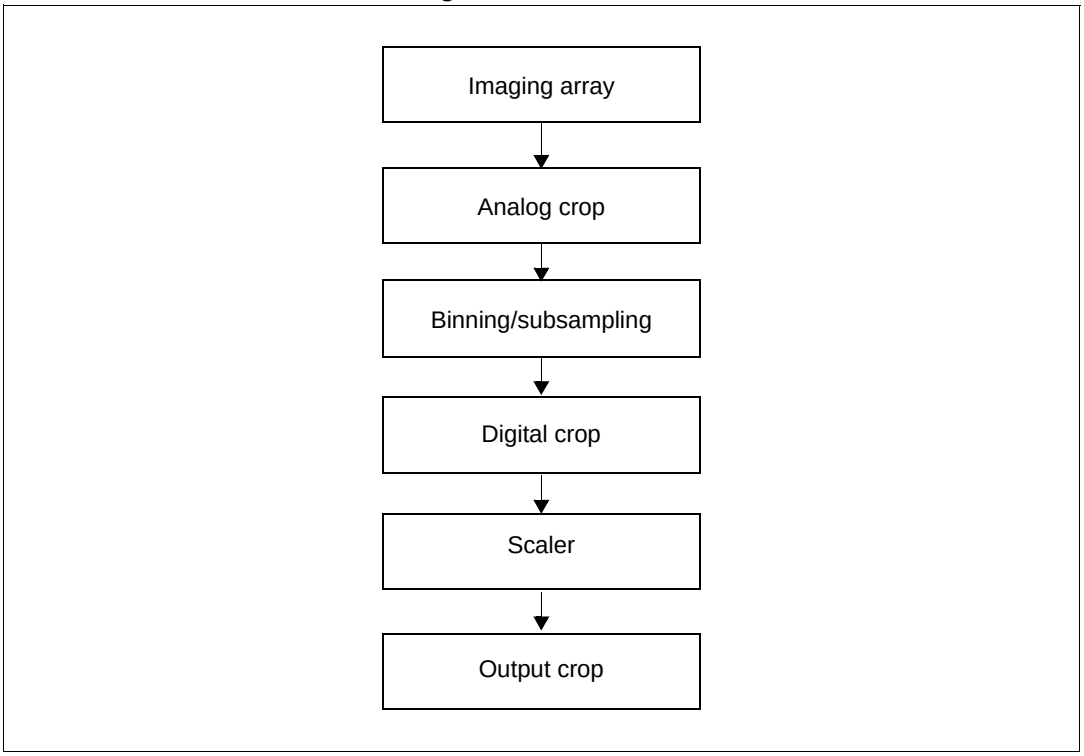
7.1 Output size

The VS6955CA has the following methods available to achieve the required output size, these can be used independently or in conjunction with any other:

- analog crop, see *Section 7.1.1 on page 53*
- subsampling, see *Section 7.1.4 on page 55*
- binning, see *Section 7.1.3 on page 55*
- digital cropping, see *Section 7.1.5 on page 56*
- scaling, see *Section 7.1.6 on page 56*
- output crop, see *Section 7.1.7 on page 58*

The programmable image size and output size are independent functions. It is the responsibility of the host to ensure that these functions are programmed correctly for the intended application. These functions also reduce the amount of data and therefore reduce the peak data rate of CCP2/CSI-2.

Figure 12. Data flow

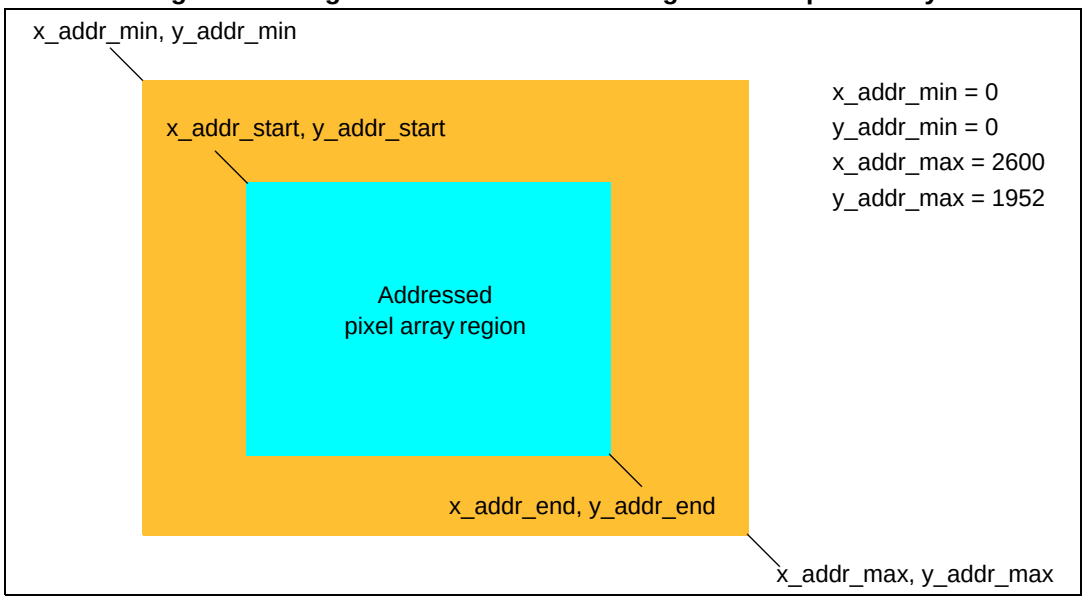


7.1.1 Programmable addressable region of the pixel array

The native size for the VS6955CA is 2592 x 1944, the maximum addressable array is 2600 x 1952 which gives border pixels (outer 4 rows and 4 columns) for the color reconstruction algorithms to use at the edges of the array.

By programming the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers it is possible to use the full size of the array as you would do for a native size output or you can select a “window of interest”. The addressed region of the array is used in any subsequent subsampling or scaling.

Figure 13. Programmable addressable region of the pixel array



The host must ensure the following rules are kept;

- the end address must be greater than the start address
- the x and y start addresses are restricted to even numbers only, and the x and y end addresses are restricted to odd numbers only, to ensure that there is always a even number of pixels read out

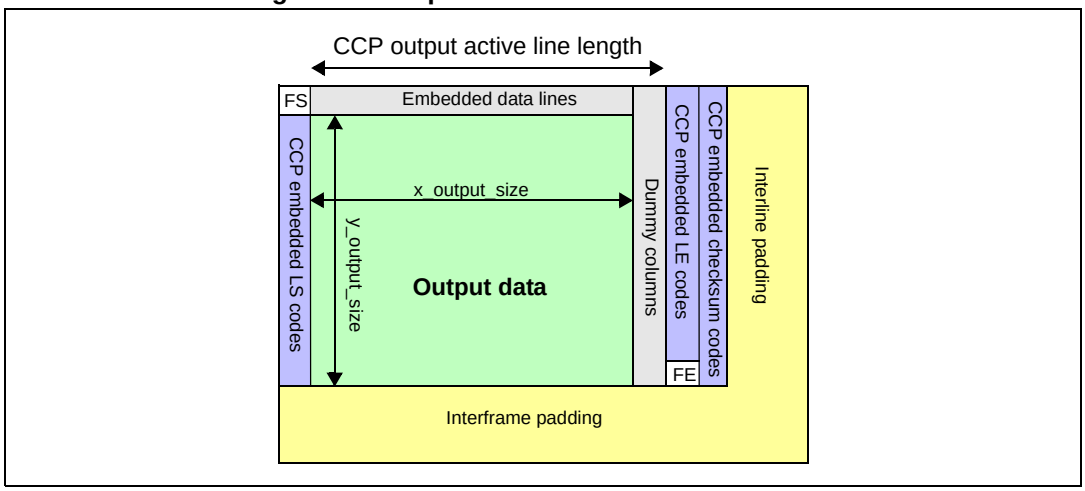
7.1.2 Programmable width and height for output image data

The x_output_size and y_output_size registers are not intended as the primary cropping controls.

They are intended to define the position of the LE/FE codes in the CCP or CSI-2 data frame so that the sensor does not need to calculate this based on region of interest or subsampling settings. It should be expected that the host will set the output sizes to exactly enclose the output image data. If the host should not do this, the VS6955CA will treat the output sizes as being calculated from the top left hand corner of the output array. So in the case where output sizes are smaller than the output data, the data shall be cropped from its right hand and lower limits. In the case where larger than the output data, the lines shall be padded out to the defined output size with undefined data.

Note: Eight additional columns of dummy data are added to all output images. This should be taken into account when defining output widths.

Figure 14. Output size within a CCP data frame

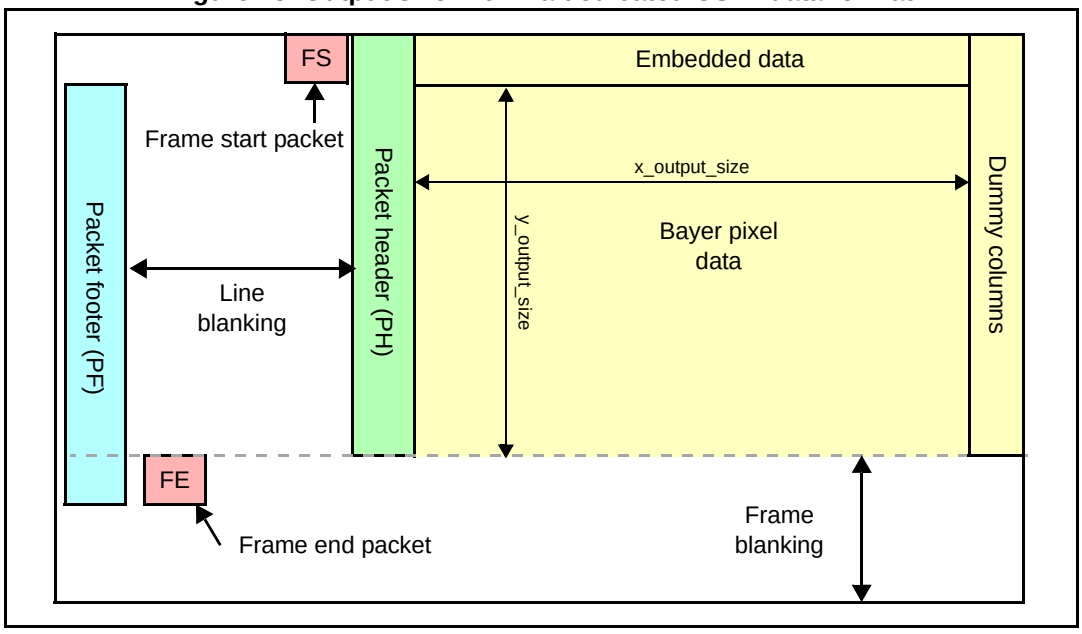


Note: CCP2 requires that the CCP output active line length (between start and end sync codes) for:

- *RAW8 is a multiple of 4 pixels*
- *RAW10 is a multiple of 16 pixels*

The host must control the x_output_size to ensure that the CCP output active line length (x_output_size + 8) meets the above criteria.

Figure 15. Output size within a dedicated CSI-2 data format



Note: CSI-2 requires that the CSI-2 output active line length (between start and end sync codes) for:

- *RAW8 is a multiple of 2 pixels*
- *RAW10 is a multiple of 4 pixels*

The host must control the x_output_size to ensure that the CSI-2 output active line length (x_output_size + 8) meets the above criteria.

7.1.3 Analog pixel binning

The VS6955CA also has a binning mode, sometimes also referred to as analogue Bayer scaling, that offers a reduced size full field of view image. The pixel binning mode averages row and column pixel data.

The binning mode results in a reduced number of lines and so can be used to give a higher image frame rate. Compared to subsampling, analog binning makes use of the light gathered from the whole pixel array and it results in higher image quality.

The binning mode is scaled by 2 x 2 or by 4 x 4 in the X and Y direction.

7.1.4 Subsampling

Subsampling is achieved by programming the x_odd_inc and y_odd_inc registers.

If the pixel being readout has an even address then the address is incremented by the even increment value either x_even_inc or y_even_inc. If the pixel being readout has an odd address then the address is incremented by the odd increment value either x_odd_inc or y_odd_inc.

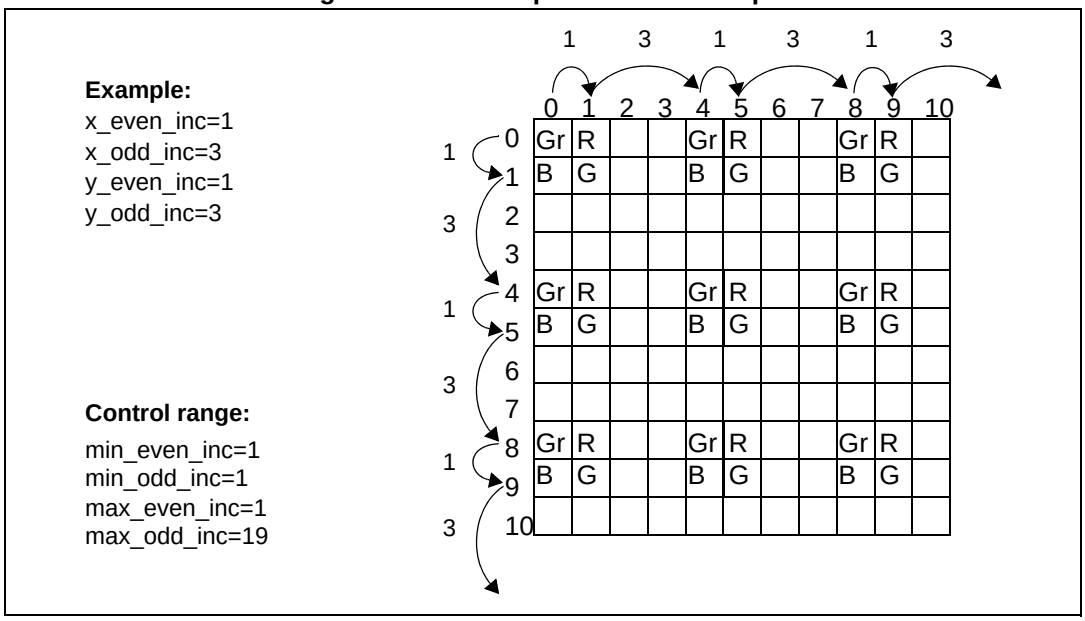
The subsampled readout is disabled by setting the odd and even increment values to 1. (The even increment must always be set to 1.)

Subsampling acts upon the addressed region of the array which is determined by the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers.

The equation for the sub-sampling factor is given below:

$$\text{sub\_sampling\_factor} = \frac{\text{even\_inc} + \text{odd\_inc}}{2}$$

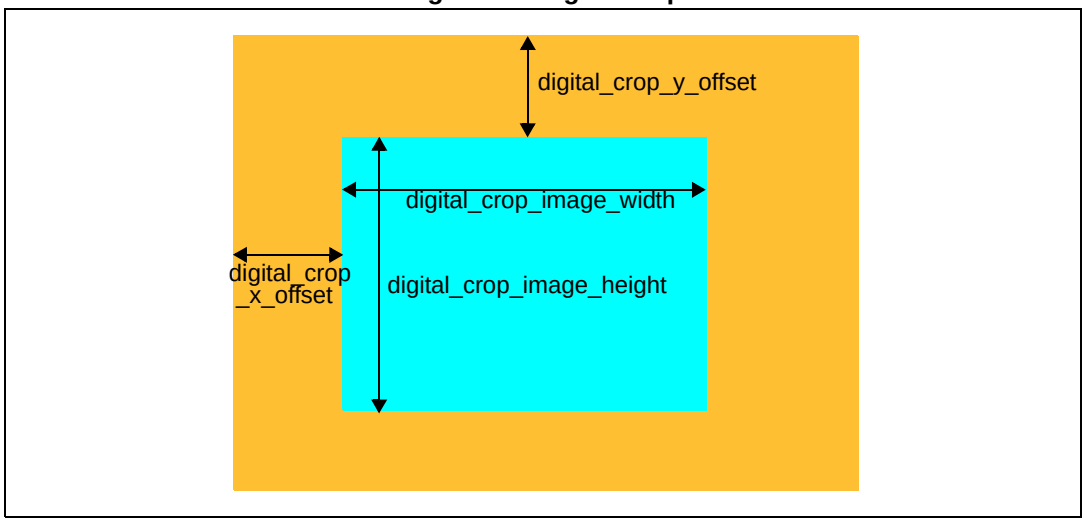
Figure 16. Subsample readout example



7.1.5 Digital crop

Digital crop can be used in addition to or instead of the analog crop function. It occurs after the subsampling function. It is affected by the amount of subsampling as well as by the analog crop. Since the input to the digital crop block is variable, there are no limit registers associated with digital crop.

Figure 17. Digital crop



The host must ensure the following rule is kept:

- the x and y offsets and the image width and height are restricted to even numbers only

Note: In VS6955CA it is mandatory to maintain a consistency between y_output_size and digital_crop_image_height to have a similar value.

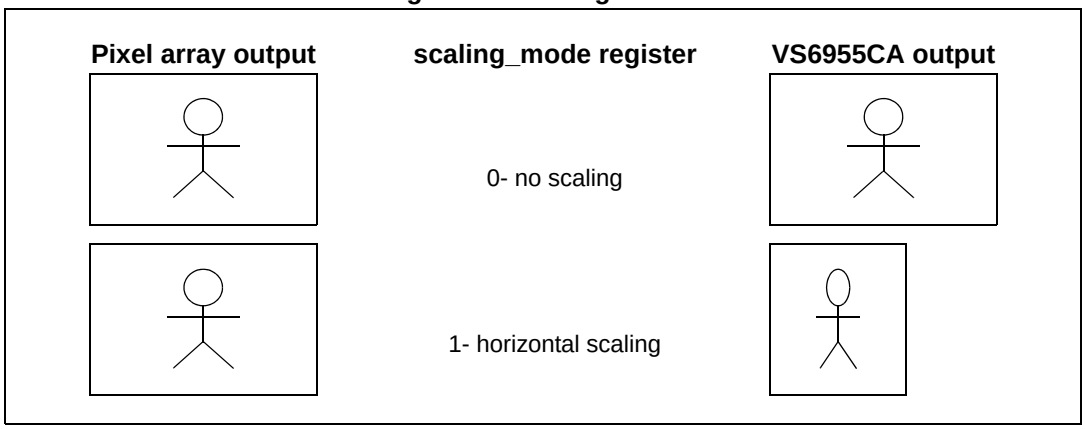
7.1.6 Scaling

The image scaling function within the sensor provides a flexible way of generating lower resolution full field of view image data, at a reduced data rates, for viewfinder and video applications.

The scaler is able to scale the full resolution of the sensor down to within 10% of a the target image size (the smallest output size is 256x192). This flexibility means that the VS6955CA can support a wide range of LCD viewfinder sizes and different codec resolutions.

The VS6955CA has two scaling modes which are controlled by the scale_mode_req register shown in *Figure 18*.

Figure 18. Scaling modes



Scaler quality

The scaler supports two options for the spatial sampling of the scaled image data (see *Figure 19*).

- Bayer sampled scaled image data

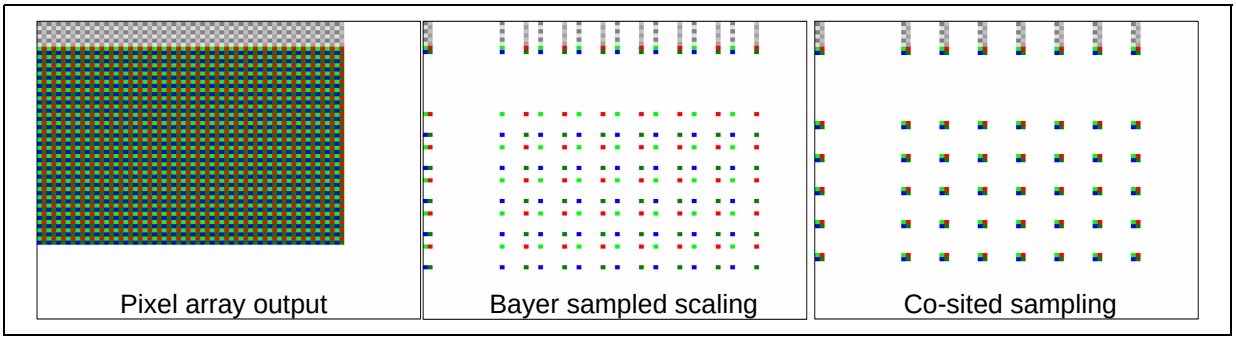
  The sampling point for the scaler for the output Gr value appears to be in the centre of the Gr pixel (that is between the first and second pixels and between the first and second rows of the original input Bayer pixel data). The R (or B) sampling points are similarly in the centre of the R pixel (or B pixel).

- Co-sited scaled image data

  The sampling point for the Gr, R. Gb and B vales in each output ‘quad’ are functions of the same color input array pixels such that the spatial sampling point for all four appears to be in the centre of the ‘quad’ that is between the second and third pixels and between the first and second rows.

The spatial sampling mode is controlled by the scale_cosite_req `register`.

Figure 19. Scaler quality



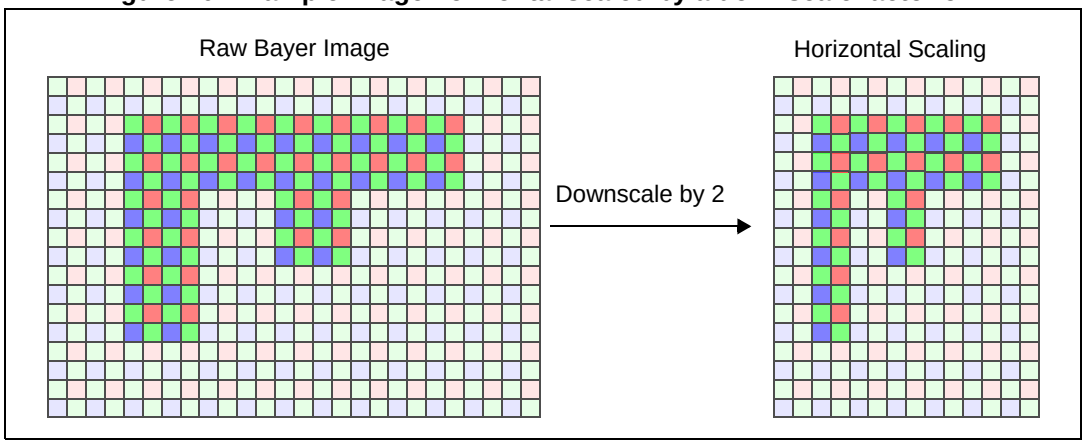
Down scaler factor

The down scaler factor is controlled by an M/N ratio, scale_m is >= 16 and scale_n is fixed at 16. scale_m is in the range 16 to 164.

$$\text{down\_scale\_factor} = \frac{\text{scale\_m}}{\text{scale\_n}} = \frac{\text{scale\_m}}{16}$$

This single down scale factor is used by the horizontal scalers. The scaler acts upon the addressed region of the array which is determined by the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers.

Figure 20. Example image horizontal scaled by a downscale factor of 2

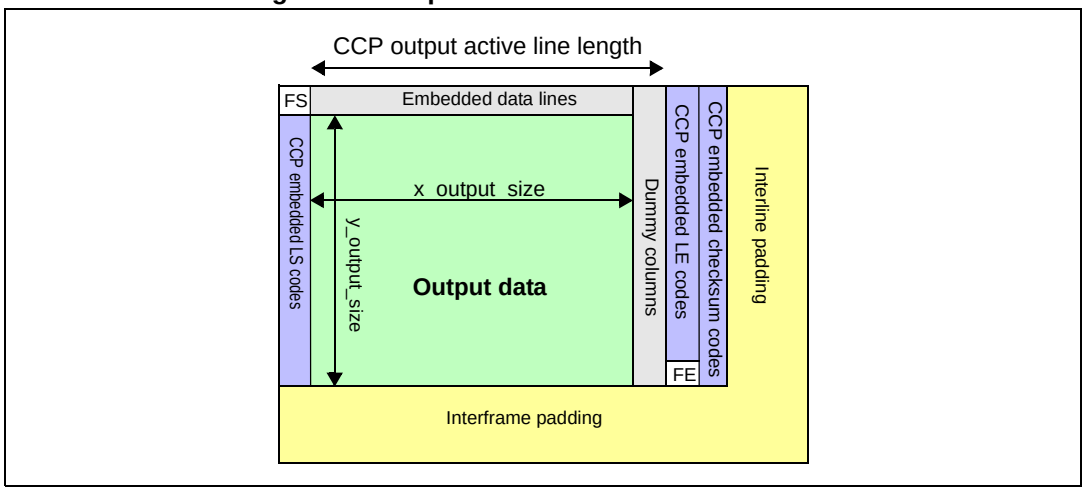


7.1.7 Output crop

The x_output_size and y_output_size registers are not intended as the primary cropping controls.

They are intended to define the position of the LE/FE codes in the CCP2 and CSI-2 data frame to comply with SMIA CCP2 and MIPI CSI-2 data format rules. It is expected that the host sets the output sizes to exactly enclose the output image data. If the host does not do this, the VS6955CA treats the output sizes as being calculated from the top left hand corner of the output array. So in the case where output sizes are smaller than the output data, the data is cropped from its right hand and lower limits. In the case where larger than the output data, the lines are padded out to the defined output size with undefined data.

Figure 21. Output size within a CCP data frame



Note: CCP2 requires that the CCP output active line length (between start and end sync codes) for RAW8 is a multiple of 4 and for RAW10 is a multiple of 16.

CSI-2 requires that RAW8 is a multiple of 2 pixels (actual definition is 1 pixel but 2 are required to preserve the Bayer pattern) and RAW10 is a multiple of 4 pixels (40 bits).

The host must control the x_output_size to ensure that the CCP output active line length meets the above criteria.

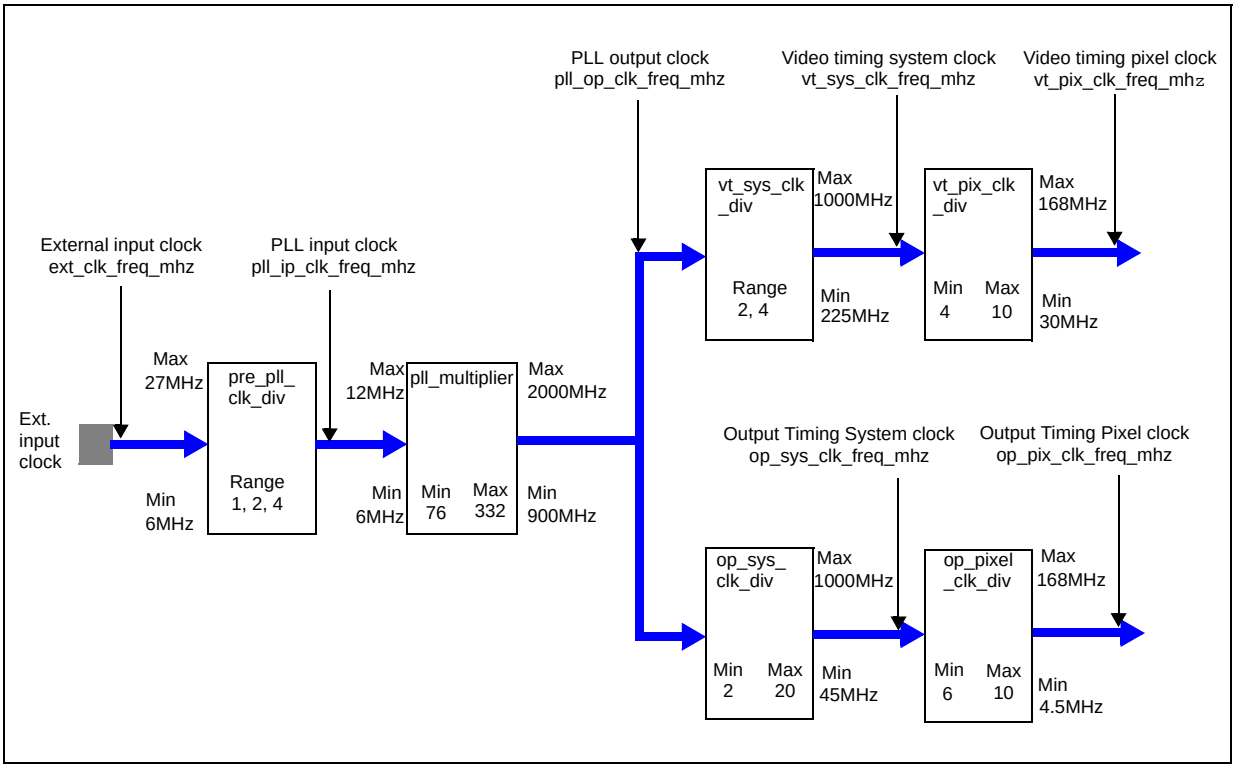
7.1.8 PLL block

The VS6955CA contains a phase locked loop (PLL) block, which generates all the necessary internal clocks from the external clock input. Changes to the PLL settings on the VS6955CA are only consumed on the software standby to streaming mode transition.

Figure 22 shows the internal functional blocks, which define the relationship between the external input clock frequency and the pixel clock frequency.

The majority of the logic within the device is clocked by vt_sys_clk however the CCI block is clocked by the external input clock.

Figure 22. VS6955CA clock relationships



The equations relating the input clock frequency to pixel clock frequencies are given below.

$$vt\_pix\_clk\_freq\_mhz = \frac{ext\_clk\_freq\_mhz \times pll\_multiplier}{pre\_pll\_clk\_div \times vt\_sys\_clk\_div \times vt\_pix\_clk\_div}$$

$$op\_pix\_clk\_freq\_mhz = \frac{ext\_clk\_freq\_mhz \times pll\_multiplier}{pre\_pll\_clk\_div \times op\_sys\_clk\_div \times op\_pix\_clk\_div}$$

7.1.9 Framerate

The framerate of the array readout and therefore the output framerate is governed by the line length, frame length and the video timing pixel clock frequency.

- Line length is specified as a number of pixel clocks, line_length_pck.
- Frame length is specified as a number of lines, frame_length_lines.
- Video timing pixel clock is specified in MHz, vt_pix_clk_freq_mhz.

The equation relating the framerate to the Line length, frame length and the video timing pixel clock frequency is given below:.

$$\text{Framerate} = \frac{\text{vt\_pix\_clk\_freq\_mhz}}{\text{line\_length\_pck} \times \text{frame\_length\_lines}}$$

The maximum frame rate that can be achieved in profile 0 for RAW10 is 18 fps with CSI2 single lane. *Table 34* provides an example of frame timing for RAW10 mode for 18 fps.

Table 34. External clock frequency example - 5.0 Mpixel RAW10 18 fps (CSI-2 single lane)

Ext clk freq	Pre-PLL clk div	PLL multiplier	VT sys clk div	VT pixel clk div	VT pixel clock	OP sys clk div	OP pixel clk div	OP pixel clock	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
9.60	1	208	2	10	99.84	2	10	99.84	2750	1976

Table 35 provides an example of frame timing for 10-8 mode for 23 fps with CSI-2 single lane.

Table 35. External clock frequency examples - 5.0 Mpixel 10-8 23 fps (CSI-2 single lane)

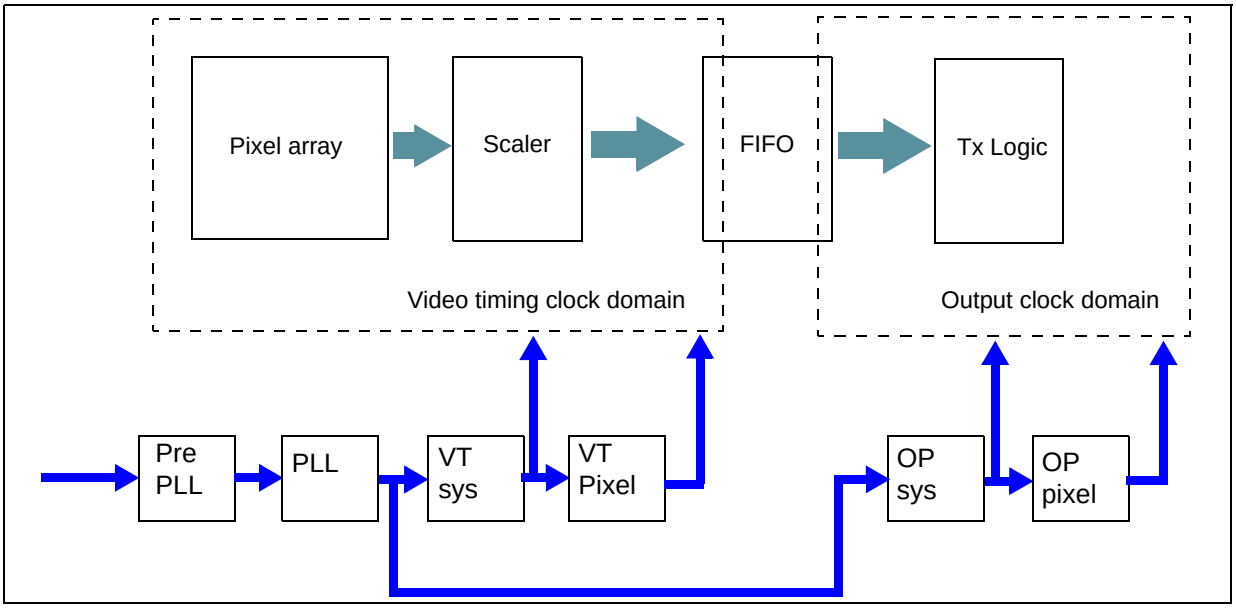
Ext clk freq	Pre-PLL clk div	PLL multiplier	VT sys clk div	VT pixel clk div	VT pixel clock	OP sys clk div	OP pixel clk div	OP pixel clock	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
9.60	1	208	2	8	124.8	2	8	124.8	2750	1976

7.1.10 Derating

To provide a wide range of data rate reduction options, the full image scaler is able to reduce the data and therefore data rates in both the horizontal and vertical directions. In the VS6955CA this is achieved by the use of a FIFO between video timing and output clock domains.

It is therefore necessary for the host to configure the OP clock domain to ensure that the FIFO neither over flows or under flows.

Figure 23. Timing block diagram



Derating shows the difference between the video timing domain and the output clock domain.

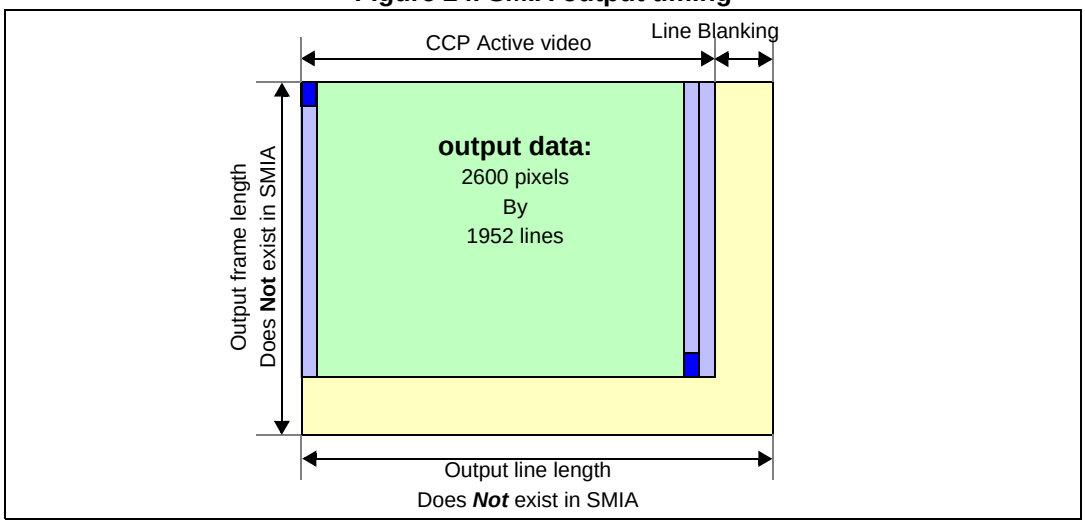
$$\text{derating} = \frac{\text{op\_sys\_clk\_div} * \text{op\_pix\_clk\_div}}{\text{vt\_sys\_clk\_div} * \text{vt\_pix\_clk\_div}}$$

FIFO

The FIFO is used to implement the data rate reduction required for profile 1 operation.

The concept of an output frame length and a line length for the output timing domain does not exist for SMIA devices such as the VS6955CA. This is a result of the FIFO input data patterns being different depending on scaling factor and if the data is co-sited or Bayer sampled, which results in variable interframe and interline blanking time between lines and between frames.

Figure 24. SMIA output timing



7.2 Image and video size capabilities

The VS6955CA supports various video modes ranging from VGA@120 fps to HD formats like 3.8 Mpixel @ 42 fps, 1080p30 and 720p30.

Table 36. Examples of video mode capabilities

	Resolution	FPS	Mode	Format
Full FOV	2600 x 1952	23 (max)	5 Mpixel 4:3	RAW8, 10/8
	2600 x 1952	18 (max)	5 Mpixel 4:3	RAW10
HD video capture	1080p	41 (max)	16:9 (full horizontal + vertical crop)	RAW8, 10/8
	1080p	33 (max)	16:9 (full horizontal + vertical crop)	RAW10
	720p	61 (max)	3.8 Mpixel 16:9 + Binning 2x2	RAW8, 10/8
VGA	VGA (648x488)	89(max)	5 Mpixel 4:3 with Binning 2x2 + 2x2 subsampling	RAW8, 10/8

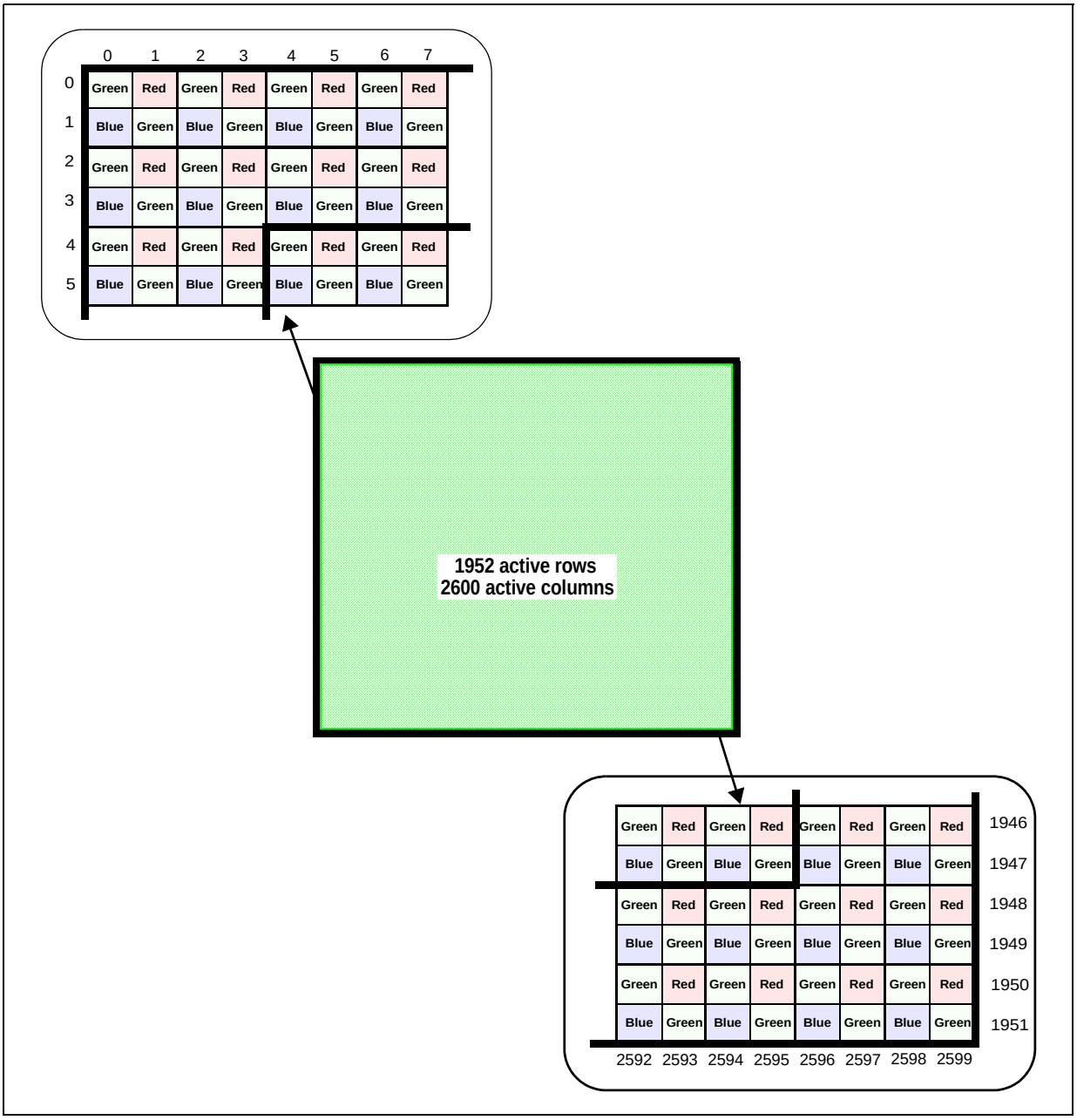
7.3 Bayer pattern

The three color (Red, Green, Blue) filters are arranged over the pixel array in a repeated 2 x 2 arrangement known as the Bayer Pattern. When the pixel array is read, the output order of red, green, blue depends on the settings of vertical flip and horizontal mirror.

Figure 25 shows the read-out order for the default settings of vertical flip and horizontal mirror both turned off. Vertical flip changes the first line to be output from a green/red line to a blue/green line and horizontal mirror changes the sequence within a line, for example, green/red to red/green.

As shown in *Figure 25*, the first pixel to be readout from the imaging array is green followed by red.

Figure 25. Bayer pattern



7.4 Image compression

The objective of image compression is to reduce the required bandwidth in transmission between the sensor and the host.

The key features of the DPCM/PCM compression algorithm are:

- visually lossless
- low cost implementation (no line memories are required)
- fixed rate compression

The 10-bit to 8-bit DPCM/PCM image compression algorithm is supported by VS6955CA. 10-bit to 8-bit compression has the additional advantage that one pixel value equals one byte of data.

The level of compression is controlled through the CSI_data_format register. The same register is also used to enable and disable compression.

The compression_mode register is used to select which compression algorithm is used. Currently only the DPCM/PCM technique is supported. Therefore the value of this register is always 0x01.

The compression_capability register tells the host whether a sensor does or does not have compression and if it has compression then what is the compression technique. Currently only the DPCM/PCM technique is supported.

Also refer to section 10 of the SMIA1.0 specification document.

7.5 Exposure and gain control

VS6955CA does not contain any form of automatic exposure control. To produce a correctly exposed image the integration period and analogue gain for the pixels must be calculated by an exposure control algorithm implemented externally. The parameters are then written to the VS6955CA through the CCI interface.

The exposure control parameters available on VS6955CA are:

- fine integration time
- coarse integration time
- analog gain
- digital gain

The exposure control parameter registers are defined in *Section 4.2.6: Integration and gain registers [0x0200 to 0x0215] on page 30*.

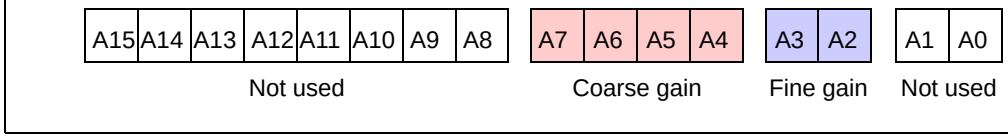
Integration time and analogue gain capability registers should be used to determine the exposure control parameter limits for a given video timing configuration. See Section 6.7 of the SMIA 1.0 part 1 specification for more information on how to interpret the integration and gain capability registers and how to calculate exposure and gain limits.

7.5.1 Analogue gain model

VS6955CA only supports the single global analogue gain mode. VS6955CA has a 16-bit register (0x0204 and 0x0205) to control analogue gain.

Figure 26 shows the way the analogue gain bits are used for VS6955CA. **Use only Coarse Gain bits for standard 1/x functionality**.

Figure 26. Analogue gain register format



The following generic equation describes VS6955CA coarse gain behavior specified by the analogue gain description registers 0x008A to 0x0093:

$$gain = c0/(m1 \cdot x + c1)$$

where:

m1 = -1

c0 = 256

c1 = 256

Table 37 specifies the valid analogue gain values for VS6955CA.

Table 37. Analogue gain control

Gain value (0x0204/0x0205)	Coarse gain code [A7:A4]	Coarse analogue gain	Fine gain code [A3:A2]	Fine analogue gain
0x0000	0000	0.0 dB (x1.00)	00	N/A
0x0010	0001	0.6 dB (x 1.07)	00	N/A
0x0020	0010	1.1 dB (x1.14)	00	N/A
0x0030	0011	1.8 dB (x1.23)	00	N/A
0x0040	0100	2.5 dB (x1.33)	00	N/A
0x0050	0101	3.2 dB (x1.45)	00	N/A
0x0060	0110	4.1 dB (x1.60)	00	N/A
0x0070	0111	5.0 dB (x1.78)	00	N/A
0x0080	1000	6.0 dB(x2.00)	00	N/A
0x0090	1001	7.2 dB (x2.29)	00	N/A
0x00A0	1010	8.5 dB (x2.66)	00	N/A
0x00B0	1011	10.1 dB (x3.20)	00	N/A
0x00C0	1100	12.0 dB (x4.00)	00	N/A
0x00D0	1101	14.5 dB (x5.33)	00	N/A
0x00E0	1110	18.1 dB (x8.00)	00	N/A
0x00E4	1110	fine ctrl	01	19.2 dB (x9.14)

Table 37. Analogue gain control (continued)

Gain value (0x0204/0x0205)	Coarse gain code [A7:A4]	Coarse analogue gain	Fine gain code [A3:A2]	Fine analogue gain
0x00E8	1110	fine ctrl	10	20.6 dB (x10.66)
0x00EC	1110	fine ctrl	11	22.1 dB (x12.80)
0x00F0	1111	24.1 dB (x16.00)	00	N/A

Also refer to section 6.3 of the SMIA1.0 specification document.

7.5.2 Digital gain

To help compensate for the relatively coarse analogue gain steps, VS6955CA contains a digital multiplier to “fill” in the missing steps. By mixing analogue and digital gain it is possible to implement 3% gain steps across the full 1x to 16x gain range

The details of the digital gain implementation are listed below:

- four individual 16-bit digital channel gains - one per Bayer channel
  - digital_gain_greenR (0x020E and 0x020F)
  - digital_gain_red (0x0210 and 0x0211)
  - digital_gain_blue (0x0212 and 0x0213)
  - digital_gain_greenB (0x0214 and 0x0215)
- the digital gain range for each channel is 1.000 to 1.96875 in steps of 0.03125 (1/32), that is, 5 fractional bits
  - digital_gain_min {0x1084:0x1085} = 0x0100 (1.00)
  - digital_gain_max {0x1086:0x1087} = 0x01F8 (1.96875)
  - digital_gain_step {0x1088:0x1089} = 0x0008 (0.03125)

7.5.3 Integration and gain parameter re-timing

The modification of exposure parameter (integration time, analog and digital gain) register values does not take effect immediately.

The exact time at which changes to certain parameters take effect is controlled both to ensure that each frame of image data produced has consistent settings and that changes in groups of related parameters can be synchronized.

A group of parameter changes is marked by the host using a dedicated Boolean control parameter, grouped_parameter_hold (register 0x0104). Any changes made to ‘retimed’ parameters while the grouped_parameter_hold signal is in the ‘hold’ state will be considered part of the same group. Only when the grouped_parameter_hold control signal is moved back to the default ‘no-hold’ state will the group of changes be executed.

8 Test modes

This chapter describes the test modes supported by the VS6955CA.

8.1 Full frame deterministic test patterns

Two types of full frame deterministic test patterns are defined. The Bayer test patterns are more suitable for some deterministic tests than real image data and are injected early in the sensor data path. The only exception to this is the PN9 test pattern that is intended to test sensor-host link integrity, the data in this pattern is not Bayer data and is injected into the data stream just prior to CSI framing.

Use of these full frame test patterns is controlled by the test_pattern_mode parameter (register 0x0600 and 0x0601). The available modes are:

- 0 – Normal operation (default)
- 1 – Solid color
- 2 – 100% color bars
- 3 – ‘Fade to gray’ color bars
- 4 – PN9

In both the default parameter state and in any undefined parameter states, normal array data should be output rather than a test pattern.

8.1.1 Solid color mode

In the solid color test pattern mode, all active pixel data is replaced with fixed Bayer test data that is defined by the four 16-bit test data color parameters registers (0x0602 to 0x609). These are 10-bit values.

8.1.2 100% color bars pattern mode

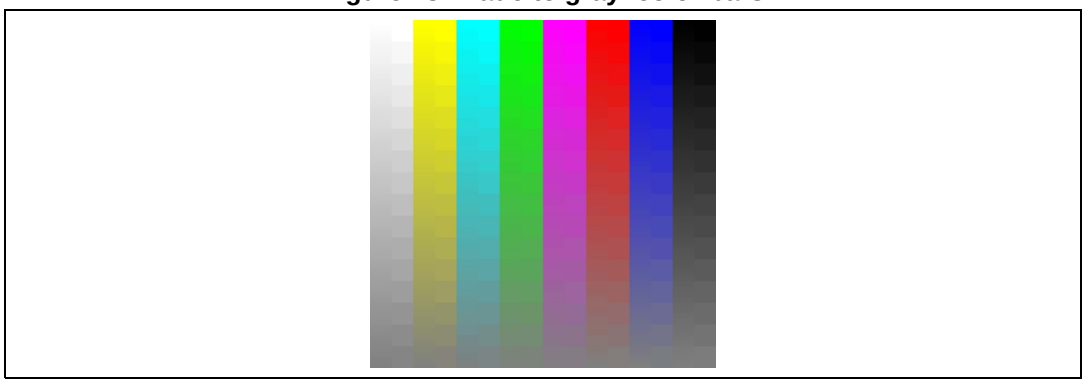
In the ‘100% color bar’ test pattern mode, all pixel data is replaced with a Bayer version of an 8-bar color bar pattern. In each bar all pixels are either 0% or 100% full scale (for example, 100/0/100/0 bars).

Figure 27. 100% color bars

8.1.3 ‘Fade to gray’ color bar mode

In the ‘fade to gray’ color bar test pattern mode, all pixel data is replaced with a color bar that fades vertically from 100% color bars to mid gray. The ‘fade to gray’ color bar pattern is designed to exercise more of the color space than 100% bars whilst still requiring minimal hardware overhead. *Figure 28* gives an indication of the pattern (although the pattern is generated as Bayer data).

Figure 28. ‘Fade to gray’ color bars



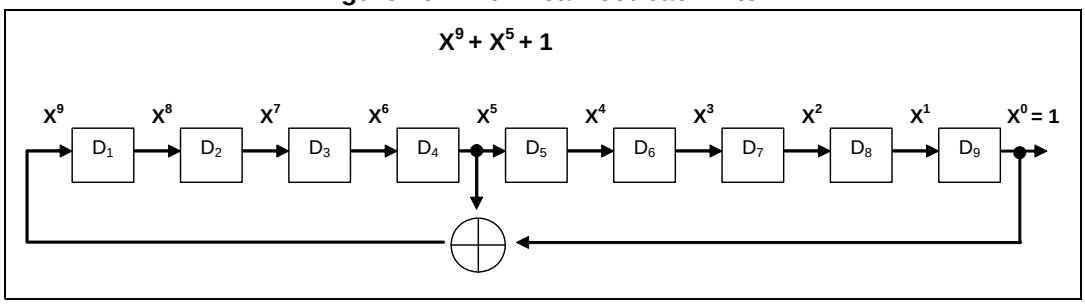
The pattern is made up of eight vertical bars that fade vertically from one of the 100% color bar colors towards a mid-gray at the bottom. The bars follow the same order as standard color bars. Each of the bars is sub-divided vertically into a left hand side that contains a smooth gradient and a right hand size that contains a quaintest version.

The aim of the quaintest portion is to offer areas of flat-field Bayer data that should be large enough to result in known data values even after demosiac (independently of the demosiac algorithm). To ensure maximum dynamic range in the quaintest data, the LSBs of the quaintest data is generated by copying the MSBs of the unquantized data (rather than forcing them to 0). The pattern may roll over and repeat if the frames is long enough.

8.1.4 PN9 mode

In the ‘PN9’ test pattern mode, all data on all lines between FS and LS code and the LE or FE code is replaced with data from internally generated 511-bit pseudo-random ‘PN9’ sequence.

Figure 29. PN9 linear feedback filter



The PN9 test pattern is included to ease testing of sensor-link integrity (for example, measurement of bit error rate). The standard PN9 linear feedback shift register with polynomial X^9+X^5+1 in Fibonacci-type notation is shown in *Figure 29*. The PN9 sequence

generator is reset at the start of the frame, the sequence is then in a known state (0x1FF) at the first replaced pixel of each frame.

Note: The frame format descriptors do not correctly report the frame format in this mode.

8.2 Test cursors

In addition to generation of full frame deterministic test patterns, VS6955CA sensor can superimpose simple ‘cursors’ on the image. These cursors don’t appear on the PN9 test mode.

The cursors are generated by replacing Bayer pixel data with fixed Bayer data within narrow vertical and/or horizontal bands of the image. Injection of the test cursors must be arranged such that the cursors can be superimposed on top of the full frame test patterns as well as array image data.

Two cursors are defined, one vertical cursor and one horizontal. The four parameters described in *Table 38* are used to control the cursors. The position and width of each cursor can be controlled manually. Each cursor can be inhibited by setting its width parameter to zero. A value of 0xFFFF in register vertical_cursor_position switches the vertical cursor into automatic mode where it automatically advances every frame (the initial position of the automatic cursor is undefined). The first pixel of the cursor replaces the pixel data at the horizontal_cursor_position-1 pixel. the width of the cursor can incremented in steps of one. The maximum valid value for horizontal_cursor_position and vertical_cursor_position is the associated x output size.

Table 38. Registers used to define the output data

Index	Byte	Register name
0x060A	Hi	horizontal_cursor_width
0x060B	Lo	
0x060C	Hi	horizontal_cursor_position
0x060D	Lo	
0x060E	Hi	vertical_cursor_width
0x060F	Lo	
0x0610	Hi	vertical_cursor_position
0x0611	Lo	

The four registers used to define the output data in solid color mode also define the Bayer data used for the image cursors.

9 Defect categorization

9.1 Pixel defects

9.1.1 Overview

Pixel defect density measures the average number of defective pixels per color channel under “Diffuse” and “Dark” conditions, refer to *Table 39: Pixel defect specification*.

Table 39. Pixel defect specification

	Reference Area	Threshold
Dark	Full Channel	64 codes
Light	9x9	+/-12%

9.1.2 Defect detection

Defect detection is performed in two parts; once in diffuse conditions and once in dark conditions, as defined in *Table 40: Image settings*. The methods used for these differ to account for the differing conditions and for the difference in the failure modes detected by each.

Table 40. Image settings

	Dark	Diffuse
Exposure	100ms	33ms(1)
Analog gain	x8	x1
Digital gain	x1	x1

1. Image exposure targets 75% of full-scale deflection in the green channels at the centre of the image.

In both the dark and light cases, two images are averaged pixel-by-pixel in order to reduce the impact of temporal noise. Detection is performed individually on the four colour channels.

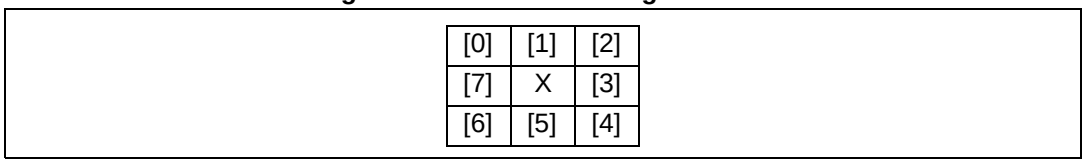
“Dark defects” are those which appear too bright in a dark image, either due to dark current or a stuck-at fault. These are measured by thresholding against the difference between the actual pixel value and the local or full-frame average (this is dependent on the uniformity of the dark image). The threshold is defined such that it can identify gain error above the normal noise distribution of photon shot noise and sensor noise and so pixels that deviate by more than the dark threshold are declared defective.

“Light defects” tend to be caused by small foreign material or damage to the die surface. The diffused image is processed to remove very low frequency variation by gaining the image towards the centre peak value for each colour channel, mimicking the lens shading gains applied in the application. Pixels that deviate from the local average by more than the light threshold in either direction are defined as defective. The 64-code pedestal is not removed from this relative calculation.

9.1.3 Defect categorisation: Single pixels

Figure 30. shows the numbering of the neighboring pixels in a 3x3 grid within a single color channel; all the pixels will either be red, green-red, green-blue or blue. The pixel under test is X. If a pixel under test is on the edge on the image, the array is reduced to its existing neighbor pixels (i.e. the top-left pixel uses only a 2x2 array).

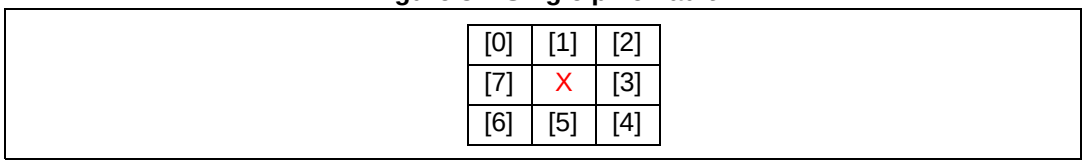
Figure 30. Pixel numbering notation



A single pixel fail is defined as a failing pixel with no adjacent failing pixels in the neighboring pixels 0 to 7. A single pixel fail can be a stuck at white, where the output of the pixel is permanently saturated regardless of the level of incident light and exposure level, a stuck at black where the pixel output is zero regardless of the level of incident light and exposure level (major fail) or simply a pixel that differs from its immediate neighbors by more than the test threshold (minor fail).

In the example in *Figure 31*, shown, we assume that pixel X is a failing pixel. For this pixel to be categorised as a single pixel fail, the pixels at positions [0], [1], [2], [3], [4], [5], [6] and [7] must be "good" pixels that pass final test. The test program will pass a sensor with up to the defined limit of single pixel faults per colour channel.

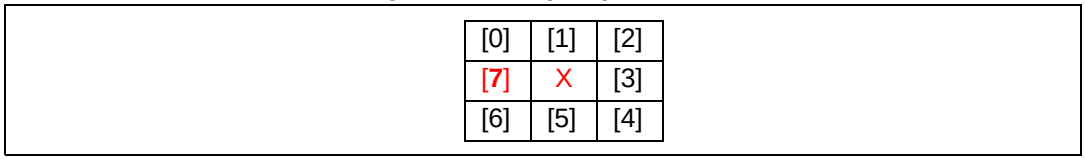
Figure 31. Single pixel fault



9.1.4 Defect categorisation: Couplets

A couplet is formed by a failing pixel at X neighboring a failing pixel at position [0] or [1] or [2] or [3] or [4] or [5] or [6] or [7], such that there is a maximum of 2 failing pixels from the group of 9 pixels. The example shown in *Figure 32: Couplet pixel fault* has the centre pixel and the pixel at position [7] failing the test criteria.

Figure 32. Couplet pixel fault



This product has on-chip mapped couplet correction capable of storing up to 14 defect locations. No unmapped couplets are allowed in a full resolution image.

9.1.5 Defect categorisation: Clusters and blobs

If pixel X is a failure and between 2 and 7 of the surrounding pixels are also defective, then the pixels are categorised as a cluster. If all nine pixels are defective then the failure is classified as a blob. Neither clusters nor blobs are allowed.

9.2 Mapped couplet correction (Bruce filter)

The mapped couplet defect correction filter is designed to intelligently correct the first defect in a couplet thereby changing a couplet into a single pixel defect. Single pixel correction is achieved by the host (coprocessor, MMP or baseband). The mapped couplet correction filter only operates in full resolution mode.

The mapped couplet correction filter requires exact coordinate information for each of the couplets to be repaired. The couplet coordinates are stored in non-volatile-memory (NVM) during production test.

10 Electrical characteristics

10.1 Absolute maximum ratings

Table 41. Absolute maximum ratings

Symbol	Parameter	Minimum	Maximum	Unit
$VDIG_{MAX}$	Digital power supply	-0.5	2.2	V
$VANA_{MAX}$	Analog power supply	-0.5	3.2	V
V_{IHMAX}	CCI signals, system clock input	-0.5	2.2	V
T_{STO}	Storage temperature	-40	+85(1)	°C
V_{ESD}	Electrostatic discharge model Human body model Charge device model(2)	 -2.0 -250	 2.0 250	 kV V

1. This is a maximum long term standard storage temperature, see soldering profile for short term high temperature tolerance.
2. CDM tests are performed in compliance with JESD22-C101D.

Caution: Stresses above those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

10.2 Operating conditions

Table 42. Operating conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Voltage					
VDIG	Digital power supply	1.62	1.80	1.98	V
VANA	Analog power supply	2.6	2.80	2.9	V
Temperature					
T_{AS}	Temperature (storage)(1)	-40	-	+85	°C
T_{AF}	Temperature (functional operating)(2)	-30	-	+70	°C
T_{AN}	Temperature (normal operating)(3)	-25	-	+55	°C
T_{AO}	Temperature (optimal operating)(4)	+5	-	+40	°C
T_{AT}	Temperature (test)(5)	+21	-	+25	°C

1. Device has no permanent degradation.
2. Device is electrically functional.
3. Device produces ‘acceptable’ images.
4. Device produces optimal optical performance.
5. 100% tested parameters are measured at this temperature.

10.3 DC electrical characteristics

In this section, typical values are quoted for nominal voltage, process and temperature and maximum values are quoted for worst case conditions (process, voltage and functional temperature) unless otherwise specified.

10.3.1 Power supply - VDIG, VANA

Table 43. Power supply - VDIG, VANA

Parameter	Digital		Analog		Unit
	Typical	Max	Typical	Max	
Hardware standby	10	45	3	35	µA
5.0 Mpixel 4:3 streaming(1):	30	40	68	90	mA

1. Profile 0, 15 fps, CSI-2 single lane, 10-10 data, 9.6 MHz external clock.

10.3.2 CCI interface

Table 44. CCI interface

Symbol	Parameter	Minimum	Maximum	Unit
V_{IL}	Low level input voltage	-0.5	0.3*VDIG	V
V_{IH}	High level input voltage	0.7*VDIG	VDIG+0.5	V

Table 44. CCI interface (continued)

Symbol	Parameter	Minimum	Maximum	Unit
V_{OL}	Low level output voltage(1)	0	0.2*VDIG	V
V_{OH}	High level output voltage	0.8*VDIG	VDIG	V
I_{IL}	Low level input current	-	-10	µA
I_{IH}	High level input current	-	10	µA

1. 3 mA sink current.

10.4 AC electrical and timing characteristics

In this section, typical values are quoted for nominal voltage, process and temperature and maximum values are quoted for worst case conditions (process, voltage and functional temperature).

10.4.1 Power supply (peak current) - VDIG, VANA

The peak current (in-rush) consumption of the sensor module is defined as any current pulse >= 10µs. The duty cycle of the peak to the low part of the current profile is 33% with a worst-case period of 500 µs.

Table 45. In-rush current - VDIG, VANA (CSI-2)

Parameter	Digital		Analog		Unit
	Typical	Maximum	Typical	Maximum	
Boot clock peak current(1)	80	100	200	230	mA
Start streaming current(2)	80	100	200	210	mA
Stop streaming current(3)	80	105	100	140	mA

1. This corresponds to the transient current when the module is powered up and the sensor is being set to SW_Standby mode. Maximum value is given for maximum supply voltages and 70°C ambient temperature. Typical value is for 25°C ambient temperature and supply voltages set to nominal value.
2. When the sensor is changed from software standby to streaming mode. Maximum value is given for maximum supply voltages and 70°C ambient temperature. Typical value is for 25°C ambient temperature and supply voltages set to nominal value.
3. When the sensor is changed from streaming to software standby. Maximum value is given for maximum supply voltages and 70°C ambient temperature. Typical value is for 25°C ambient temperature and supply voltages set to nominal value.

10.4.2 System clock - EXTCLK

Table 46. System clock

Symbol	Parameter	Minimum	Maximum	Unit
V_{CL}	DC coupled square wave low level	-0.5	0.3*VDIG	V
V_{CH}	DC coupled square wave high level	0.7*VDIG	VDIG+0.5	V
f_{EXTCLK}	Clock frequency input	6.0 - 1%(1)	27 + 1%(1)	MHz

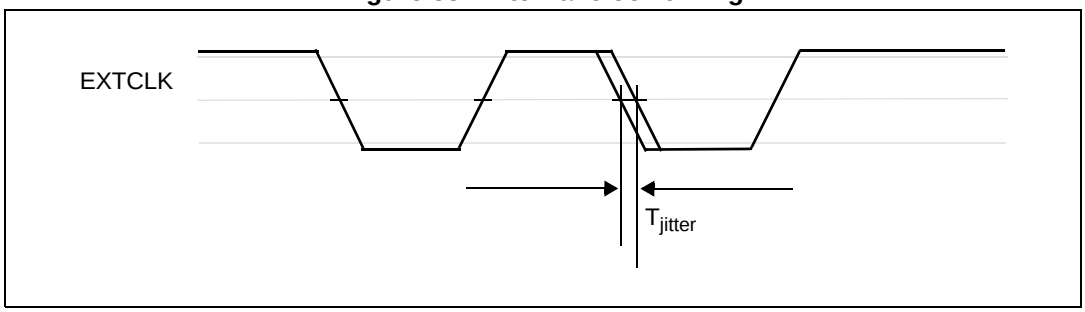
1. Nominal frequencies are 6.0 to 27 MHz with a 1% centre frequency tolerance.

10.4.3 EXTCLK - timing characteristics

Table 47. External clock timing characteristics

Symbol	Parameter	Minimum	Maximum	Unit
T_{jitter}	Input clock jitter	-	100	ps

Figure 33. External clock timing



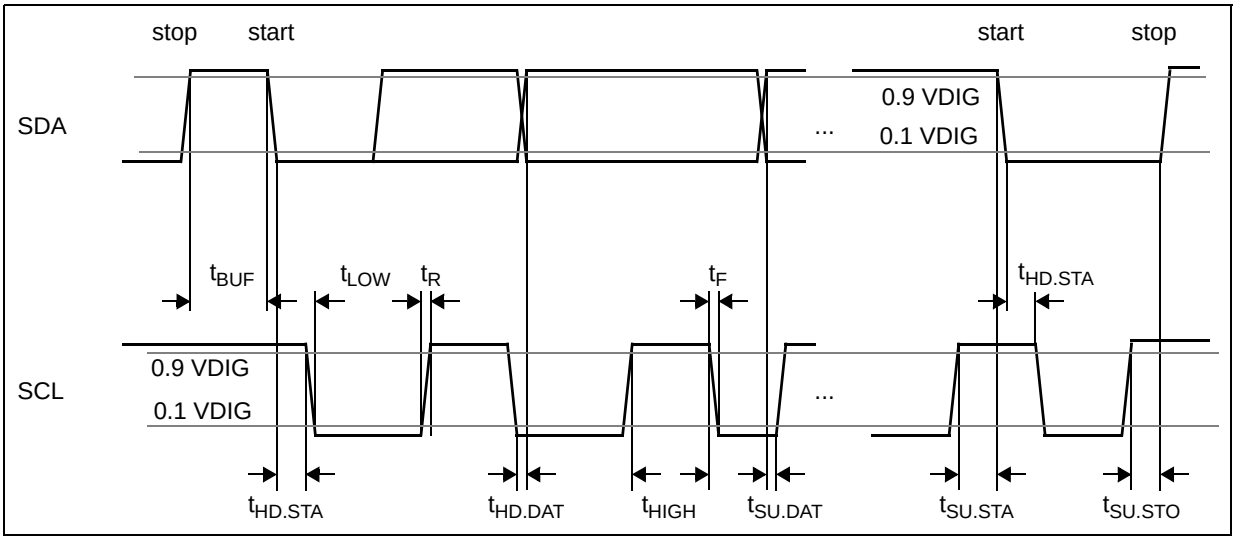
10.4.4 CCI interface - timing characteristics

Table 48. CCI interface timing characteristics

Symbol	Parameter	Minimum	Maximum	Unit
t_{SCL}	SCL clock frequency	0	400	kHz
t_{LOW}	Clock pulse width low	1.3	-	ms
t_{HIGH}	Clock pulse width high	0.6	-	ms
t_{BUF}	Bus free time between transmissions	1.3	-	ms
$t_{HD.STA}$	Start hold time	0.6	-	ms
$t_{SU.STA}$	Start set-up time	0.6	-	ms
$t_{HD.DAT}$	Data in hold time	0	0.9	ms
$t_{SU.DAT}$	Data in set-up time	100	-	ns
t_R	SCL/SDA rise time	20+0.1 C_b(1)	300	ns
t_F	SCL/SDA fall time	20+0.1 C_b(1)	300	ns
$t_{SU.STO}$	Stop set-up time	0.6	-	ms
Ci/o	Input/output capacitance (SDA)	-	8	pF
Cin	Input capacitance (SCL)	-	6	pF

1. Cb = total capacitance of one bus line in pF

Figure 34. CCI AC characteristics



All timings are measured from either 0.1 VDIG or 0.9 VDIG.

For further information on the CCI interface, refer to the following specification documents: MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2).

10.4.5 CSI interface - DATA+, DATA-, CLK+, CLK-

Table 49. CSI interface - DATA+, DATA-, CLK+, CLK- characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{OD}	HS transmit differential voltage(1)	140	200	270	mV
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
t_r and t_f	20% to 80% rise time and fall time	150		0.3UI(2)	ps

1. Value when driving into load impedance anywhere in the Z_{ID} range (80 to 125Ω).
2. UI is equal to 1/(2*fh) where fh is the fundamental frequency of the transmission for a certain bit rate. For example, for 600 Mbps fh is 300 MHz.

Note: For further information on the D-PHY, refer to the following specification document: MIPI Alliance Standard for D_PHY.

11 Mechanical

Figure 35. VS6955CA outline drawing - 1 of 3 - All dimensions in mm

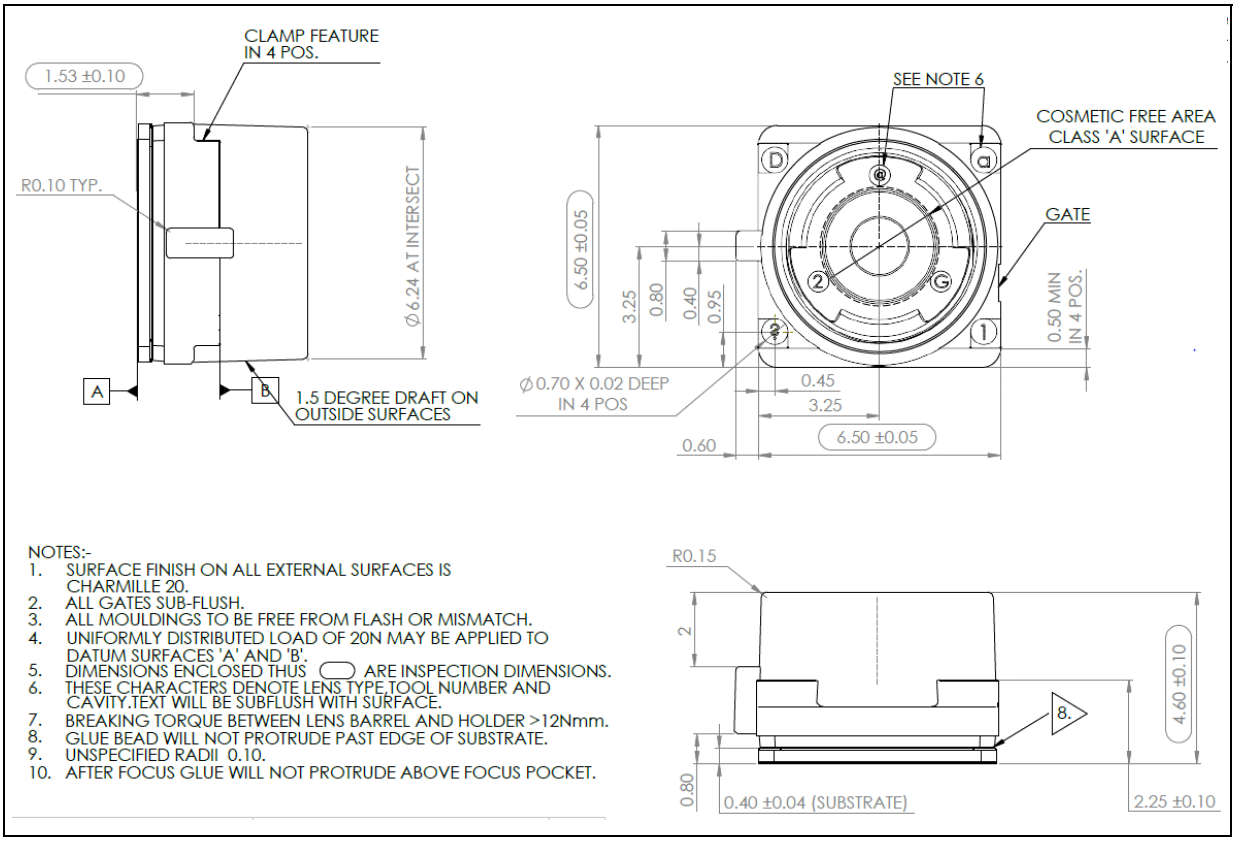
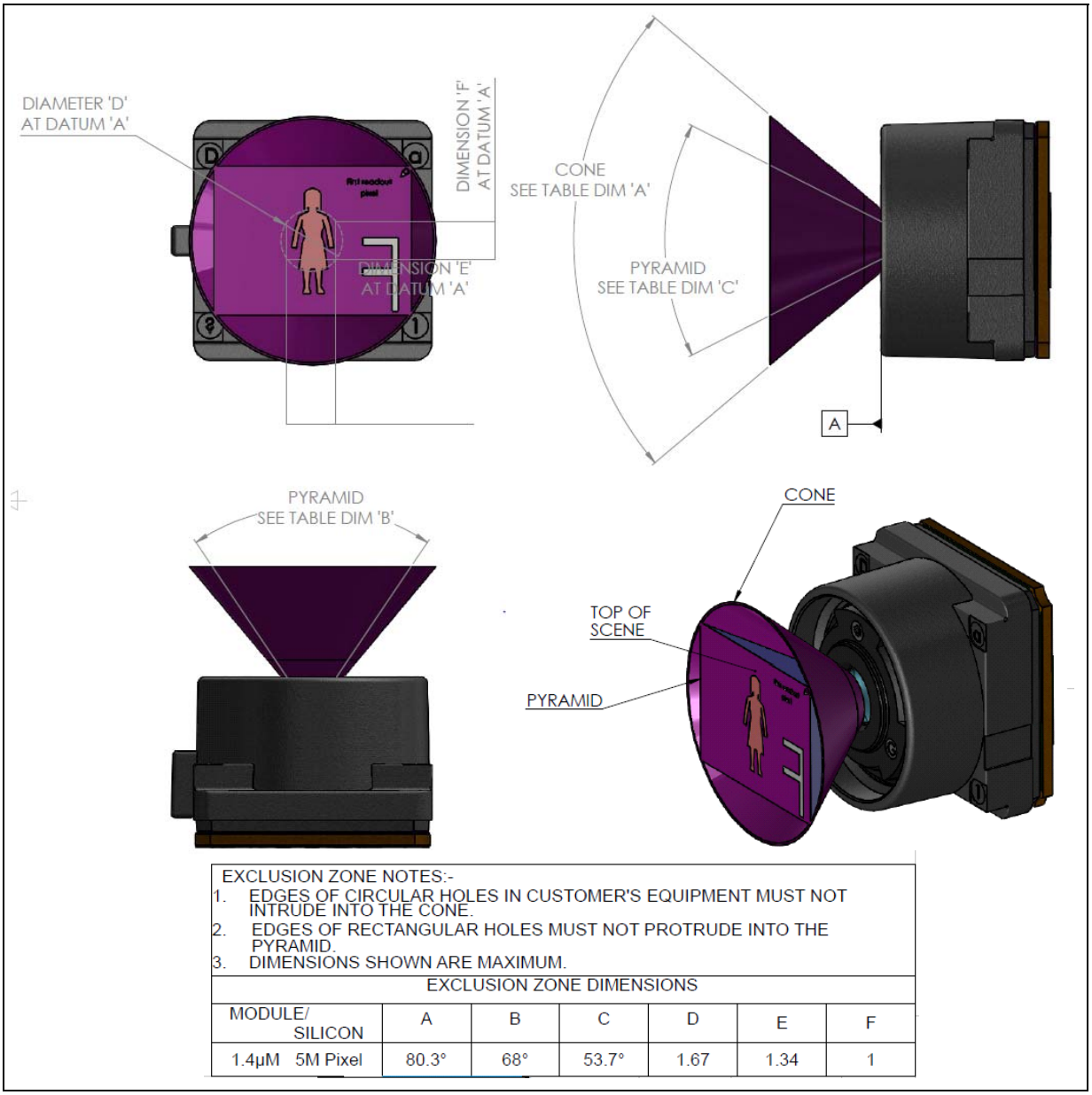


Figure 36. VS6955CA outline drawing - 2 of 3 - All dimensions in mm



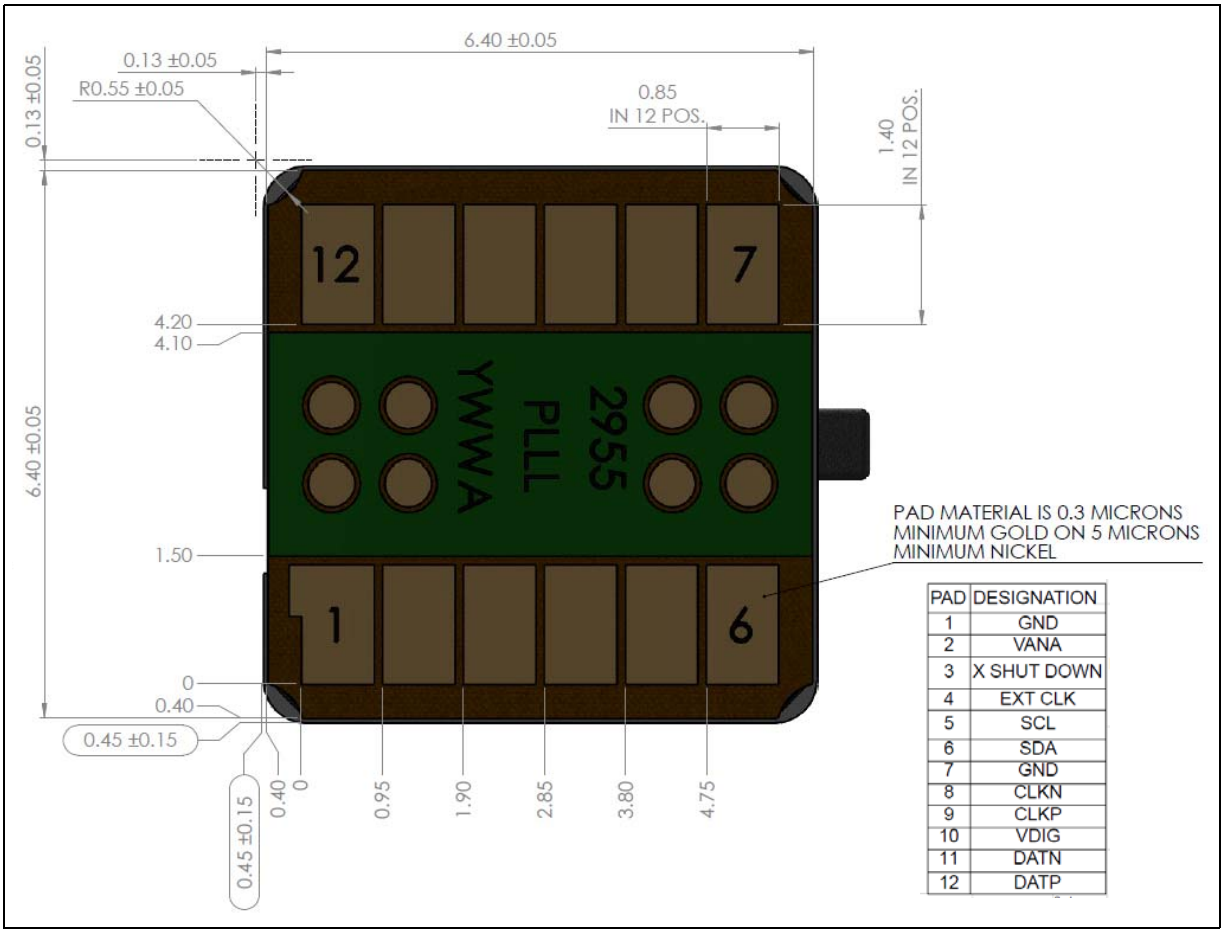
EXCLUSION ZONE NOTES:-

1. EDGES OF CIRCULAR HOLES IN CUSTOMER'S EQUIPMENT MUST NOT INTRUDE INTO THE CONE.
2. EDGES OF RECTANGULAR HOLES MUST NOT PROTRUDE INTO THE PYRAMID.
3. DIMENSIONS SHOWN ARE MAXIMUM.

EXCLUSION ZONE DIMENSIONS

MODULE/ SILICON	A	B	C	D	E	F
1.4µM 5M Pixel	80.3°	68°	53.7°	1.67	1.34	1

Figure 37. VS6955CA outline drawing - 3 of 3 - All dimensions in mm



PAD	DESIGNATION
1	GND
2	VANA
3	X SHUT DOWN
4	EXT CLK
5	SCL
6	SDA
7	GND
8	CLKN
9	CLKP
10	VDIG
11	DATN
12	DATP

12 Cosmetic inspection

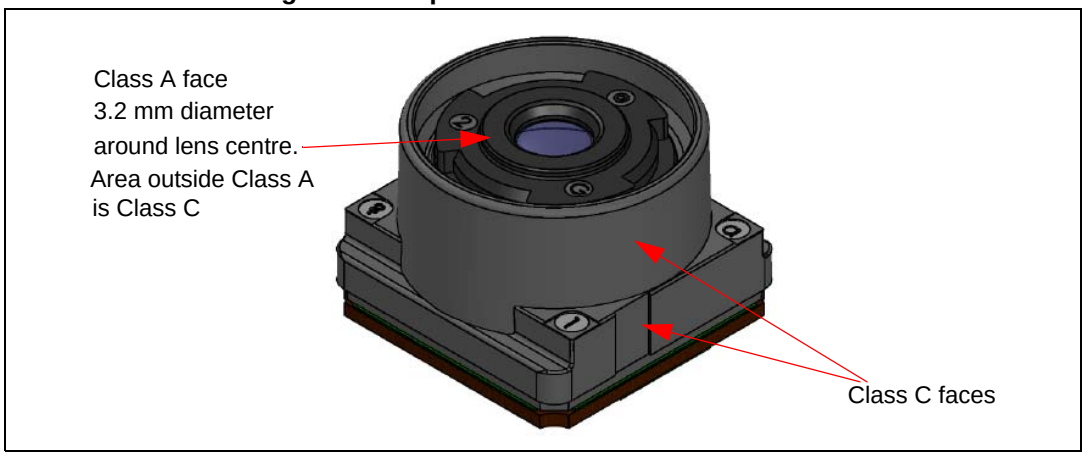
The cosmetic inspection criteria used for the camera module is based on the demerit system to gauge the length and width of imperfections. It should be noted that the depth or height of an imperfection **does not** affect the form, fit or function of the camera module particularly with regard to the camera socket on the phone platform.

Areas of the camera module are given a surface class of A, B or C. This is detailed in *Table 50* and *Figure 38*.

Note: The camera module comprises of class A and C surfaces, none are class B.

The camera module is inspected, in normal lighting conditions using the naked eye at 30 cm, for scratches, chips, marks, foreign material inclusions and discoloration. The length and width of these imperfections are measured and awarded demerit points. If there is more than one imperfection, the demerit points are accumulated.

Figure 38. Inspection areas on the VS6955CA



Cosmetic inspection should be carried out using the naked eye at 30 cm in normal office lighting. Scratches and marks are permitted on the shield.

Refer to the outline drawing for the definition of the cosmetic class A surface.

Table 50. Surface class definitions

Surface class	Surface description	Reject demerit level
'A'	Primary surface exposed to direct view in ordinary use by customer – top face only.	1 or more
'B'	Secondary surface exposed, but not in direct view in ordinary use. No class B surfaces for this camera module.	6 or more
'C'	Surface not visible in ordinary use – all other surfaces other than A above.	10 or more

The demerit system covers - scratches, chips, marks, foreign material inclusions, discoloration of parts and is detailed in *Table 51*. The depth or height of an imperfection **does not** affect the form, fit or function of the camera module particularly with regard to the camera socket on the phone platform.

Table 51. Demerit points

Length/width of imperfection	Demerit points
>3.5mm	8
2.5mm - 3.5mm	6
2.0mm - 2.5mm	5
1.5mm - 2.0mm	4
1.0mm - 1.5mm	3
0.8mm - 1.0mm	2
0.4mm - 0.8mm	1
< 0.4mm	0

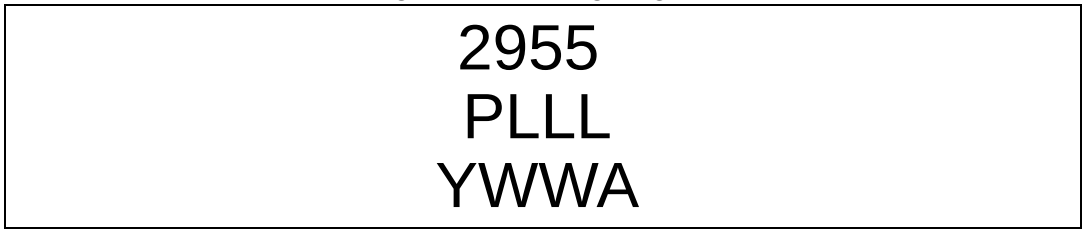
Examples of pass/fail

Table 52. Examples of pass/fail

Surface class	Imperfection	Pass/Fail
A	0.3mm scratch, 0 demerit	Pass
A	0.5mm scratch, 1 demerit	Fail
C	3.4mm mark, 6 demerits	Pass
C	0.9mm scratch, 2 demerits; 1.4mm mark, 3 demerits - Total 5 demerits	Pass
C	2 * 2.6mm scratches, 2 * 6 demerits = 12 demerits	Fail

13 Packaging and delivery

Figure 39. Marking diagram



Substrate marking codification

Line one: Product code

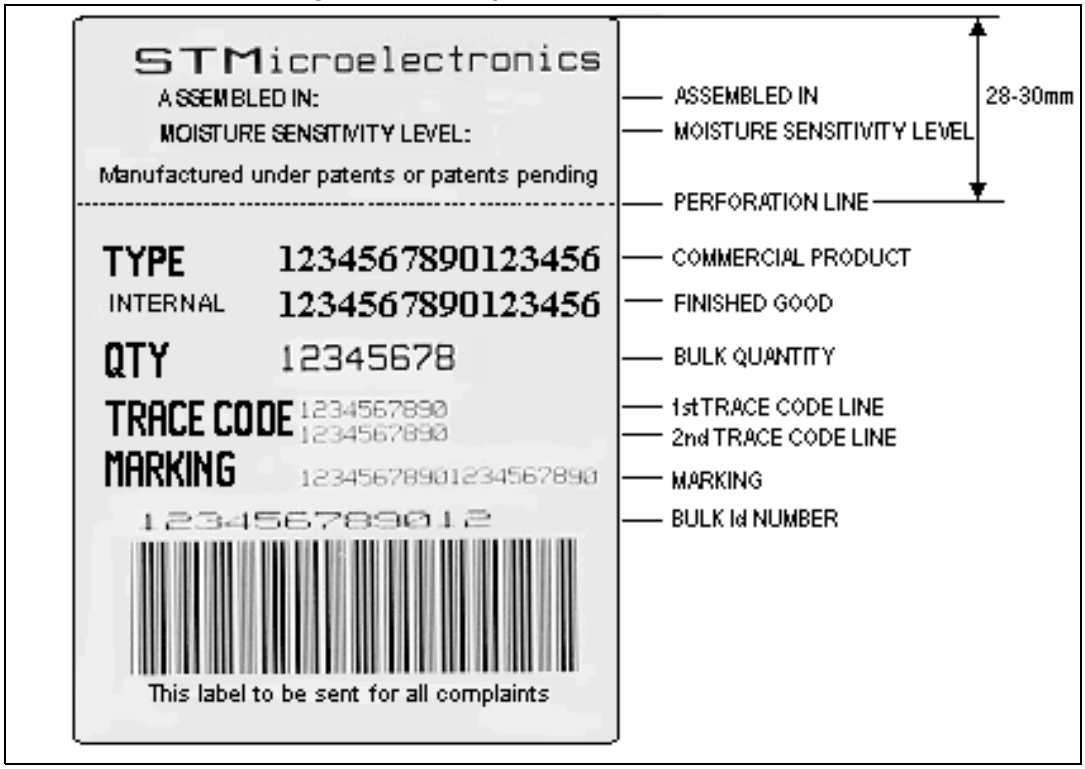
Line two: P is the assembly plant
LLL is the B/E sequence

Line three: Y is the year
WW is the week number
A is the module revision

The VS6955CA packing is tape and reel.

Inner box labeling

Figure 40. Example of ST inner box label



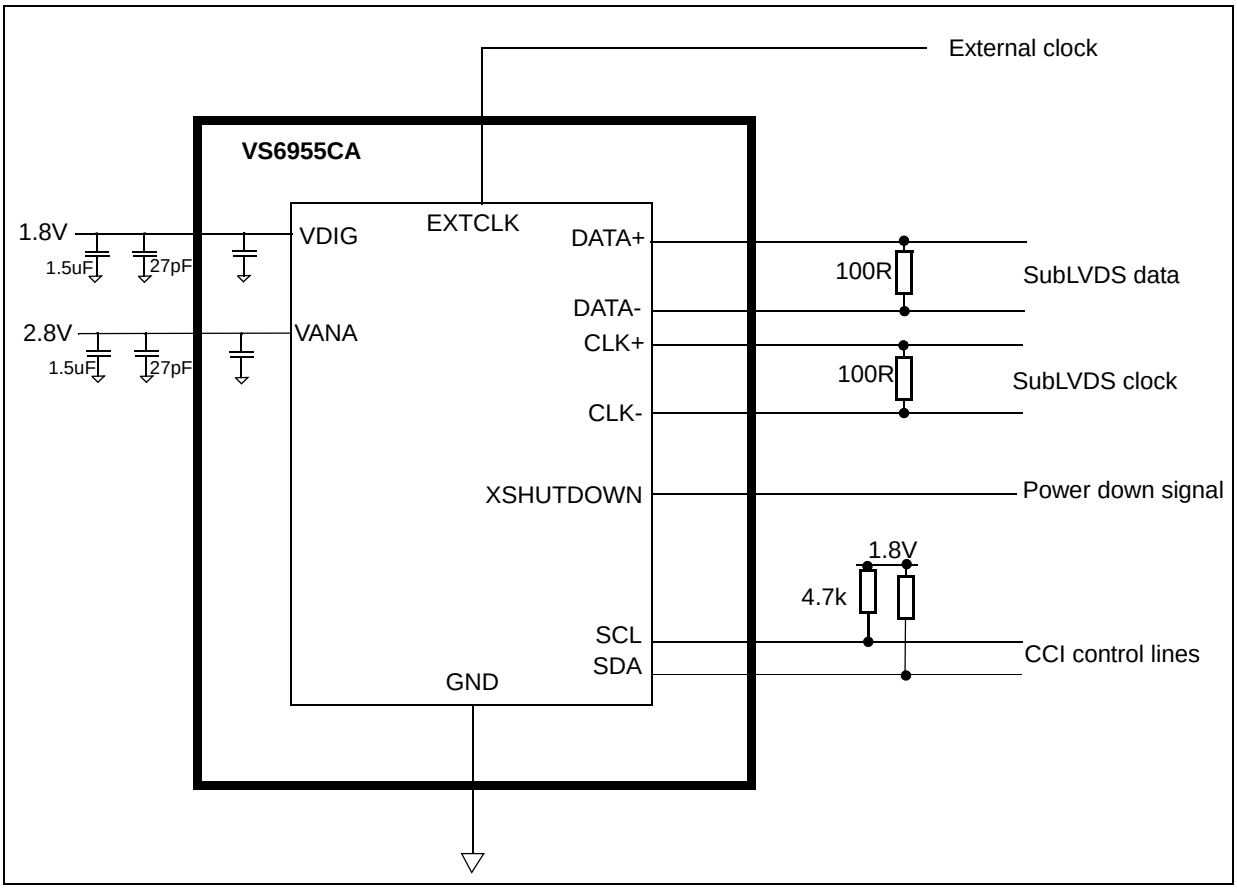
The labeling follows the ST standard packing acceptance specification.

The information on the inner box label is the following:

- assembly site
- moisture sensitivity level (Jedec Level 0)
- order code
- quantity
- trace code
- marking (product name + NMP code for NMP products)
- QA number

14 Application

Figure 41. Mobile camera application



15 Acronyms and abbreviations

Table 53. Acronyms and abbreviations

Acronym/ abbreviation	Definition
CCI	Camera control interface
CMI	Camera module integrator
CSI	Camera serial interface
DPCM	Differential pulse code modulation
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOF	End of frame
EOT	End of transmission
FE	Frame end
fps	Frames per second
FS	Frame start
HS	High speed; identifier for operation mode
HS-RX	High speed receiver (low-swing differential)
HS-TX	High speed transmitter (low-swing differential)
I^2C	Inter ICbus
LE	Line end
LLP	Low level protocol
LS	Line start
LSB	Least significant byte
LP	Low power; identifier for operation mode
LP-RX	Low power receiver (large-swing single ended)
LP-TX	Low power transmitter (large-swing single ended)
LVDS	Low voltage differential signaling
Mbps	Megabits per second
MIPI	Mobile industry processor interface
MSB	Most significant byte
PCK	Pixel clock
PCM	Pulse code modulation
PF	Packet footer
PH	Packet header
PI	Packet identifier
PT	Packet type

Table 53. Acronyms and abbreviations (continued)

Acronym/ abbreviation	Definition
PHY	Physical layer
PLL	Phase locked loop
RO	Read only
RW	Read/write
SCL	Serial clock (for CCI)
SDA	Serial data (for CCI)
SMIA	Standard mobile imaging architecture
SOT	Start of transmission
SOF	Start of frame
SSCG	Spread spectrum clock generator
SubLVDS	Sub-low voltage differential signaling
WDR	Wide dynamic reconstruction
ULPM	Ultra low power mode

16 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

17 Revision history

Table 54. Document revision history

Date	Revision	Changes
10-Sep-2015	1	Initial release.
02-Nov-2015	2	update *Table 9: Status registers [0x0000 to 0x001F]*