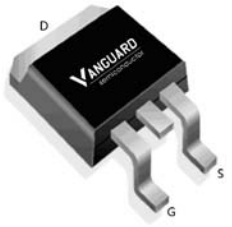
V_{DS}	80	V
$R_{DS(on),TYP}$@ V_{GS}=10V	6.4	mΩ
I_D	100	A

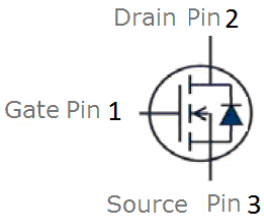
Features

- N-Channel，10V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=10V
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

Pb-Free RoHS HF Halogen-Free

TO-263





Part ID	Package Type	Marking	Tape and reel information
VS7580ATD	TO-263	7580ATD	1000pcs/Reel

Maximum ratings, at T_j=25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		80	V
I_S	Diode continuous forward current	T_C=25°C	100	A
I_D	Continuous drain current @V_{GS}=-10V	T_C=25°C	100	A
		T_C=100°C	71	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	400	A
EAS	Avalanche energy, single pulsed ②		245	mJ
P_D	Maximum power dissipation	T_C=25°C	150	W
V_{GS}	Gate-Source voltage		±25	V
T_{STG} T_J	Storage and operating temperature range		-55 to 175	°C
Thermal Characteristics				
$R_{\theta JC}$	Thermal Resistance-Junction to Case		1.0	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		62.5	°C/W

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @T_j= 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	80	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=75V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=75V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±25V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=10V, I_D=40A	--	6.4	9	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	3300	3900	4500	pF
C_{oss}	Output Capacitance		250	345	450	pF
C_{rss}	Reverse Transfer Capacitance		180	275	380	pF
R_g	Gate Resistance	f=1MHz	--	3.2	--	Ω
Q_g	Total Gate Charge	V_{DS}=40V,I_D=40A, V_{GS}=10V	--	61	--	nC
Q_{gs}	Gate-Source Charge		--	14	--	nC
Q_{gd}	Gate-Drain Charge		--	13	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=40V, I_D=40A, R_G=3Ω, V_{GS}=10V	--	11	--	nS
t_r	Turn-on Rise Time		--	11	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	39	--	nS
t_f	Turn-Off Fall Time		--	10	--	nS
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	--	0.9	1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=40A, V_{GS}=0V di/dt=300A/μs	--	19	--	nS
Q_{rr}	Reverse Recovery Charge			23		nC

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH,R_G = 25Ω, I_{AS} = 24A,V_{GS} =10V. Part not recommended for use above this value

③ Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

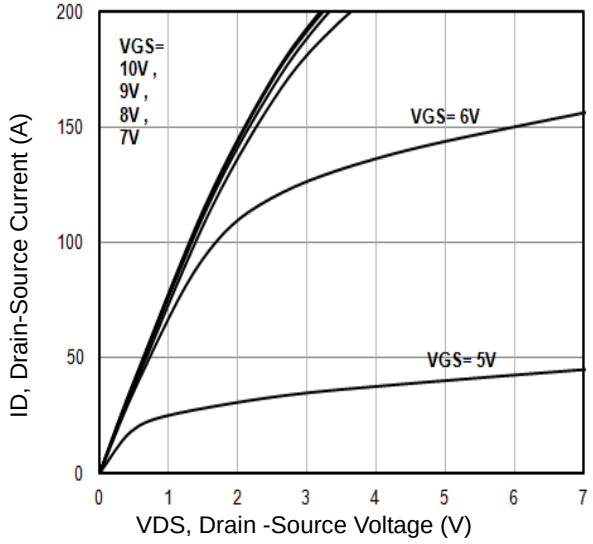


Fig1. Typical Output Characteristics

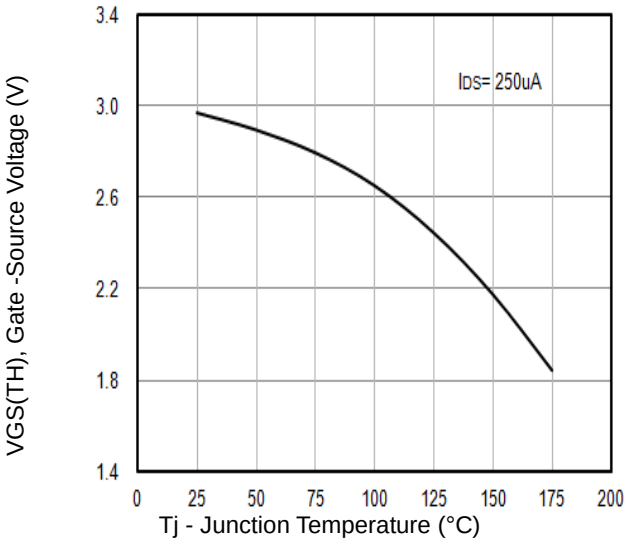


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

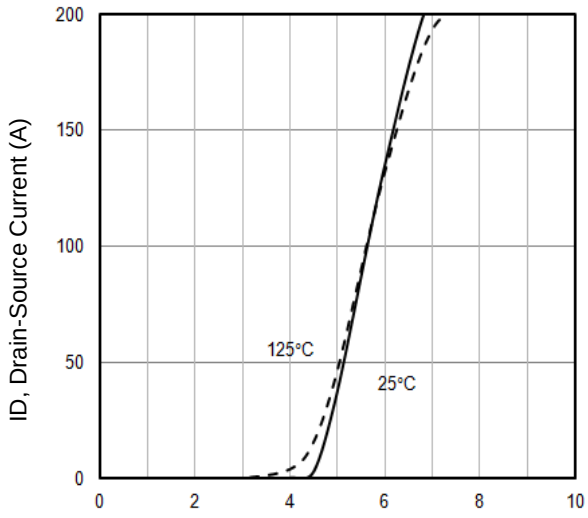


Fig3. Typical Transfer Characteristics

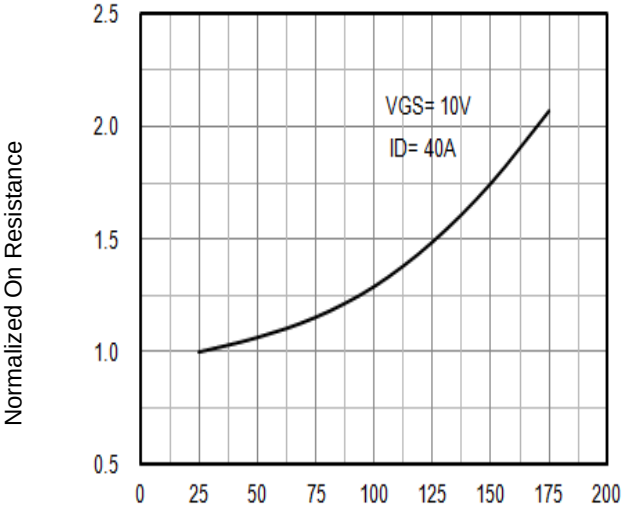


Fig4. Normalized On-Resistance Vs. Tj

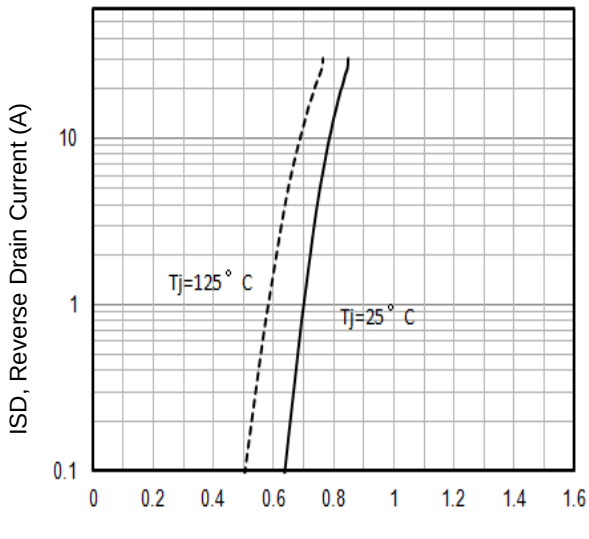


Fig5. Typical Source-Drain Diode Forward Voltage

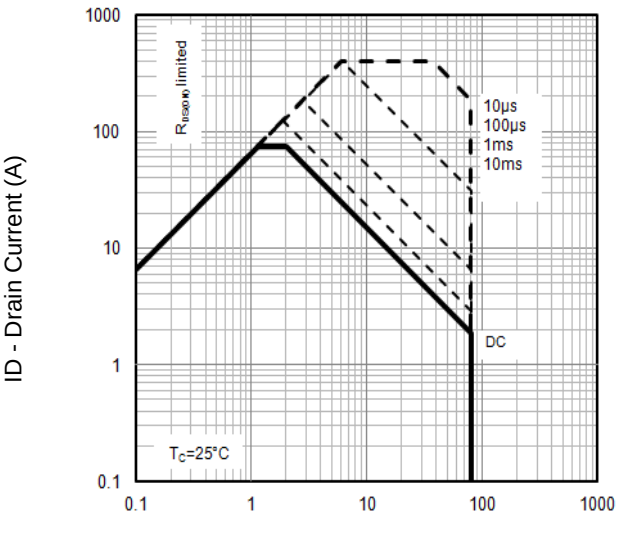


Fig6. Maximum Safe Operating Area

Typical Characteristics

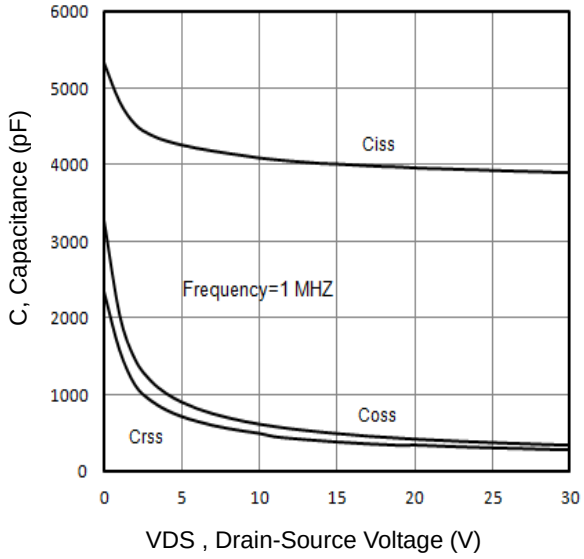


Fig7. Typical Capacitance Vs.Drain-Source Voltage

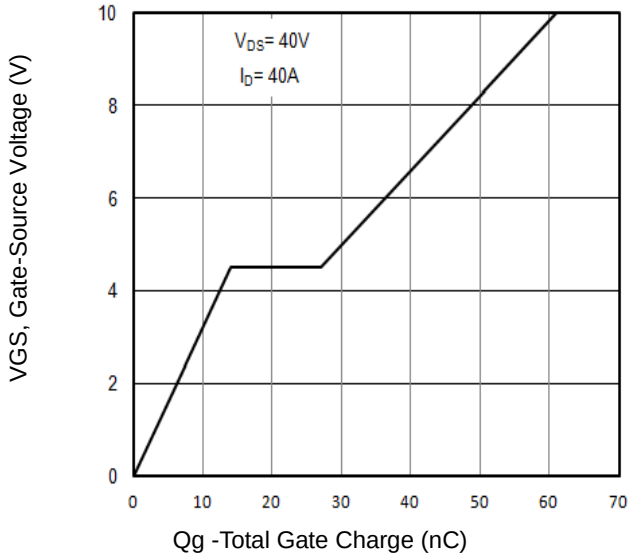


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

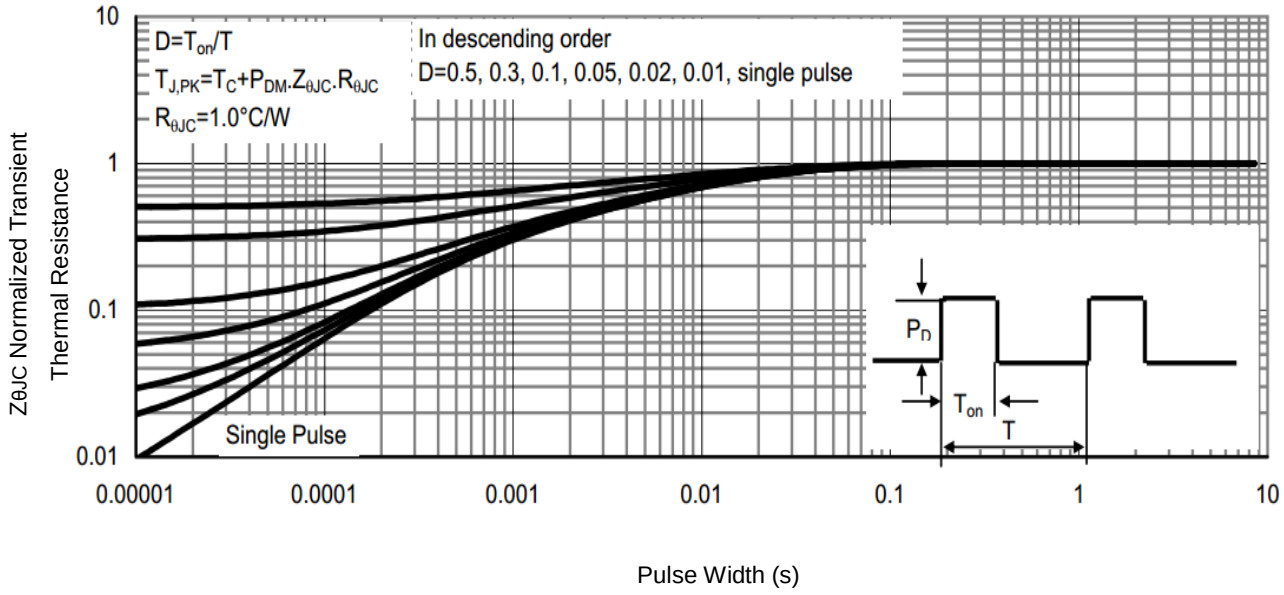


Fig9. Normalized Maximum Transient Thermal Impedance

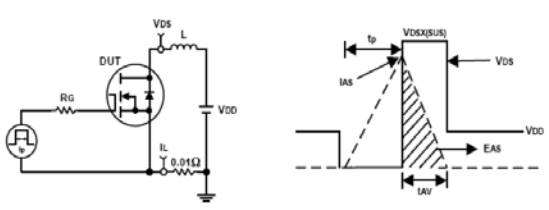


Fig10. Unclamped Inductive Test Circuit and waveforms

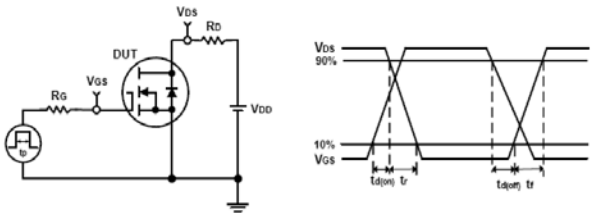
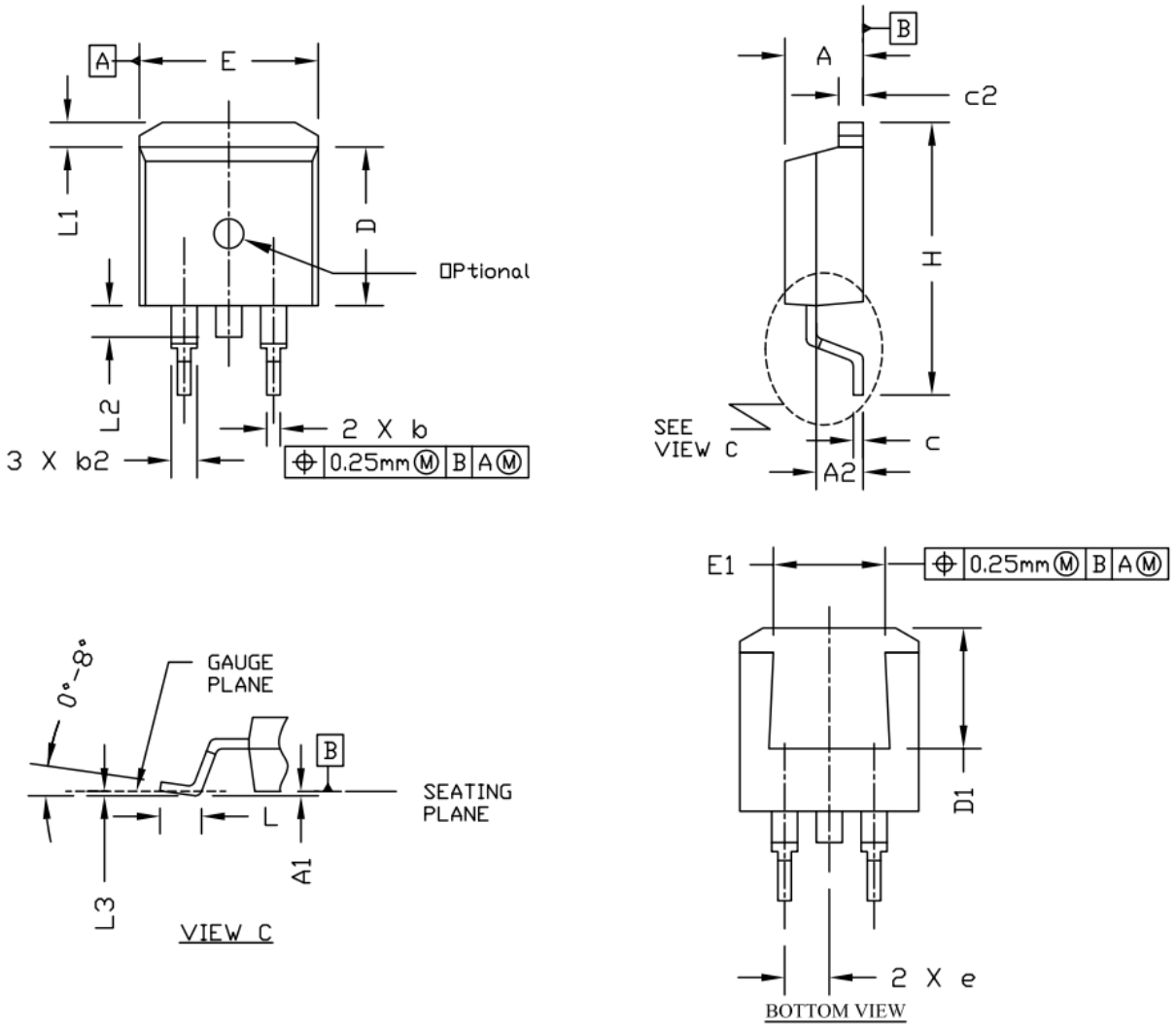


Fig11. Switching Time Test Circuit and waveforms

TO-263 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.400	4.570	4.700
A1	0.000	0.100	0.200
A2	2.300	2.400	2.500
b	0.700	0.800	0.900
b2	1.200	1.270	1.360
c	0.381	0.500	0.737
c2	1.220	1.300	1.350
D	8.600	9.200	9.300
D1	6.860		
e	2.540 BSC		
E	9.780	9.880	10.260
E1	6.225		
H	14.700	15.100	15.500
L	2.000	2.550	2.750
L1	1.000	1.200	1.400
L2	1.300	1.600	1.700
L3	0.255 BSC		

Notes:

1. Refer to JEDEC TO-263 variation AB
2. Dimension "D" & "E" do NOT include mold flash, mold flash shall not exceed 0.127mm per side.

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