VSC4500/VSC2000

T-42-11-90

Low Power, High Speed - LP Series GaAs Gate Arrays

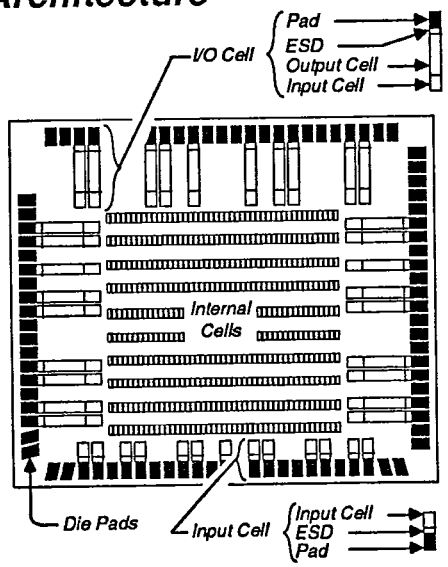
Features

- Superior Performance:
  High Speed, High Density,
  Very Low Power Dissipation
- Proven GaAs E/D MESFET Process
- Array Performance
  - Flip-flop toggle rates:
    943 MHz @ 4.0 mW (typical)
  - Typical gate delay:
    120 ps @ 0.34 mW (2-input NOR)
  - ECL inputs/outputs at 1 GHz
  - TTL inputs/outputs at 100 MHz
  - Typical delay-power product:
    ~0.03 pJ (2-input NOR)
- 100% Utilization Possible
- Programmable Input/Output Interface
  - TTL or ECL (10K, 10KH, or 100K)
  - Mixed ECL and TTL
- Three Temperature Ranges
  - Commercial: 0° to +70° C
  - Industrial: -40° to +85° C
  - Military: -55° to +125° C
- Mil-Std-883C, Level B Screening and Qualification Available
- Fully Supported on MENTOR, DAISY or VALID CAD Platforms

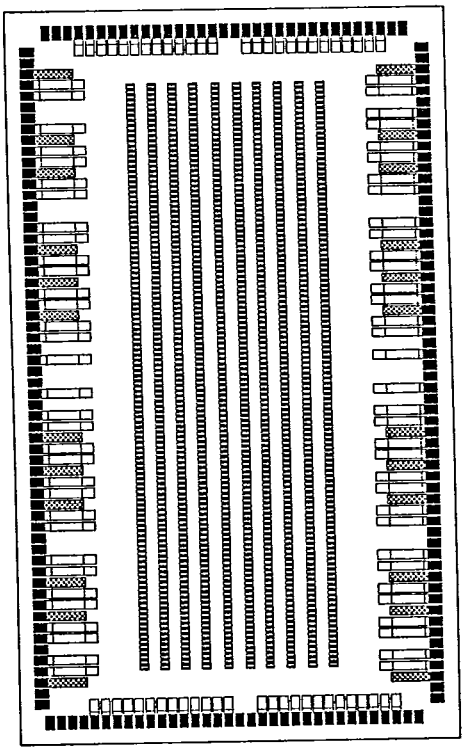
- **VSC2000 Specs**
  - Density: 1800 2-input NOR gates, or 257 D flip-flops in the core array
  - I/O Count: Up to 41 inputs/28 outputs; all can be ECL or TTL
  - Power Disspation: ~1W typical
  - Packages: 52 pin Ceramic LDCC or LCC

- **VSC4500 Specs**
  - Density: 4000 2-input NOR gates, or 570 D flip-flops in the core array
  - Up to 120 input cells; all can be ECL or TTL
  - Up to 68 output or bidirectional cells; all can be ECL, 48 can be TTL
  - Power Dissipation: 2.5W typical
  - Packages: 149 pin Ceramic PGA or 164 pin Ceramic LDCC

Architecture



VSC2000



VSC4500

Introduction

The VSC2000 and VSC4500 are LSI ASICs suited for applications which require high levels of complexity coupled with low power state-of-the-art performance. The VSC2000 and VSC4500 are members of the LP (Low Power) Series Gate Arrays offered by Vitesse Semiconductor Corporation. Vitesse utilizes a proprietary high yielding 0.8µ GaAs enhancement/depletion MESFET process, much like silicon nMOS, to build the LP Series Gate Arrays. These arrays interface with TTL and ECL signal levels and power supplies and can easily be designed into systems utilizing these technologies without any additional system requirements. The LP Series offers the same level of performance of leading-edge ECL arrays with 1/3 to 1/4 of the power dissipation.

Applications

The LP Series can be used in a wide variety of applications including computers, workstations, communications, instrumentation, and military/aerospace systems. These arrays are intended for high performance systems requiring high speed, low power digital logic at medium to high levels of integration.

Computers

Existing mainframe systems using ECL gate arrays can improve system speed and drastically reduce power dissipation with the LP Series. The density and low power dissipation of the VSC2000 make it ideal for the consolidation of multiple PAL designs into a single chip. Systems which use standard microprocessors can bring supercomputing power to workstations by using the VSC4500. Superminicomputers can increase system performance while reducing or eliminating the need for expensive cooling systems.

Communications

Fiber optic communication links for voice or data transmission can be designed with the LP Series. These arrays offer the low power, high performance typically required in these systems while providing the high level of complexity needed to design sophisticated architectures.

Military/Aerospace

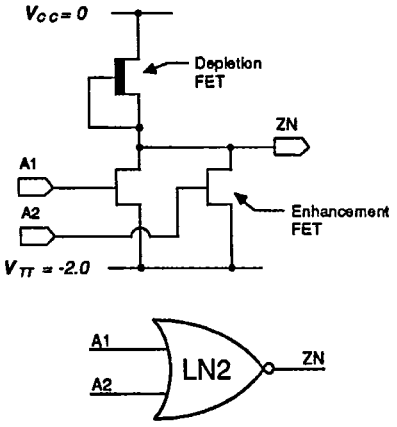
The inherent ability of GaAs devices to withstand extremes in temperature and radiation make the LP Series ideally suited for military/aerospace applications.

Architecture T-42-11-90

These arrays contain three basic cell types: internal logic cells, input only cells, and input/output cells which contain both input and output cells. A simplified layout of each array is shown on page 1-7.

Internal Logic Cells

The internal logic cells comprise the majority of the area of the array. The primitive element or building block is a "cell", which consists of a single depletion transistor and two enhancement transistors optimized to be configured as a 2-input NOR gate shown in the figure below. The internal arrays contain 1800 and 4000 of these cells respectively.



Schematic and Symbol for a 2-Input NOR Gate

Input Cells

The input only cells are located along the bottom in the VSC2000 and along the bottom and top in the VSC4500 (see page 1-7). There is also an input cell in each input/output cell. Input cells can be personalized as ECL or TTL inputs or as differential to single-ended ECL inputs. TTL inputs accept standard TTL signal levels at frequencies up to 150 MHz.

ECL inputs accept standard ECL signals at up to 1 GHz. An internal reference generator is provided to ensure that adequate noise margins will be maintained under worst case conditions. Provisions are made so that the user can provide an external reference, if larger margins are desired. ECL inputs can also be used as differential receivers.

Input/Output Cells

Input/output cells are located on the top, left and right sides of the VSC2000 and on the left and right sides of the VSC4500 (see page 1-7). I/O cells contain both input and output cells and can be configured as inputs, outputs, or bidirectionals. All Input and I/O cells contain circuitry which provides ESD protection.

Output Cells

Output cells are located in input/output cells. These cells can be personalized as ECL or TTL single-ended outputs or as ECL differential outputs.

TTL outputs will provide standard TTL signal levels at frequencies up to 150 MHz. TTL outputs are available in totem pole, tri-state or open collector configurations.

ECL outputs can provide up to 1 GHz single-ended or differential 10K or 100K signal levels which can be driven across external 50Ω loads to V_{TT}. Two output drivers can be connected in parallel to provide 25Ω drive capability.

Power Supplies

The LP Series Gate Arrays can be operated in three different interface modes: a) ECL only, b) TTL only, and c) mixed ECL/TTL. The table below summarizes the power supply requirements in these various interface configurations.

I/O CONFIGURATION	POWER SUPPLIES
ECL Only	-2.0 Volts and Ø Volts
TTL Only	+5.0, -2.0 and Ø Volts
Mixed ECL/TTL	+5.0, -2.0 and Ø Volts

Macrocell Library T-42-11-90

Vitesse provides a Macrocell Library featuring commonly used SSI and MSI logic functions. These macros define the optimized interconnection of transistors in one or more cells in the array. Following is a representative list of the macrocells which are currently available for the LP Series Gate Arrays. Sample performance specifications are listed on the following pages. For complete information, refer to the macrocell library in the LP Series Design Manual.

LP Series Macro Library

Name	Description	# of Cells
Input/Output Macros		
IE	ECL input buffer	1
IEDIFF	Differential to single-ended ECL input buffer	1
OE	ECL output buffer	1
OEDIFF	Differential ECL output buffer	2
IT	TTL input buffer	1
OT	TTL output buffer	1
OTOC	TTL output buffer open drain	1
BIT	Bidirectional TTL I/O buffer	1
BITOC	Bidirectional TTL I/O buffer open drain	1
Buffers		
CDF1	Differential clock buffer, 1x drive	4
CDF2	Differential clock buffer, 2x drive	8
CDF3	Differential clock buffer, 3x drive	12
CLK1	Clock buffer, 1x drive	18
CLK2	Clock buffer, 3x drive	36
CSD1	Single-ended to differential clock buffer	5
LB1	Buffer	4
LB2	Inverter, 3x drive	2
LB3	Inverter, 1x drive	1
LDR1	Line driver/inverting clock buffer, 1x drive	5
LDR2	Line driver/inverting clock buffer, 2x drive	8
LDR3	Line driver/inverting clock buffer, 3x drive	12
Flip-Flops		
LF1	Negative edge triggered D flip-flop	10
LF1L	Negative edge triggered D flip-flop (unbuffered)	7
LF1LX4	Negative edge triggered D flip-flop 4 bit register (unbuffered)	28
LF2	Negative edge triggered D flip-flop w/2-input OR gate data	11
LF3	Negative edge triggered D flip-flop w/asynchronous set & clear	15
LF3R	Negative edge triggered D flip-flop w/asynchronous clear	12
LF4	Negative edge triggered D flip-flop w/3-input OR, synchronous reset	13
LF5	Negative edge triggered D flip-flop w/4-input OR	12
LFC1	Negative edge triggered D flip-flop w/differential clocks	10
LFC2	Negative edge triggered 2-input D flip-flop w/differential clocks	11
LFC3	Negative edge triggered D flip-flop with asynchronous set/reset and differential clocks	16
LFC4	Negative edge triggered D flip-flop w/2-input OR gate data and differential clocks	16
LFC5	D flip-flop w/2-2 OR-AND input and differential clocks	14

Name	Description	# of Cells
Flip-flops (continued)		
LS1	Negative edge triggered flip-flop, w/2:1 multiplexer input	14
LS2	Negative edge triggered flip-flop, w/2:1 multiplexer input and set & reset	18
LS3	Negative edge triggered flip-flop, w/2:1 multiplexer input	18
Logic Gates		
LA1	Half-adder	8
LA2	Full-adder	19
LAND	2-input AND gate	4
LD1	2:4 decoder	10
LD2	3:8 decoder	19
LL1	Low transparent D-latch	6
LL2	Low transparent D-latch w/2-input NOR gate	7
LM1	2:1 Multiplexer	5
LM3	4:1 Multiplexer	14

Name	Description	# of Cells
Logic Gates (continued)		
LM5	8:1 Multiplexer	27
LN2	2-input NOR gate	1
LN2B	Buffered 2-input NOR gate	6
LN3	3-input NOR gate	2
LN4	4-input NOR gate	2
LN5	5-input NOR gate	3
LN6	6-input NOR gate	3
LN8	8-input NOR gate	4
LNA2	2-input NAND gate	2
LR1	2-2 OR-AND gate	4
LR2	2-2-2-2 OR-AND gate	8
LR3	2-2-2 OR-AND gate	5
LX1	2-input exclusive OR gate	6
LX2	2-input exclusive NOR gate	6
Miscellaneous		
PD	Pull-down	1

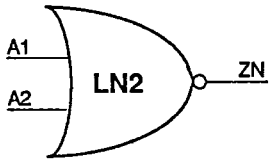
Selected Macrocell AC Performance Characteristics

T-42-11-90

(Over recommended operating conditions, $V_{CC} = V_{CCA} = GND$, Load: F.O. = Ø; Ø mm wire.)

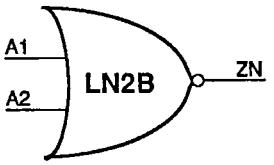
LN2: 2-input NOR - 1 Cell

Parameter		Min	Typ	Max	Units
Propagation Delay A1, A2 to ZN	*Rising Signal*	74	95	121	ps
	Falling Signal	50	60	73	ps
Load Dependent Delay Delay/Fan-out	*Rising Signal*	43	55	71	ps
	Falling Signal	11	13	16	ps
Delay/mm wire	*Rising Signal*	353	450	575	ps
	Falling Signal	36	43	52	ps
Power Dissipation		0.18	0.34	0.53	mW



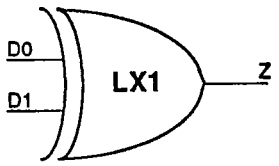
LN2B: Buffered 2-input NOR - 6 Cells

Parameter		Min	Typ	Max	Units
Propagation Delay A1, A2 to ZN	*Rising Signal*	93	120	152	ps
	Falling Signal	79	95	114	ps
Load Dependent Delay Delay/Fan-out	*Rising Signal*	6	8	10	ps
	Falling Signal	7	8	10	ps
Delay/mm wire	*Rising Signal*	49	63	80	ps
	Falling Signal	22	27	32	ps
Power Dissipation		1.14	1.3	2.18	mW



LX1: 2-input XOR - 6 Cells

Parameter		Min	Typ	Max	Units
Propagation Delay D0, D1 to Z	*Rising Signal*	254	325	414	ps
	Falling Signal	338	405	488	ps
Load Dependent Delay Delay/Fan-out	*Rising Signal*	21	26	34	ps
	Falling Signal	8	10	12	ps
Delay/mm wire	*Rising Signal*	168	215	274	ps
	Falling Signal	28	33	40	ps
Power Dissipation		1.38	1.8	3.1	mW



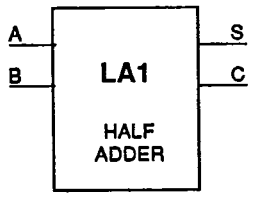
Selected Macrocell AC Performance Characteristics (Cont.)

(Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Load: F.O. = Ø; Ø mm wire.)

T-42-11-90

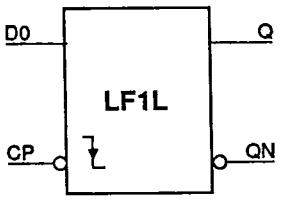
LA1: Half Adder - 19 Cells

Parameter		Min	Typ	Max	Units
Propagation Delay					
A, B to S	*Rising Signal*	384	490	626	ps
	Falling Signal	382	460	551	ps
A, B to C	*Rising Signal*	161	205	263	ps
	Falling Signal	295	355	426	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	21	26	34	ps
	Falling Signal	11	13	16	ps
Delay/mm wire	*Rising Signal*	168	215	274	ps
	Falling Signal	36	43	52	ps
Power Dissipation		1.1	1.4	2.4	mW



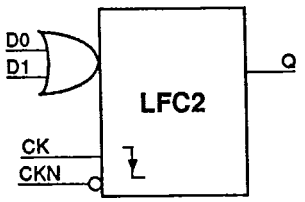
LF1L: Unbuffered Negative Edge Triggered D Flip-flop - 7 Cells

Parameter		Min	Typ	Max	Units
Propagation Delay					
CP to Q	*Rising Signal*	496	635	808	ps
	Falling Signal	374	450	541	ps
CP to QN	*Rising Signal*	477	610	778	ps
	Falling Signal	382	460	551	ps
t_{SET-UP}		317	380	458	ps
t_{HOLD}		93	120	156	ps
Toggle frequency		672	840	1054	MHz
Power Dissipation		1.9	3.2	4.5	mW



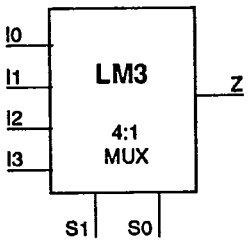
LFC2: Negative Edge Triggered D Flip-flop with 2-input OR & Differential Clocks - 11 Cells

Parameter		Min	Typ	Max	Units
Propagation Delay					
CK, CKN to Q	*Rising Signal*	310	395	505	ps
	Falling Signal	266	320	385	ps
t_{SET-UP}		245	295	354	ps
t_{HOLD}		—	0	—	ps
Toggle frequency		916	1120	1370	MHz
Power Dissipation		2.9	4.0	6.7	mW



LM3: 4:1 Multiplexer - 14 Cells

Parameter		Min	Typ	Max	Units
Propagation Delay					
I0 - I3 to Z	*Rising Signal*	254	325	414	ps
	Falling Signal	346	415	499	ps
S0, S1 to Z	*Rising Signal*	471	600	768	ps
	Falling Signal	439	530	634	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	21	26	34	ps
	Falling Signal	9	11	13	ps
Delay/mm wire	*Rising Signal*	168	215	274	ps
	Falling Signal	30	36	43	ps
Power Dissipation		1.9	2.4	4.0	mW



Notes: *AC Characteristics:*
- *MAX corresponds to worst case delay over temperature, process and power supply variations.*
- *TYP corresponds to the delay at T_C = 25° C, typical process and power supply variations.*
- *MIN corresponds to the delay at T_C = 0° C, worst case process and power supply variations.*

Toggle Frequency:
- *MAX corresponds to MIN delays with FO = 1, wire = 0.25mm.*
- *MIN corresponds to MAX delays with FO = 1, wire = 0.25mm.*

DC Characteristics

ECL Inputs/Outputs: *(Over recommended operating conditions with internal V_{REF}. V_{CC} = GND, Output load 50Ω to V_{TT})*

T-42-11-90

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	—	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1040	—	-650	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1600	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	10	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential ECL output pins must be terminated identically.

TTL Inputs/Outputs: *(Over recommended operating conditions, TTLGND = GND)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—		V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage		—	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	—		V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage		—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OCZ}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

Absolute Maximum Ratings (1)

Power Supply Voltage (ECL), (V_{TT}) ..... -2.5V to +0.5V
Power Supply Voltage (TTL) (V_{TTL}) ..... +6.0V to -0.5V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... +0.5V to V_{TT}
TTL Input Voltage Applied (2), (V_{TTLIN}) ..... -0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HIGH) ..... 50 mA
Maximum Junction Temperature, (T_J) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature(3), (T_{STG}) ..... -65° to +150°C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

2) V_{TT} (V_{TTL}) must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.

3) Lower limit of specification is ambient temperature and upper limit is case temperature.

Recommended Operating Conditions

T-42-11-90

ECL Power Supply Voltage (1), (V_{TT}) ..... -2.1V to -1.9V

TTL Power Supply Voltage, (V_{TTL}) ..... +4.75V to +5.25V

Operating Temperature (2), (T)...(Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTE: 1) When using Internal ECL 100K reference level.

2) Lower limit of specification is ambient temperature and upper limit is case temperature.

Packaging

The VSC2000's standard package is a 52-pin ceramic leaded (LDCC) or leadless (LCC) chip carrier. The VSC4500 may be packaged in a 149 pin ceramic pin grid array (PGA) or a 164 pin ceramic leaded chip carrier (LDCC). All three packages are multilayer ceramic packages with the cavity down and a Cu-W heat spreader on top. Particular attention has been paid to reduce crosstalk of high speed signals and to keep the trace impedance at 50Ω.

Option Development Procedure

Vitesse Semiconductor offers its customers the option of fully designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse application engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are performed by a Vitesse application engineer.

- Final placement and routing of the design
- Net-length extraction
- Fan-out and metal delay calculation
- Design rule check and layout vs. schematic

Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The figure at right summarizes the typical gate array project flow and specifies the various task responsibilities which are delegated to the customer or to Vitesse.

CAD Tools/Support

LP Series designs are supported on MENTOR, DAISY, and VALID workstations. The Vitesse support package includes documentation and software which allows the customer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back annotated simulation upon completion of place and route. Also, Vitesse has an interactive pre-placement program that the customer may use.

Training

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process, and are recommended to customers planning to implement a design in a Vitesse gate array. Classes last two days in length and are provided at Vitesse's facility or at the customer's site.