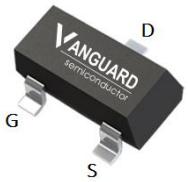
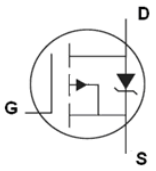
Features

- P-Channel
- Enhancement mode
- Fast Switching
- Pb-free lead plating; RoHS compliant

V_{DS}	-100	V
$R_{DS(on),max}$ @V_{GS}=-10V	480	mΩ
$R_{DS(on),max}$ @V_{GS}=-4.5V	510	mΩ
I_D	-1.3	A

SOT23





Pb-Free RoHS Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VSC600P10MS	SOT23	1P2	3000pcs/reel

Maximum ratings, at T_A =25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		-100	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_A =25°C	-0.8	A
I_D	Continuous drain current @V_{GS}=-10V	T_A =25°C	-1.3	A
		T_A =70°C	-1	A
I_{DM}	Pulse drain current tested ①	T_A =25°C	-5.2	A
PD	Maximum power dissipation	T_A =25°C	1	W
T_{STG},T_J	Storage and operating temperature range		-55 to 150	°C
Thermal Characteristics				
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead		80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		125	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_j=25℃)	V_{DS}=-100V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=-100V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.0	-2.0	-3.0	V
$R_{DS(on)}$	Drain-Source On-State Resistance②	V_{GS}=-10V, I_D=-1.3A	--	480	600	mΩ
		V_{GS}=-4.5V, I_D=-1A	--	510	650	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=-30V,V_{GS}=0V, f=1MHz	440	515	590	pF
Coss	Output Capacitance		20	25	30	pF
Crss	Reverse Transfer Capacitance		10	15	20	pF
$Q_{g(-10V)}$	Total Gate Charge	V_{DS}=-50V,I_D=-1A, V_{GS}=-10V	--	11	--	nC
$Q_{g(-4.5V)}$	Total Gate Charge		--	5.3	--	nC
Qgs	Gate-Source Charge		--	1.7	--	nC
Qgd	Gate-Drain Charge		--	2	--	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=-50 V, I_D=-1A, R_G=2.7Ω, V_{GS}=-10V	--	6.4	--	ns
Tr	Turn-on Rise Time		--	3.4	--	ns
Td(off)	Turn-Off Delay Time		--	40	--	ns
Tf	Turn-Off Fall Time		--	31	--	ns
Source- Drain Diode Characteristics@ T_j= 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=-1A,V_{GS}=0V	--	-0.8	-1.2	V
Trr	Reverse Recovery Time	T_j=25℃,I_{sd}=-1A, V_{GS}=0V di/dt=-100A/μs	--	22	--	ns
Qrr	Reverse Recovery Charge		--	20	--	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

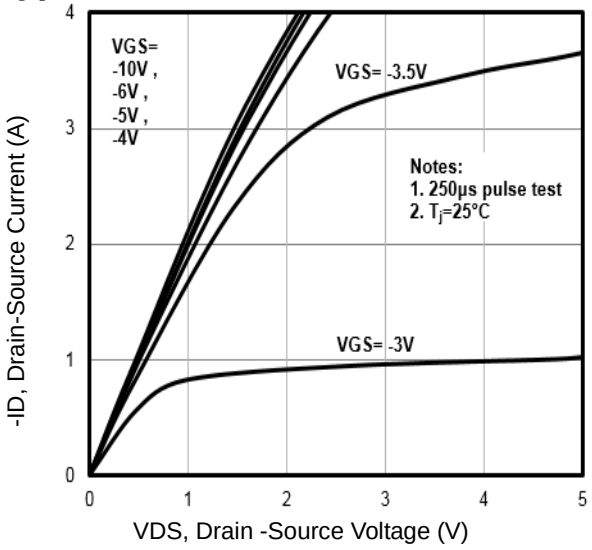


Fig1. Typical Output Characteristics

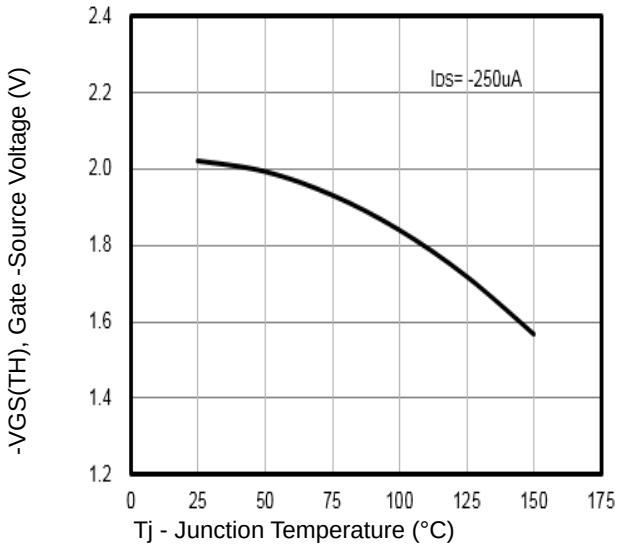


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

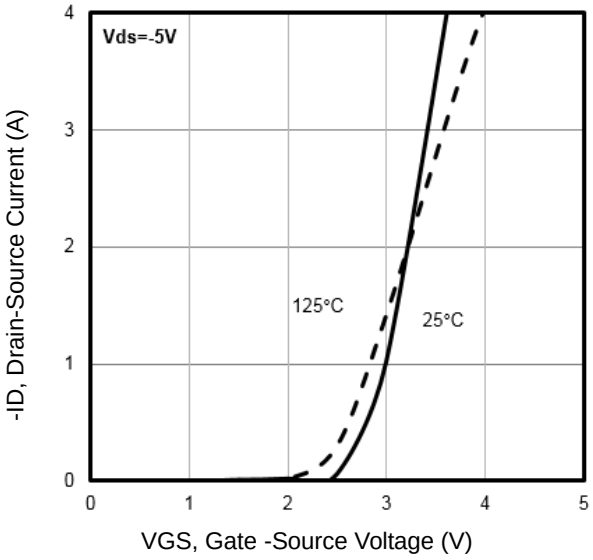


Fig3. Typical Transfer Characteristics

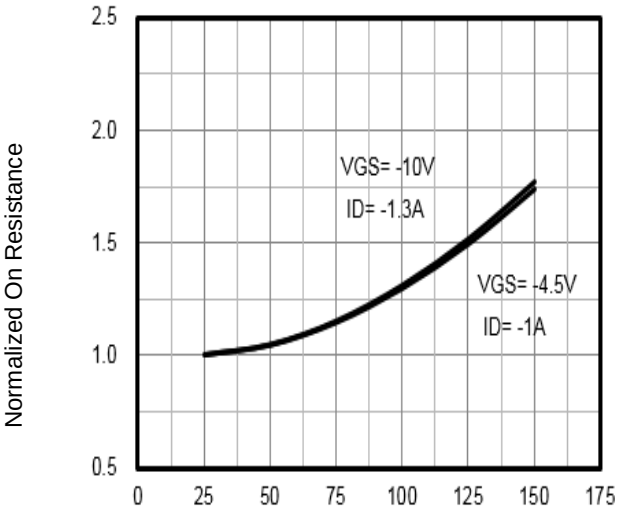


Fig4. Normalized On-Resistance Vs. Tj

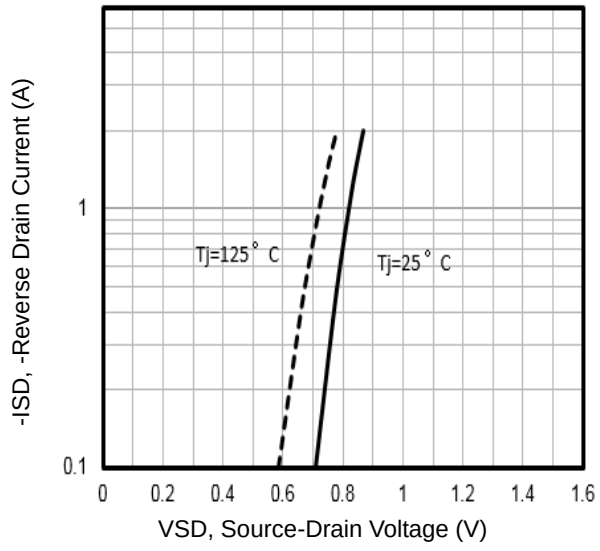


Fig5. Typical Source-Drain Diode Forward Voltage

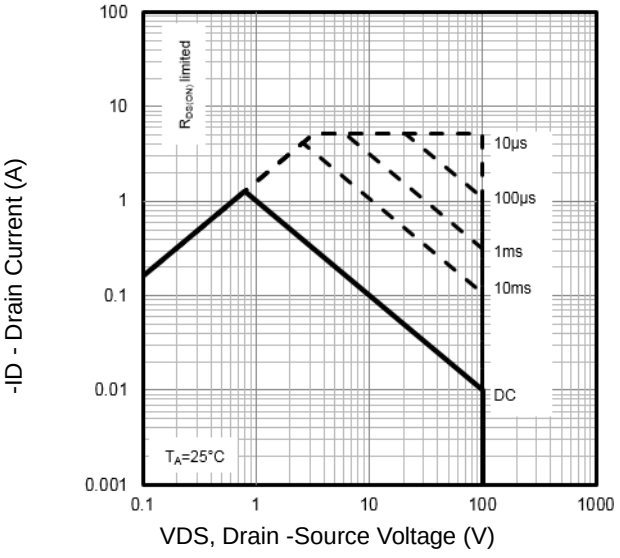


Fig6. Maximum Safe Operating Area

Typical Characteristics

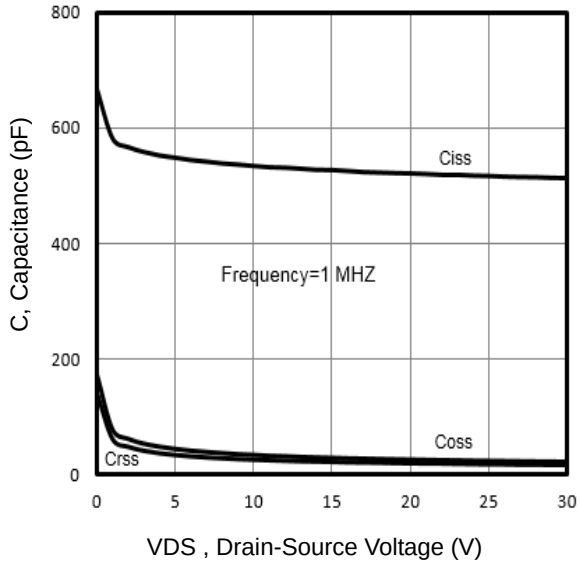


Fig7. Typical Capacitance Vs.Drain-Source Voltage

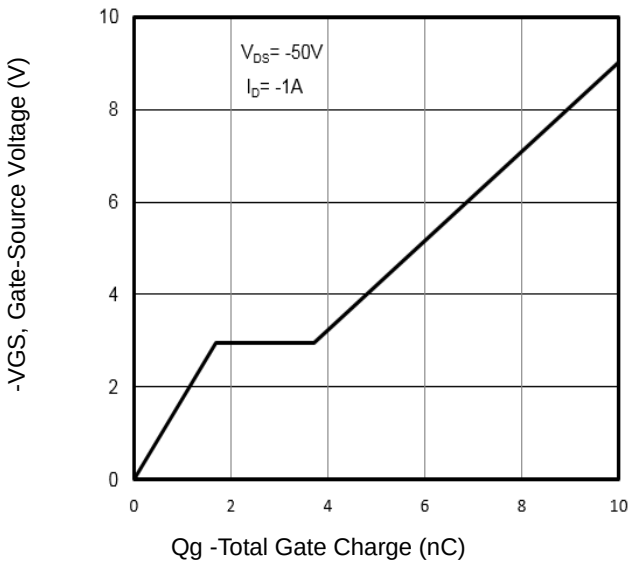


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

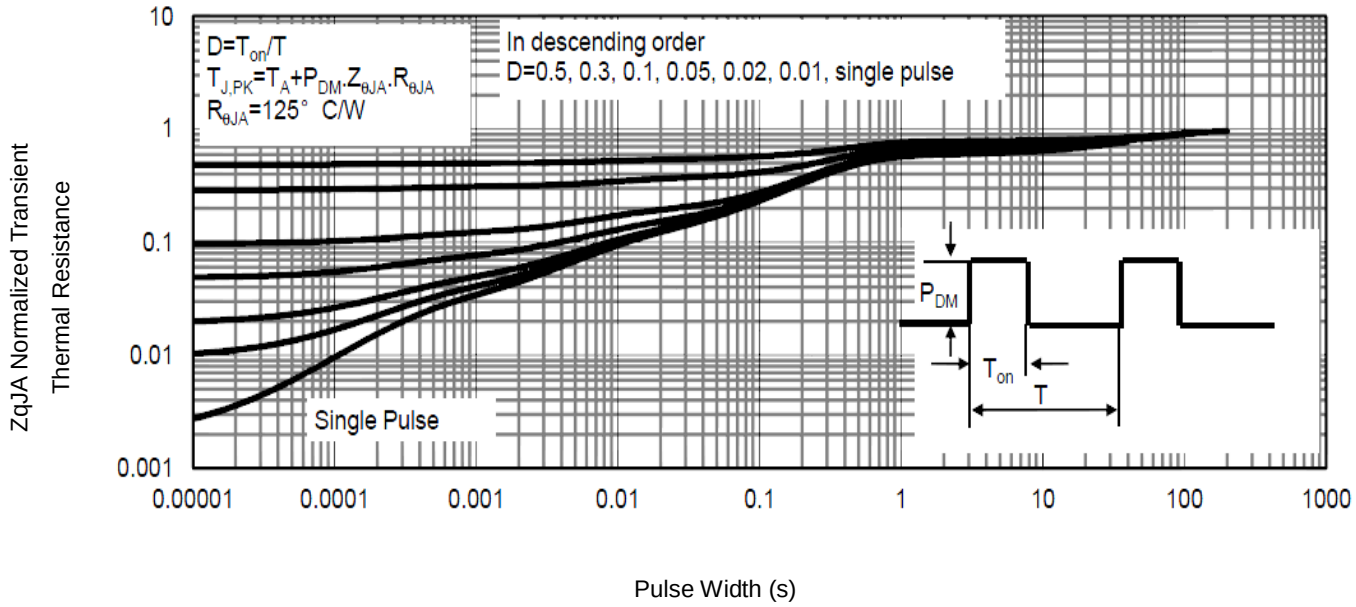


Fig9. Normalized Maximum Transient Thermal Impedance

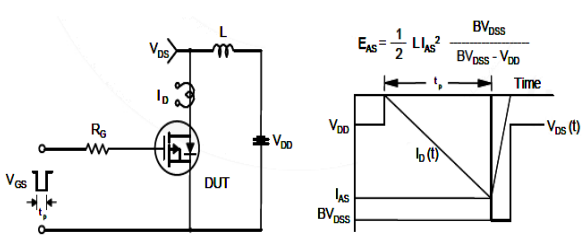


Fig10. Unclamped Inductive Test Circuit and waveforms

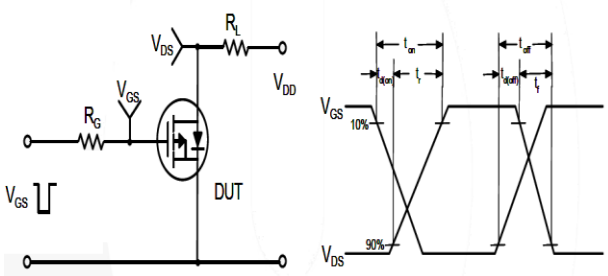
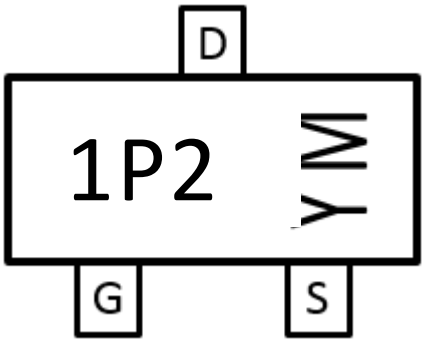


Fig11. Switching Time Test Circuit and waveforms

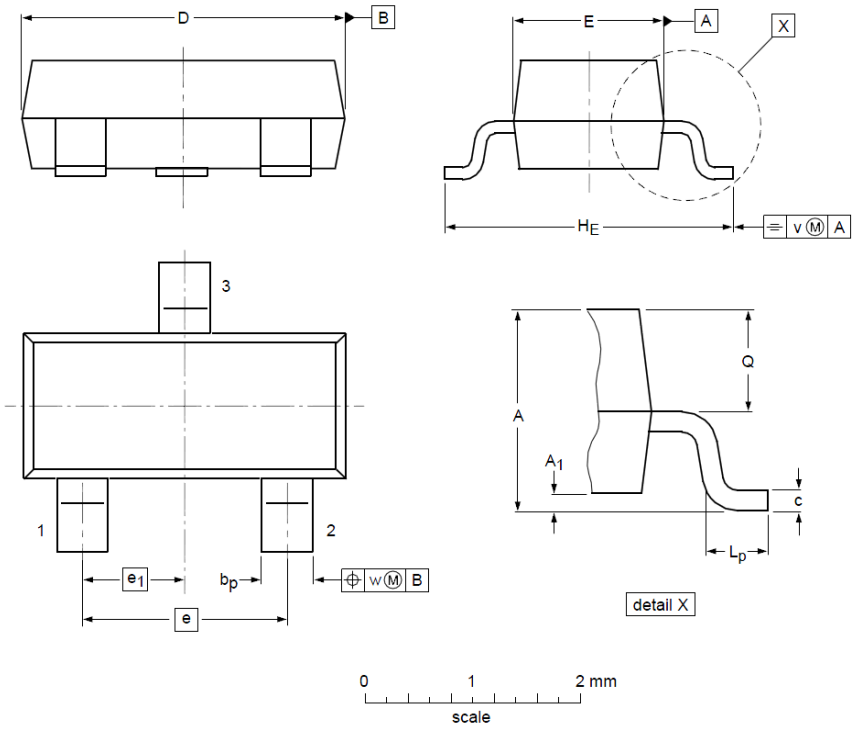
Marking Information



1P2： Part Number

YM： Date Code，Y means assembly year (e.g. E=2017, F=2018, G=2019, H=2020, etc)，
M means assembly month (e.g. 9=September, O=October, N=November, D=December, etc)

SOT23 Package Outline Data



Label	DIMENSIONS (unit: mm)		
	Min	Typ	Max
A	0.90	1.03	1.10
A_1	0.01	0.05	0.10
b_p	0.38	0.42	0.48
c	0.09	0.13	0.15
D	2.80	2.92	3.00
E	1.20	1.33	1.40
e	--	1.90	--
e_1	--	0.95	--
H_E	2.10	2.40	2.50
L_p	0.40	0.50	0.60
Q	0.45	0.49	0.55
v	--	0.20	--
w	--	0.10	--

Notes:

1. Follow JEDEC TO-236, variation AB.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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