Preliminary Datasheet

VSC7139

Quad Transceiver for Gigabit Ethernet and Fibre Channel

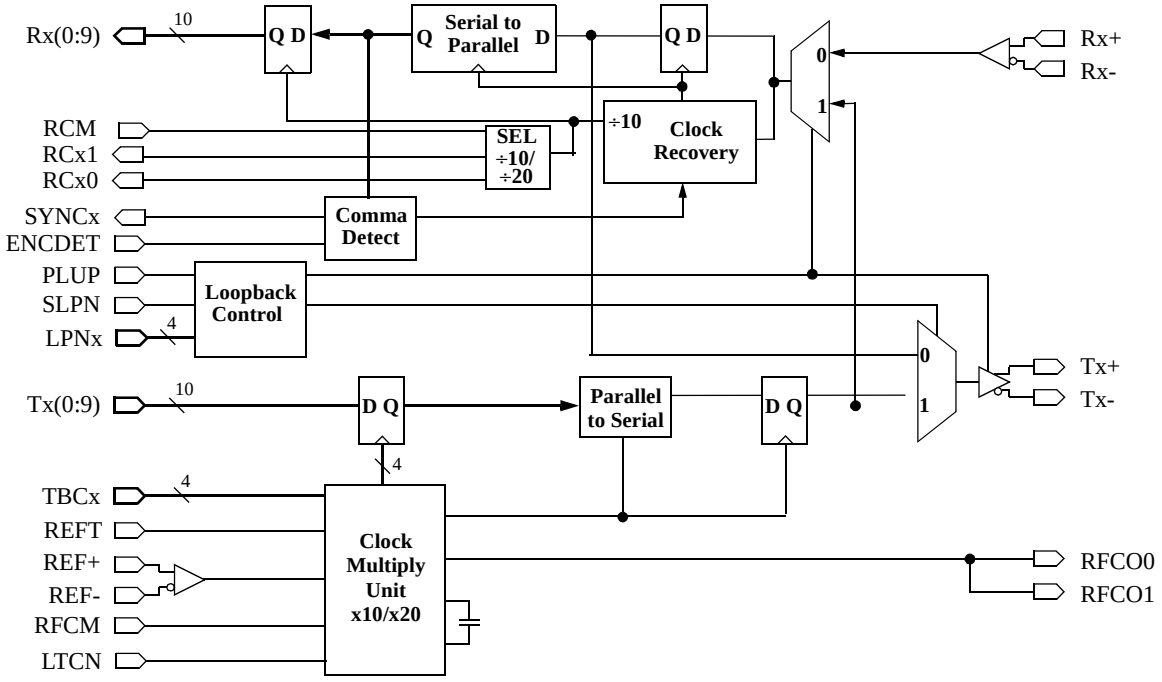
Features

- Four Complete Transmitter/ Receiver Functions in a Single Integrated Circuit
- Full Fibre Channel (T11) and Gigabit Ethernet (IEEE 802.3z) Compliance
- 1.05Gb/s to 1.36Gb/s Operation per Channel
- Common or Per-Channel Transmit Byte Clocks
- TTL or PECL Reference Clock Input
- 1/10th or 1/20th Baud Rate Recovered Clocks
- Common and Per-Channel, Serial and Parallel Loopback Controls
- Common Comma Detect Enable Inputs
- Per-Channel Comma Detect Outputs
- Cable Equalization in Receivers
- Automatic Lock-to-Reference
- 3.3V Power Supply, 2.67 W Max Power Dissipation
- 208-Pin, 23mm BGA Packaging

General Description

The VSC7139 is a full-speed Quad Fibre Channel and Gigabit Ethernet Transceiver IC. Each of the four transmitters has a 10-bit wide bus, running up to 136MHz, which accepts 8B/10B encoded transmit characters and serializes the data onto high speed differential outputs at speeds up to 1.36Gb/s. The transmit data can be synchronous to the reference clock, a common transmit byte clock or a per-channel transmit byte clock. Each receiver samples serial receive data, recovers the clock and data, deserializes it into 10-bit receive characters, outputs a recovered clock and detects “Comma” characters. The VSC7139 contains on-chip (PLL) circuitry for synthesis of the baud-rate transmit clock and extraction of the clocks from the received serial streams.

VSC7139 Block Diagram (1 of 4 Channels)



Functional Description

Notation

In this document, each of the four channels are identified as Channel A, B, C or D. When discussing a signal on any specific channel, the signal will have the Channel letter embedded in the name, i.e., "T**A**(0:9)." When referring to the common behavior of a signal which is used on each of the four channels, a lower case "x" is used in the signal name, i.e. T**x**(0:9). Differential signals, i.e. RA+ and RA-, may be referred to as a single signal, i.e. RA, by dropping reference to the "+" and "-". "REF" refers to either the TTL input REFT, or the PECL differential inputs REF+/REF-, whichever is used.

Clock Synthesizer

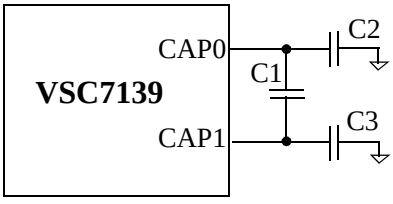
The VSC7139 clock synthesizer multiplies the reference frequency provided on the REF input by 10 or 20 to achieve a baud rate clock between 1.05GHz and 1.36GHz. The REF input can be either TTL or PECL. If TTL, connect the TTL input clock to REFT. If PECL, connect the PECL inputs to REF+ and REF-. The internal clock presented to the Clock Synthesizer is a logical XNOR of REFT and REF+/-. The reference clock will be active HIGH if the unused input is HIGH. The reference clock is active LOW if the unused input is LOW. REFT has an internal pull-up resistor. Internal biasing resistors set the proper DC level on REF+/- so AC-coupling may be used.

The TTL outputs, RFCO0 and RFCO1, provide a clock that is frequency locked to the REF input. This clock is derived from the clock synthesizer and is always 1/10 the baud rate, regardless of the state of the RFCM input.

The on-chip PLL uses a single external 0.1µF capacitor, connected between CAP0 and CAP1, to control the Loop Filter. This capacitor should be a multilayer ceramic dielectric, or better, with at least a 5V working voltage rating and a good temperature coefficient, i.e., NPO is preferred but X7R may be acceptable. These capacitors are used to minimize the impact of common mode noise on the Clock Multiplier Unit (CMU), especially power supply noise. Higher value capacitors provide better robustness in systems. NPO is preferred because if an X7R capacitor is used, the power supply noise sensitivity will vary with temperature.

For best noise immunity, the designer may use a three capacitor circuit with one differential capacitor between CAP0 and CAP1, C1, a capacitor from CAP0 to ground, C2, and a capacitor from CAP1 to ground, C3. Larger values are better but 0.1µF is adequate. However, if the designer cannot use a three capacitor circuit, a single differential capacitor, C1, is adequate. These components should be isolated from noisy traces.

Figure 1: Loop Filter Capacitors (Best Circuit)



C1=C2=C3= >0.1µF
MultiLayer Ceramic
Surface Mount
NPO (Preferred) or X7R
5V Working Voltage Rating

Serializer

The VSC7139 accepts TTL input data as a parallel 10 bit character on the Tx(0:9) bus which is latched into the input register on the rising edge of either REF or TBCx. Three clocking modes are available and automatically detected by the VSC7139. If TBCC is static and RFCM is HIGH, then all four Tx(0:9) busses are latched on the rising edges of REF. If TBCC is static and RFCM is LOW, then REF is multiplied by 20 and the input busses are latched on the rising edges of REF and at the midpoint between rising edges. If TBCC is toggling but TBCB is static, then all four Tx(0:9) busses are latched on the rising edges of TBCC. If TBCB and TBCC are both toggling then the rising edge of each TBCx latches the corresponding Tx(0:9) bus.

The active TBCC or TBCx inputs must be frequency-locked to REF. There is no specified phase relationship. Prior to normal data transmission, LTCN must be asserted LOW so that the VSC7139 can lock to TBCx which may result in corrupted data being transmitted. Once LTCN has been raised HIGH, the transmitters remain locked to REF and can tolerate $\pm$2 bit times of drift in TBCx relative to REF.

The 10-bit parallel transmission character will be serialized and transmitted on the Tx PECL differential outputs at the baud rate with bit Tx0 (bit a) transmitted first. User data should be encoded using 8B/10B or an equivalent code. The mapping to 10B encoded bit nomenclature and transmission order is shown in Table 1, along with the recognized comma pattern.

Table 1: Transmission Order and Mapping of a 10B Character

Data Bit	*Tx9*	*Tx8*	*Tx7*	*Tx6*	*Tx5*	*Tx4*	*Tx3*	*Tx2*	*Tx1*	*Tx0*
10B Bit Position	j	h	g	f	i	e	d	c	b	a
Comma Character	x	x	x	1	1	1	1	1	0	0

Clock Recovery

The VSC7139 accepts differential high speed serial input from the selected source (either the PECL Rx+/Rx- pins or the internal Tx+/- data), extracts the clock and retimes the data. Equalizers are included in the receiver to open the data eye and compensate for InterSymbol Interference (ISI) which may be present in the incoming data. The serial bit stream should be encoded so as to provide DC balance and limited run length by an 8B/10B encoding scheme. The digital Clock Recovery Unit (CRU) is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within $\pm$200 ppm of ten times the REF frequency. For example, Gigabit Ethernet systems would use 125MHz oscillators with a $\pm$100ppm accuracy resulting in $\pm$200 ppm between VSC7139 pairs.

Deserializer

The recovered serial bit stream is converted into a 10-bit parallel output character. The VSC7139 provides complementary TTL recovered clocks, RCx0 and RCx1, which are at one-twentieth of the serial baud rate (if RCM=LOW) or one-tenth (if RCM=HIGH). The clocks are generated by dividing down the high-speed recovered clock which is phase locked to the serial data. The serial data is retimed, deserialized and output on Rx(0:9).

If serial input data is not present, or does not meet the required baud rate, the VSC7139 will continue to produce a recovered clock so that downstream logic may continue to function. The RCx0/RCx1 output frequency under these circumstances will differ from its expected frequency by no more than $\pm$1%.

Word Alignment

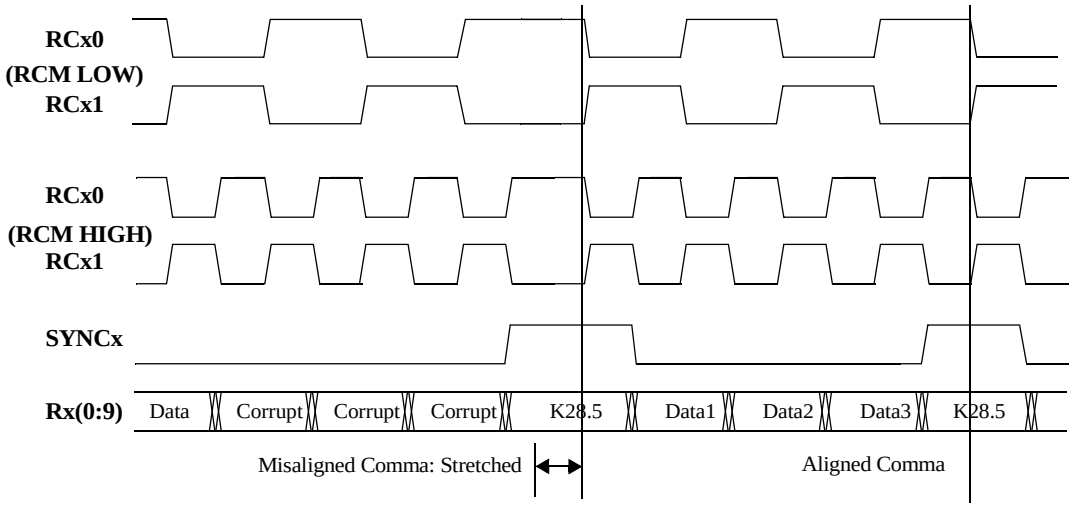
The VSC7139 provides 7-bit comma character recognition and data word alignment. Word synchronization is enabled on all channels by asserting ENCDET HIGH. When synchronization is enabled, the receiver examines the recovered serial data for the presence of the "Comma" pattern. This pattern is "0011111XXX", where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which are defined for synchronization purposes. Improper comma alignment is defined as any of the following conditions:

1. The comma is not aligned within the 10-bit transmission character such that Rx(0...6) = "0011111".
2. The comma straddles the boundary between two 10-bit transmission characters.
3. The comma is properly aligned but occurs in the received character presented during the rising edge of RCx0 rather than RCx1.

When ENCDET is HIGH and an improperly-aligned comma is encountered, the recovered clock is stretched, never slivered, so that the comma character and recovered clocks are aligned properly to Rx(0:9). This results in proper character and word alignment. When the parallel data alignment changes in response to a improperly-aligned comma pattern, data which would have been presented on the parallel output port prior to the comma character, and possibly the comma character itself, may be lost. Possible loss of the comma character is data dependent, according to the relative change in alignment. Data subsequent to the comma character will always be output correctly and properly aligned. When ENCDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

On encountering a comma character, SYNCx is driven HIGH. The SYNCx pulse is presented simultaneously with the comma character and has a duration equal to the data. The SYNCx signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RCx1. Functional waveforms for synchronization are given in Figure 2. The first K28.5 shows the case where the comma is detected, but it is misaligned so a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process. The second K28.5 shows the case when a comma is detected and no phase adjustment is necessary. Figure 2 illustrates the position of the SYNCx pulse in relation to the comma character on Rx(0:9).

Figure 2: Misaligned and Aligned K28.5 Characters



Loopback Operation

Loopback operation is controlled by the PLUP (Parallel Loopback), SLPN (Serial Loopback) and LPNx inputs as shown in Table 2. LPNx enables PLUP/SLPN on a per-channel basis when LOW. If LPNx is HIGH, PLUP/SLPN have no impact on Channel x. When SLPN and PLUP are both HIGH the transmitter output is held HIGH. When RXx is looped back to TXx, the data goes through a clock recovery unit so much of the input jitter is removed. However, the TXx outputs may not meet jitter specifications listed in the "Transmitter AC Specifications" due to low frequency jitter transfer from RXx to TXx.

Table 2: Loopback Selection

LPNx	*PLUP*	*SLPN*	*Tranmitter Source*	*Receiver Source*
LOW	LOW	LOW	Receiver	Receiver
LOW	LOW	HIGH	Transmitter	Receiver
LOW	HIGH	LOW	Transmitter	Transmitter
LOW	HIGH	HIGH	HIGH	Transmitter
HIGH	X	X	Transmitter	Receiver

JTAG Access Port

A JTAG Access Port is provided to assist in board-level testing. Through this port most pins can be accessed or controlled and all TTL outputs can be tri-stated. A full description of the JTAG functions on this device is available in "VSC7139 JTAG Access Port Functionality."

AC Characteristics

Figure 3: Transmit Timing Waveforms

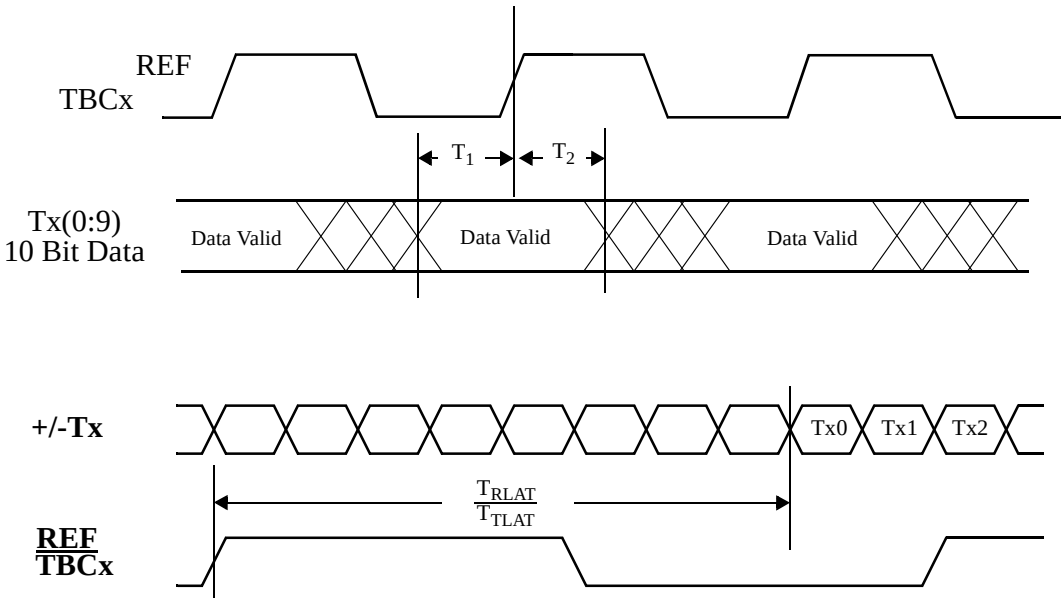


Table 3: Transmitter AC Characteristics

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_1	Tx(0:9) Setup time to the rising edge of TBCx or REF	1.5	—	—	ns	Measured between the valid data level of Tx(0:9) to the 1.4V point of TBCx or REF
T_2	Tx(0:9) hold time after the rising edge of TBCx or REF	1.0	—	—	ns	
T_{SDR},T_{SDF}	Tx+/Tx- rise and fall time	—	—	300	ps	20% to 80%, 75Ω load to $V_{DD}/2$, tested on a sample basis
T_{RLAT}	Latency from rising edge of REF to Tx0 appearing on TX+/TX-	7bc + 0.66ns	—	7bc + 1.46ns		bc = Bit clocks ns = nanoseconds
T_{TLAT}	Latency from rising edge of TBCx to Tx0 appearing on TX+/TX-	5bc + 0.66ns	—	11bc + 1.46ns	ns	bc = Bit clocks ns = nanoseconds
Transmitter Output Jitter						
RJ	Random jitter (RMS)	—	5	8	ps	Measured at SO+/-, 1 sigma deviation of 50% crossing pointt
DJ	Serial data output deterministic jitter (pk-pk)	—	35	80	ps	IEEE 802.3Z Clause 38.68, tested on a sample basis

Figure 4: Receive Timing Waveforms

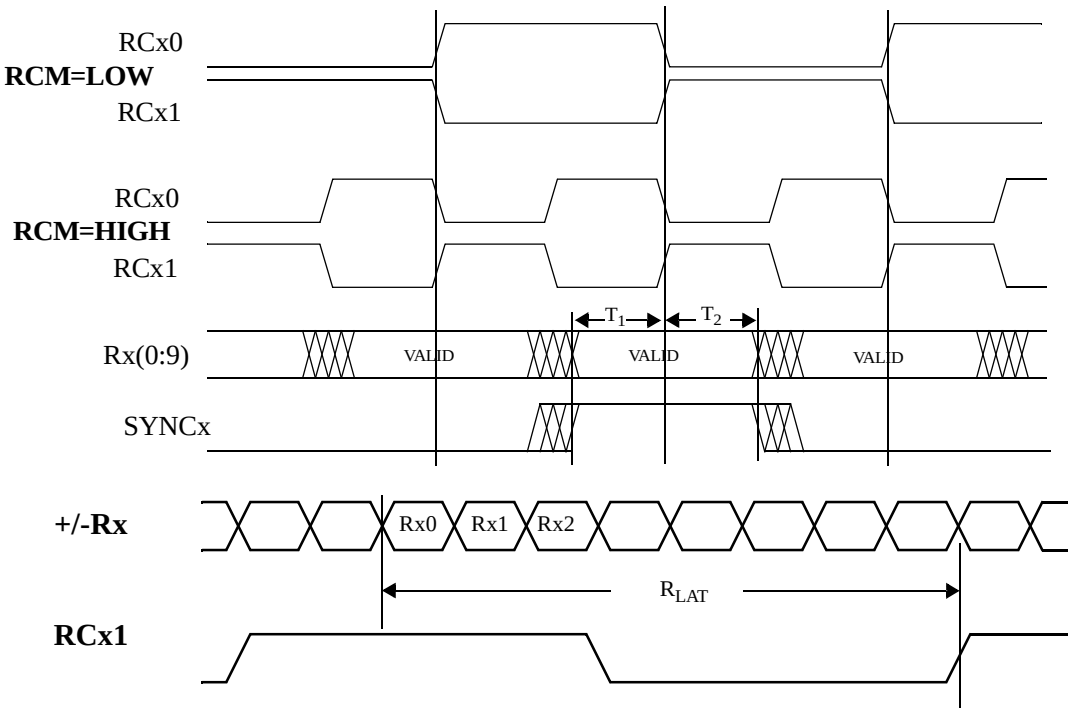


Table 4: Receive AC Characteristics

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_1	TTL Outputs Valid prior to RCx1/ RCx0 rise	4.0 3.0 TBD	— — —	— — —	ns	@ 1.0625Gb/s @ 1.25Gb/s @ 1.36Gb/s
T_2	TTL Outputs Valid after RCx1 or RCx0 rise	3.0 2.0 TBD	— — —	— — —	ns	@ 1.0625Gb/s @ 1.25Gb/s @ 1.36Gb/s
T_3	Delay between rising edge of RCx1 to rising edge of RCx0	10 x T_{RX} -500	—	10 x T_{RX} +500	ps	T_{RX} is the bit period of the incoming data on Rx.
T_4	Period of RCx1 and RCx0	1.98 x T_{REF}	—	2.02 x T_{REF}	ps	Whether or not locked to serial data.
T_R, T_F	TTL Output rise and fall time	—	—	2.4	ns	Between $V_{IL(max)}$ and $V_{IH(min)}$, into 10 pf. load.
R_{LAT}	Latency from serial bit Rx0 to rising edge RCx1	12bc + 2.77ns	—	13bc + 7.28ns		bc = Bit clock ns = Nano second
T_{LOCK}	Data acquisition lock time(1)	—	—	1400	bit times	8B/10B IDLE pattern. Tested on a sample basis

NOTE: (1) Probability of recovery for data acquisition is 95% per Section 5.3 of FC-PH, rev. 4.3.

Figure 5: REF and TBCx Waveforms

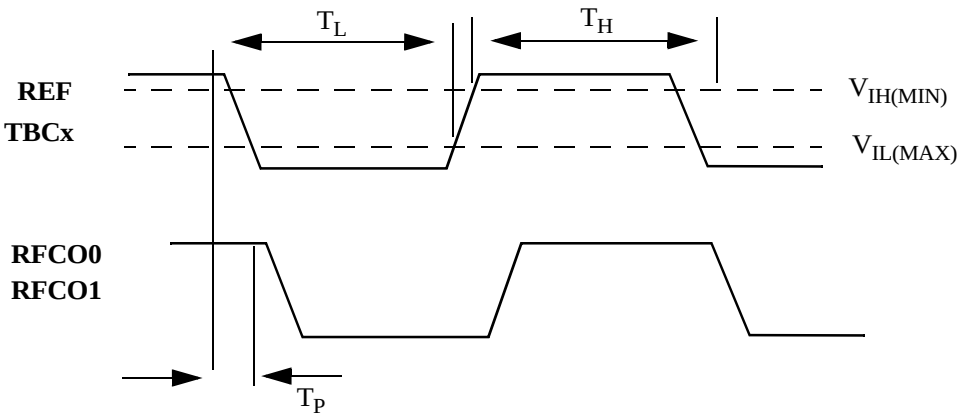


Table 5: Reference Clock Requirements

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
FR	Frequency Range	105	—	136	MHz	Range over which both transmit and receive reference clocks on any link may be centered
FO	Frequency Offset	-200	—	200	ppm	Maximum frequency offset between transmit and receive reference clocks on one link
T_P	Delay from REF to RFCO0/1	1.97	—	3.58	ns	
DC	RFC0/1 Duty Cycle	40	—	60	%	
T_R/T_F	RFC0/1 rise and fall time	0.25	—	1.5	ns	Between $V_{IL(max)}$ and $V_{IH(min)}$
DC	REF/TBCx duty cycle	35	—	65	%	Measured at 1.4V
T_{RCR},T_{RCF}	REF/TBCx rise and fall time	—	—	1.5	ns	Between $V_{IL(max)}$ and $V_{IH(min)}$

DC Characteristics

Parameters	*Description*	*Mi.*	*Typ*	*Max*	*Units*	*Conditions*
TTL Outputs						
V_{OH}	TTL output HIGH voltage	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	TTL output LOW voltage	—	—	0.5	V	I_{OL} = +1.0mA
I_{OZ}	TTL output Leakage current	—	—	50	µA	When set to high-impedance state through JTAG.
TTL Inputs						
V_{IH}	TTL input HIGH voltage	2.0	—	5.5	V	5V Tolerant Inputs
V_{IL}	TTL input LOW voltage	0	—	0.8	V	
I_{IH}	TTL input HIGH current	—	50	500	µA	V_{IN} =2.4V
I_{IL}	TTL input LOW current	—	—	-500	µA	V_{IN} =0.5V
PECL Input (REF+/REF-)						
V_{IH}	PECL input HIGH voltage	V_{DD} - 1.1	—	V_{DD} - 0.7	V	
V_{IL}	PECL input LOW voltage	V_{DD} - 2.0	—	V_{DD} - 1.5	V	
I_{IH}	PECL input HIGH current	—	—	200	µA	V_{IN} =$V_{IH(MAX)}$
I_{IL}	PECL input LOW current	- 50	—	—	µA	V_{IN} =$V_{IL(MIN)}$
ΔV_{IN}	PECL input differential peak-to-peak voltage swing	400	—	—	mV	$V_{IH(MIN)}$ - $V_{IL(MAX)}$
High Speed Outputs						
ΔV_{OUT75}(1)	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V (TX+) - (TX-)
ΔV_{OUT50}(1)	TX Output differential peak-to-peak voltage swing	1000	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V (TX+) - (TX-)
High Speed Inputs						
ΔV_{IN}(1)	PECL differential peak-to-peak input voltage swing	200	—	2600	mV	Rx+ - Rx-
Miscellaneous						
V_{DD}	Power supply voltage	3.14	—	3.47	V	3.3V ± 5%
P_D	Power dissipation	—	2.2	2.67	W	Max at 3.47V, outputs open, 136MHz Clk, PRBS 2-7, parallel input pattern, at +25ºC.
I_{DD}	Supply current (All Supplies)	—	—	770	mA	
I_{DDA}	Supply current on V_{DDA}	—	100	—	mA	

NOTE: (1) Refer to Application Note, AN-37, for differential measurement techniques.

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{DD}) ..... -0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL outputs) ..... +/-50mA
Output Current (PECL outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+125^{o}$C
Storage Temperature ..... -65^{o}C to $+150^{o}$C

NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) ..... +3.3V$\pm$5%
Operating Temperature Range ..... 0^{o}C Ambient to $+100^{o}$C Case Temperature

Table 6: Pin Table

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSST	VDD	VSST	SYNCB	RCB0	RB0	RB4	RB6	VDDT	VDD	VSST	RC1	VDDT	RC8	VSST	VDDT	VSST
B	RA7	RA8	RA9	VSST	RCB1	RB1	VDDT	RB7	VSS	SYNCC	RC0	RC2	RC5	RC9	SYNCD	RCD0	RCD1
C	RA4	RA5	RA6	VDDT	VDDT	RB2	VSST	RB8	SLPN	RCC0	VDDT	RC3	RC6	VDD	VDDT	VSST	RD0
D	RA0	RA1	VDDT	VSST	LPND	RB3	RB5	RB9	TMS	RCC1	VSST	RC4	RC7	RD1	RD2	RD3	RD4
E	RCA0	RCA1	RA2	RA3										VDDT	VSST	RD5	RD6
F	TBCB	SYNCA	VDDT	VSST										RD7	RD8	RD9	VSS
G	TB8	TB9	VSS	VDD										TC2	TC1	TC0	VDDT
H	TB4	TB5	TB6	TB7										TC6	TC5	TC4	TC3
J	TB0	TB1	TB2	TB3										VDD	TC9	TC8	TC7
K	TBCA	TDO	VSS	LPNC										VSS	VSS	VDD	TBCC
L	TA8	TA9	VSS	VDD										TD3	TD2	TD1	TD0
M	TA4	TA5	TA6	TA7										TD7	TD6	TD5	TD4
N	TA0	TA1	TA2	TA3										PLUP	VDD	TD9	TD8
P	LTCN	RFCM	REF-	LPNB	TA-	VSS	TB-	VSS	CAP0	VSS	TC+	VSS	TD+	RFCO1	TD1	RFCO0	TBCD
R	REFT	REF+	LPNA	VDD	TA+	VSS	TB+	VSSA	CAP1	VSS	TC-	VSS	TD-	VDD	TRSTN	VDDTR	ENCDET
T	RCM	VSS	VDD	VDD	VDDPA	VSS	VDDPB	VSS	VDDA	VSS	VDDPC	VSS	VDDPD	VDD	VSS	VSSTR	TCK
U	VSS	VSS	RA-	RA+	VDD	RB-	RB+	VSS	VSS	RC-	RC+	VSS	RD-	RD+	VSS	VSS	VSS

NOT POPULATED

Table 7: Pin Identifications

Pin	*Name*	*Description*
N1, N2, N3 N4, M1, M2, M3, M4, L1 L2	TA0, TA1, TA2 TA3, TA4, TA5 TA6, TA7, TA8 TA9	INPUT - TTL: 10-bit Transmit bus for Channel A. Parallel data on this bus is latched on the rising edge of REF, TBCC or TBCA. TA0 is transmitted first.
J1, J2, J3 J4, H1, H2 H3, H4, G1 G2	TB0, TB1, TB2 TB3, TB4, TB5 TB6, TB7, TB8 TB9	INPUT - TTL: 10-bit Transmit bus for Channel B. Parallel data on this bus is latched on the rising edge of REF, TBCC or TBCB. TB0 is transmitted first.
G16, G15, G14 H17, H16, H15 H14, J17, J16 J15	TC0, TC1, TC2 TC3, TC4, TC5 TC6, TC7, TC8 TC9	INPUT - TTL: 10-bit Transmit bus for Channel C. Parallel data on this bus is latched on the rising edge of REF or TBCC. TC0 is transmitted first.
L17, L16, L15 L14, M17, M16 M15, M14, N17 N16	TD0, TD1, TD2 TD3, TD4, TD5 TD6, TD7, TD8 TD9	INPUT - TTL: 10-bit Transmit bus for Channel D. Parallel data on this bus is latched on the rising edge of REF, TBCC or TBCD. TD0 is transmitted first.
R2 P3	REF+ REF-	INPUT - Differential PECL or TTL: This rising edge of REF+/- provides the reference clock, at 1/10th or 1/20th of the baud rate (depending on RFCM) to the Clock Multiplying PLL. If REF+/- is used, either leave REFT open or set REFT HIGH. Internally biased to VDD/2. If all TBCx inputs are HIGH, the rising edge of REF will latch Tx(0:9) on all four channels
R1	REFT	INPUT - TTL: TTL REFerence clock. This rising edge of REFT provides the reference clock, at 1/10th or 1/20th of the baud rate (depending on RFCM) to the Clock Multiplying PLL. If REFT is used, set REF+ HIGH and leave REF- open. If all TBCx inputs are HIGH, the rising edge of REFT will latch Tx(0:9) on all four channels
P2	RFCM	INPUT - TTL: REFerence clock Mode select. When LOW, REF is at 1/20th of the transmit baud rate (i.e. 62.5 MHz for 1.25 Gb/s). When HIGH, REF is at 1/10th the baud rate (i.e. 125 MHz for 1.25 Gb/s).
P16 P14	RFCO0 RFCO1	OUTPUT - TTL: These are identical copies of the transmit baud rate clock divided by 10.
K1, F1 K17, P17	TBCA, TBCB TBCC, TBCD	INPUT - TTL: Per channel Transmit Byte Clock for Channel x. All four channels' parallel Tx(0:9) inputs may be timed to REF, TBCC, or independently to TBCx. Refer to the Serializer description.
P1	LTCN	INPUT - TTL: Latch Transmit Byte Clocks. When LOW, internal PLLs align clocks with each of the transmit byte clocks, if present. Data may be corrupted when LOW. When HIGH, alignment will remain static regardless of actual TBCx location.

Pin	Name	Description
R5, P5 R7, P7 P11, R11 P13, R13	TA+, TA- TB+, TB- TC+, TC- TD+, TD-	OUTPUT - Differential PECL (AC Coupling recommended) These pins output the serialized transmit data for Channel x when PLUP is LOW. When PLUP is HIGH, Tx+ is HIGH and Tx- is LOW.
D1, D2, E3 E4, C1, C2 C3, B1, B2 B3	RA0, RA1, RA2 RA3, RA4, RA5 RA6, RA7, RA8 RA9	OUTPUT - TTL: 10-bit Receive bus for Channel A. Parallel data on this bus is synchronous to RCA0 and RCA1. RA0 is the first bit received.
A6, B6, C6 D6, A7, D7 A8, B8, C8 D8	RB0, RB1, RB2 RB3, RB4, RB5 RB6, RB7, RB8 RB9	OUTPUT - TTL: 10-bit Receive bus for Channel B. Parallel data on this bus is synchronous to RCB0 and RCB1. RB0 is the first bit received.
B11, A12, B12 C12, D12, B13 C13, D13, A14 B14	RC0, RC1, RC2 RC3, RC4, RC5 RC6, RC7, RC8 RC9	OUTPUT - TTL: 10-bit Receive bus for Channel C. Parallel data on this bus is synchronous to RCC0 and RCC1. RC0 is the first bit received.
C17, D14, D15 D16, D17, E16 E17, F14, F15 F16	RD0, RD1, RD2 RD3, RD4, RD5 RD6, RD7, RD8 RD9	OUTPUT - TTL: 10-bit Receive bus for Channel D. Parallel data on this bus is synchronous to RCD0 and RCD1. RD0 is the first bit received.
T1	RCM	INPUT - TTL: Recovered clock MODE control. When LOW, RCx0/RCx1 is 1/20th of the incoming baud rate. When HIGH, RCx0/RCx1 is 1/10th the incoming baud rate.
E1 E2	RCA0 RCA1	OUTPUT - Complementary TTL: Recovered complementary clocks for Channel A at 1/10th the incoming baud rate (RCM=HIGH) or 1/20th (RCM=LOW). Synchronous to the RA(0:9) and SYNCA bus.
A5 B5	RCB0 RCB1	OUTPUT - Complementary TTL: Recovered complementary clocks for Channel B at 1/10th the incoming baud rate (RCM=HIGH) or 1/20th (RCM=LOW). Synchronous to the RB(0:9) and SYNCB bus.
C10 D10	RCC0 RCC1	OUTPUT - Complementary TTL: Recovered complementary clocks for Channel C at 1/10th the incoming baud rate (RCM=HIGH) or 1/20th (RCM=LOW). Synchronous to the RC(0:9) and SYNCC bus.
B16 B17	RCD0 RCD1	OUTPUT - Complementary TTL: Recovered complementary clocks for Channel D at 1/10th the incoming baud rate (RCM=HIGH) or 1/20th (RCM=LOW). Synchronous to the RD(0:9) and SYNCD bus.
U4, U3 U7, U6 U11, U10 U14, U13	RA+, RA- RB+, RB- RC+, RC- RD+, RD-	INPUT - Differential PECL (AC Coupling recommended): Serial receive data inputs for Channel x which are selected when PLUP is LOW. [Internally biased to VDD/2]
N14	PLUP	INPUT - TTL: Parallel Loopback Enable input. Rx is input to the CRU for Channel x (normal operation) when PLUP is LOW. When HIGH, internal loopback paths from Tx to Rx are enabled. Refer to Table 2.

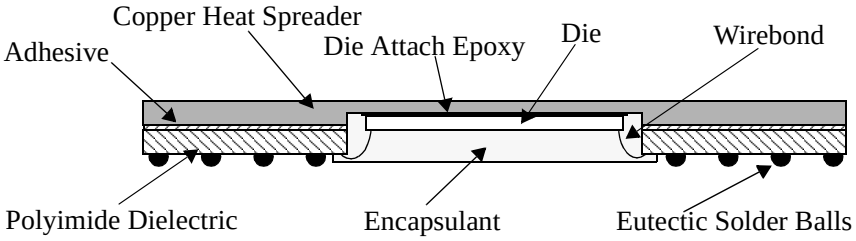
Pin	*Name*	*Description*
C9	SLPN	INPUT - TTL: Serial Loopback enable input. Normal operation when HIGH. When LOW, Rx+/- is looped back to Tx+/- internally for diagnostic purposes. Refer to Table 2 and related description.
R3 P4 K4 D5	LPNA LPNB LPNC LPND	INPUT - TTL: Loopback Enable Pins. When LPNx is LOW, PLUP/SLPN impact Channel x. When HIGH, PLUP/SLPN have no effect on Channel x.
R17	ENCDET	INPUT - TTL: Enables SYNCx and word alignment when HIGH. When LOW, keeps current word alignment and disables SYNCx (always LOW).
F2 A4 B10 B15	SYNCA SYNCB SYNCC SYNCD	OUTPUT - TTL: Comma Detect for Channel x. This output goes HIGH for half of an RCx1 period to indicate that Rx(0:9) contains a Comma Character (‘0011111XXX’). SYNCx will go HIGH only during a cycle when RCX0 is rising. SYNCx is enabled when ENCDET is HIGH.
P9 R9	CAP0 CAP1	ANALOG: Loop Filter capacitor for the Clock Multiply Unit. Typically 0.1 uF connected between CAP0 and CAP1. Amplitude is less than 3.3V.
T17	TCK	INPUT - TTL: JTAG Test Clock
D9	TMS	INPUT - TTL: JTAG Test Mode Select
R15	TRSTN	INPUT - TTL: JTAG Test Reset, Active Low
P15	TDI	INPUT - TTL: JTAG Test Data Input
K2	TDO	OUTPUT - TTL: JTAG Test Data Output
T9	VDDA	Analog Power Supply
R8	VSSA	Analog Ground. Tie to common ground plane with VSS.
A2,A10,C14 G4,J14,K16 L4,N15,R4 R14,T3 T4,T14,U5	VDD	Digital Logic Power Supply
C4, D3,F3 A9, B7, C5 A13, A16, C11 C15, E14, G17	VDDT	TTL Output Power Supply.
T5 T7 T11 T13	VDDPA VDDPB VDDPC VDDPD	PECL I/O Power Supply for Channel x.
R16	VDDTR	TTL Output Power Supply for RFCO0 and RFCO1
T16	VSSTR	TTL Ground for RFCO0 and RFCO1
A1,A3,A11,A15 A17,B4,C7 C16,D4,D11 E15,F4	VSST	Ground for TTL Outputs

Pin	*Name*	*Description*
B9,F17,G3,K3, K14,K15,L3,P6, P8,P10,P12 R6,R10,R12,T2T 6,T8,T10,T12T1 5,U1,U2,U8,U9, U12,U15 U16, U17	VSS	Ground

Package Thermal Characteristics

The VSC7139 is packaged in a 23 mm BGA package with 1.27mm eutectic ball spacing. The construction of the package is shown in Figure 6.

Figure 6: Package Cross Section



The VSC7139 is designed to operate with a case temperature up to 100°C. In order to comply with this target, the user must guarantee that the case temperature specification of 100°C is not violated. With the Thermal Resistances shown in Table 8, the VSC7139 can operate in still air ambient temperatures of 56.75°C [56.75°C = 100°C - 2.5W * 17.3°C/W]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided.

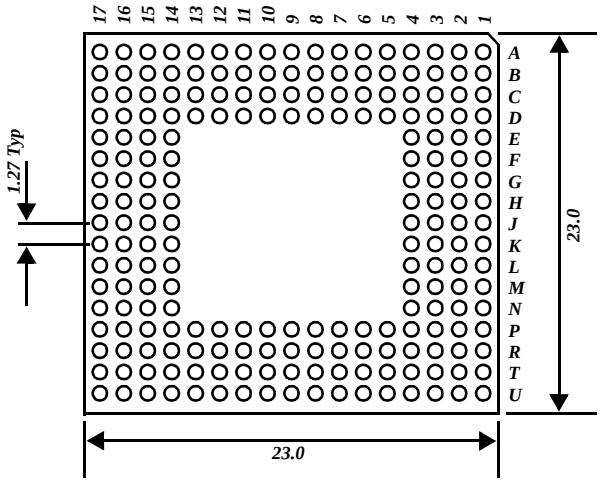
Table 8: Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	1.0	°C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads.	17.3	°C/W
θ_{ca-100}	Thermal resistance from case to ambient with 100 LFM airflow	15.7	°C/W
θ_{ca-200}	Thermal resistance from case to ambient with200 LFM airflow	14.5	°C/W
θ_{ca-400}	Thermal resistance from case to ambient with 400 LFM airflow	13.0	°C/W
θ_{ca-600}	Thermal resistance from case to ambient with 600 LFM airflow	12.0	°C/W

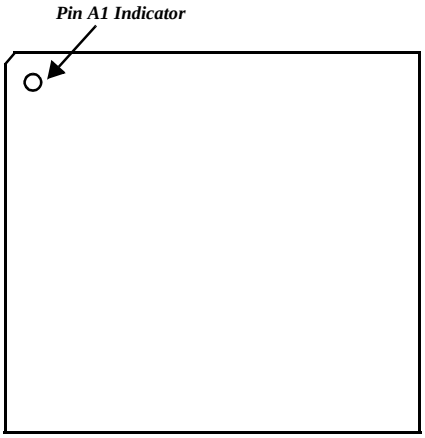
Moisture Sensitivity Level

This device is rated at a Moisture Sensitivity Level 3 rating with maximum floor life of 168 hours at 30ºC, 60% relative humidity. Please refer to Application Note AN-20 for appropriate handling procedures.

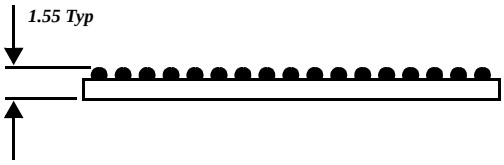
Package Information



BOTTOM VIEW

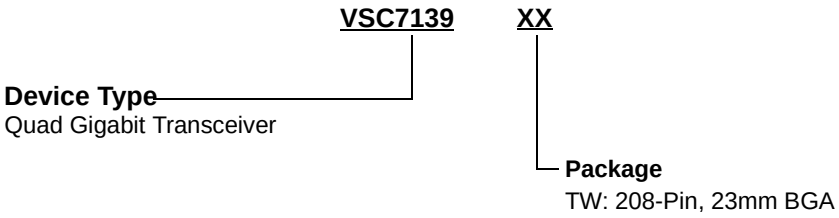


TOP VIEW



Order information

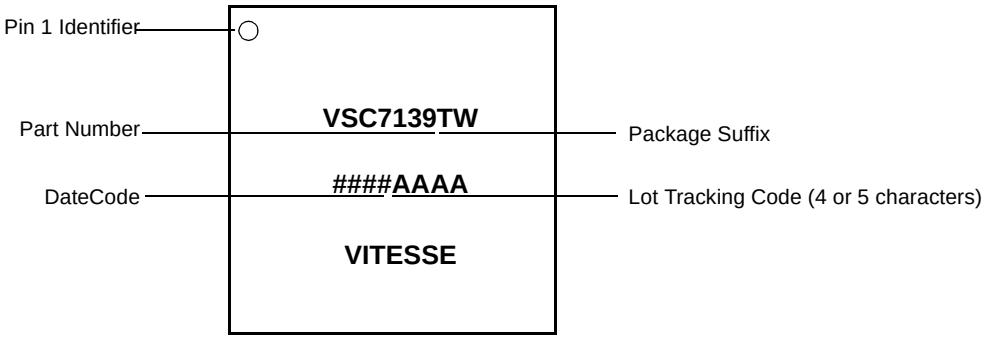
The order number for this product is formed by a combination of the device number, and package type.



Marking Information

The top of the package is marked as in Figure 7.

Figure 7: Package Marking Information



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