VSC7173 Data Sheet

Enhanced 2:1 Port Selector and 1:2 Port Multiplier for Serial ATA and Serial Attached SCSI

FEATURES

- 2:1 port selector and 1:2 port multiplier for both Serial ATA (SATA) and Serial Attached SCSI (SAS) links
- Serial ATA 1.0 compliant at 1.5 Gbps (3.0 Gbps capable)
- Passes Serial ATA patterns transparently
- Programmable receiver sensitivity
- High output swing mode with pre-emphasis
- Compatible with VSC7175 and VSC7177 designs
- 0.7 W power dissipation
- 3.3 V power supply
- 32-pin, 7 mm x 7 mm QFP-N package

APPLICATIONS

- Active-passive redundant failover systems
- Dual-port Serial ATA and Serial Attached SCSI disk arrays (JBODs)
- NAS servers
- RAID subsystems
- Disk-based backup systems
- Serial ATA and Serial Attached SCSI routing applications
- Buffers for externally connected links
- Serial ATA port replicators
- Serial ATA Host Bus Adapters selecting between internal and external connectors

To order the VSC7173 device, see "Ordering Information," page 17.

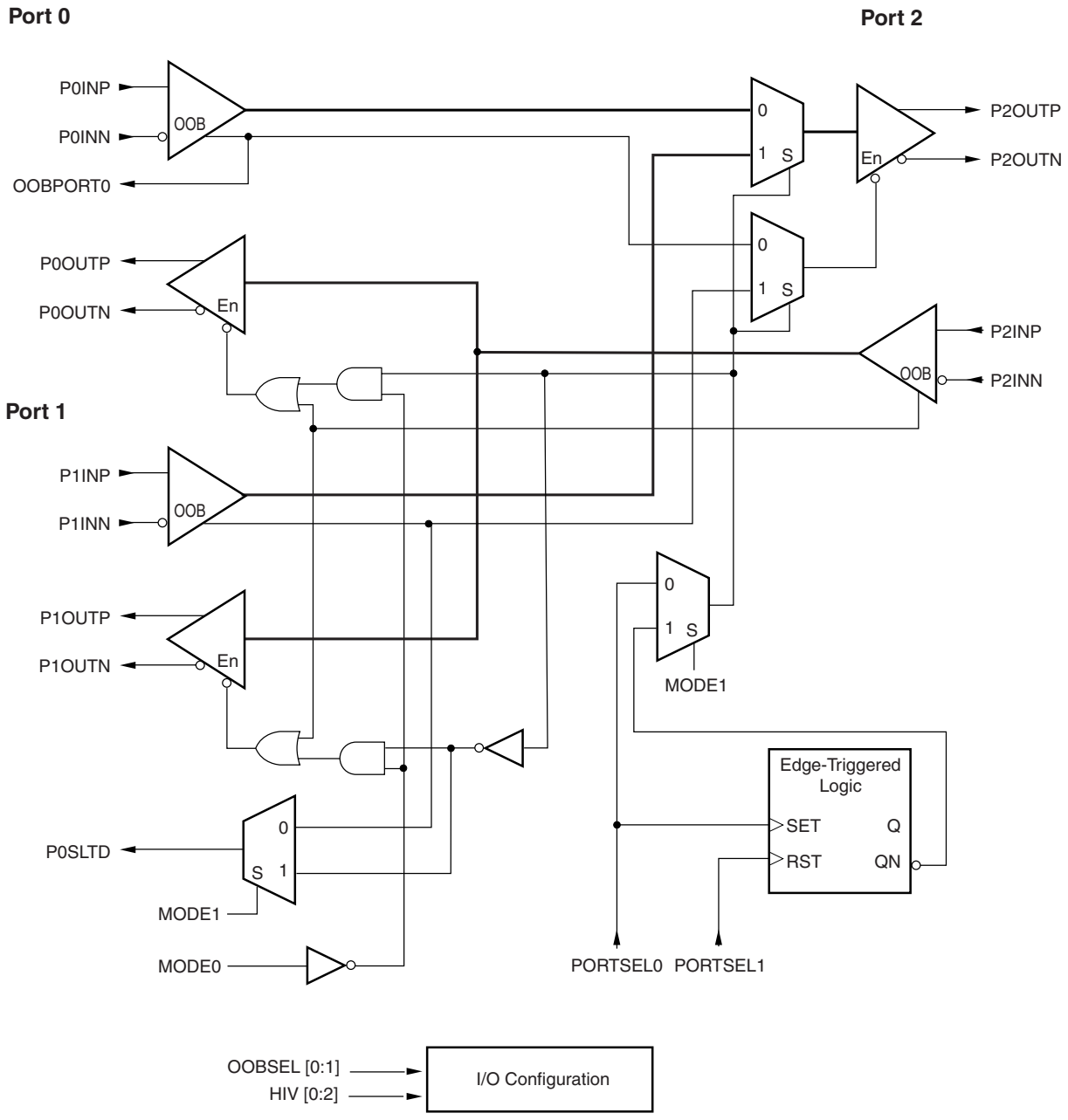
GENERAL DESCRIPTION

The VSC7173 is a Serial ATA and Serial Attached SCSI multiplexer and buffer that implements a 2:1 port selector function for 1.5 Gbps and 3.0 Gbps links. This function is used when dual hosts, such as I/O controllers, must access single-port disk drives in high availability storage subsystems where redundancy and load sharing are important. The outputs from the I/O controllers are multiplexed to a Serial ATA or Serial Attached SCSI drive. The output from the Serial ATA drive is buffered and replicated to the I/O controllers. When switching from one I/O controller to the other, a Serial ATA link must be re-initialized with out-of-band (OOB) signals, which are transferred through the VSC7173 transparently. The VSC7173 provides high output swings with pre-emphasis, and programmable receiver sensitivity that are needed to drive long backplanes and external cables.

In addition to the above features, the VSC7173 also supports a 1:2 port multiplier mode where one host can connect two drives.

Port connectivity for the device is configured by driving external I/O pins. See the block diagram on page 2.

VSC7173 Block Diagram



Application Examples

The VSC7173 allows two Serial ATA hosts to access one Serial ATA drive. Figure 1 shows a common application where redundant I/O controllers in disk arrays have multiplexed access to single-port Serial ATA disk drives.

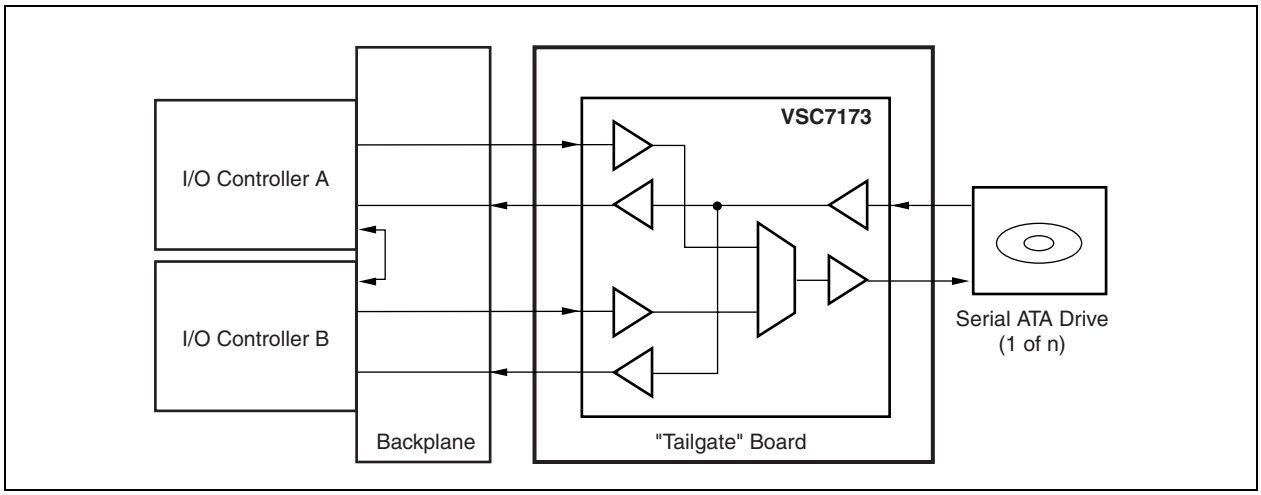


Figure 1. Serial ATA Backplane Application

Another application example (Figure 2) is for simple port replication to enable an existing Serial ATA Host Bus Adapter (HBA) to connect to two ports. By using the VSC7173, a single channel from the HBA may be selectively connected to an internal connector or an external connector. The VSC7173 provides both the mulitplexing functionality and buffering to drive external connections.

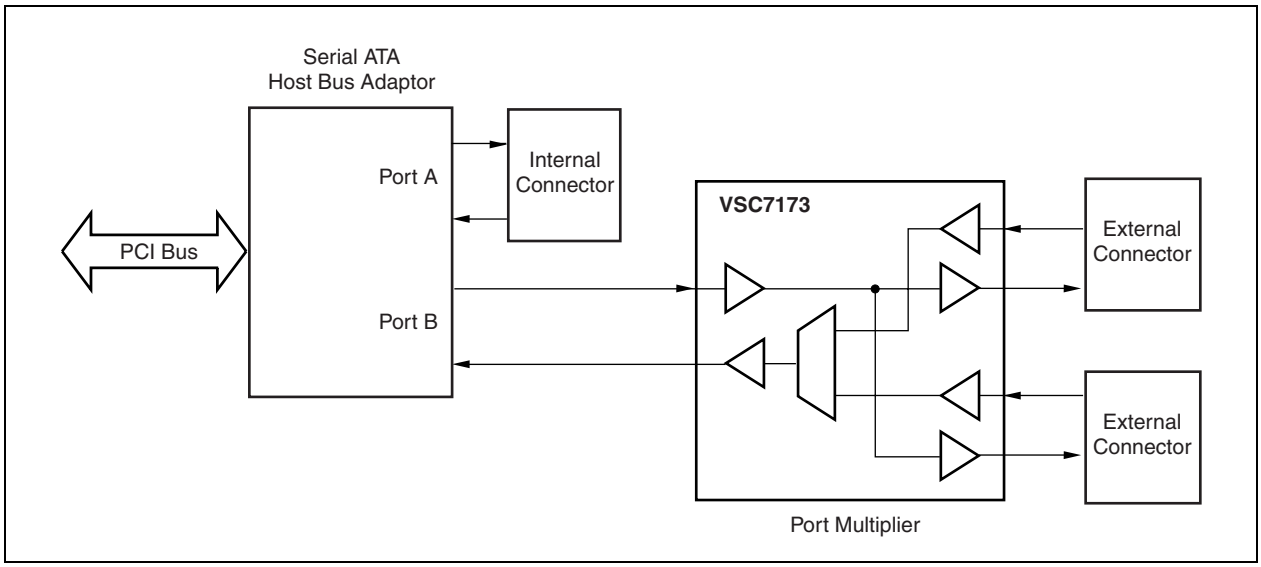


Figure 2. Port Multiplier Application

FUNCTIONAL DESCRIPTIONS

Modes of Operation

Table 1 summarizes the VSC7173 operational mode choices. The mode of the VSC7173 is determined by the following pins.

MODE1: Controls whether the selection of port 0 to port 1 is edge-sensitive or level-sensitive. When LOW, port selection is level-sensitive (to enable level-sensitive port selection, pin PORTSEL1 must also be LOW). When HIGH, port selection is edge-sensitive.

MODE0: Controls the function of the unselected port. When LOW, the output of this port is turned off. When HIGH, the output of this unselected port is the same data as seen on the selected port.

PORTSEL0: In level-sensitive mode (MODE1 is LOW and PORTSEL1 is LOW), controls the selection of port 0 or port 1. When LOW, port 0 is selected; when HIGH, port 1 is selected. In edge-sensitive mode (MODE1 is HIGH), controls the selection of port 0; a rising edge on this pin selects port 0.

PORTSEL1: In level-sensitive mode (MODE1 is LOW), must be held LOW. In edge-sensitive mode (MODE1 is HIGH), controls the selection of port 1; a rising edge on this pin selects port 1.

Table 1. Port Selection Operating Modes

Input Pins				High-Speed Connections		
MODE1	MODE0	PORTSEL0	PORTSEL1	P0OUT	P1OUT	P2OUT
0 (level)	0	0	0	P2IN	OFF	P0IN
0 (level)	0	1	0	OFF	P2IN	P1IN
0 (level)	1	0	0	P2IN	P2IN	P0IN
0 (level)	1	1	0	P2IN	P2IN	P1IN
1 (edge)	0	X	↑	OFF	P2IN	P1IN
1 (edge)	0	↑	X	P2IN	OFF	P0IN
1 (edge)	1	X	↑	P2IN	P2IN	P1IN
1 (edge)	1	↑	X	P2IN	P2IN	P0IN

X = don't care; ↑ = rising.

Status Pins

Two output pins, P0SLTD and OOBPORT0, are provided for status monitoring. Table 2 summarizes the functionality of these two output pins. OOBPORT0 reports whether the signal on port 0 is above or below the threshold selected in Table 5. P0SLTD, depending on the state of MODE1, can either report which port is selected or can report whether the signal on port 1 is above or below the threshold selected in Table 5.

Table 2. Output Status Pins

Input Pins			Output Status Pins	
MODE1	PORTSEL0	PORTSEL1	P0SLTD	OOBPORT0
0 (level)	X	X	OOB status port 1—1 indicates signal is below OOB threshold, 0 indicates signal is above OOB threshold	OOB status port 0—1 indicates signal is below OOB threshold, 0 indicates signal is above OOB threshold
1 (edge)	X	↑	Indicates port selected, 0 = port 1	OOB status port 0
1 (edge)	↑	X	Indicates port selected, 1 = port 0	OOB status port 0

X = don't care; ↑ = rising.

Reset State

The power-up state of the VSC7173 is based on the PORTSEL0 and PORTSEL1 input signals. When in level-sensitive mode, the active port connected to port 2 is controlled directly by the PORTSEL0 input. This is the same behavior as the normal operating condition described above. When in edge-sensitive mode, the active port connected to port 2 is defined in Table 3. The state diagram in Figure 3 indicates the same result in a different format.

Table 3. Power-up State (Edge-Sensitive Mode)

PORTSEL0	PORTSEL1	Active Port	P0SLTD Output
0	0	Port 0 selected	1
1	0	Port 0 selected	1
0	1	Port 1 selected	0
1	1	Port 0 selected	1

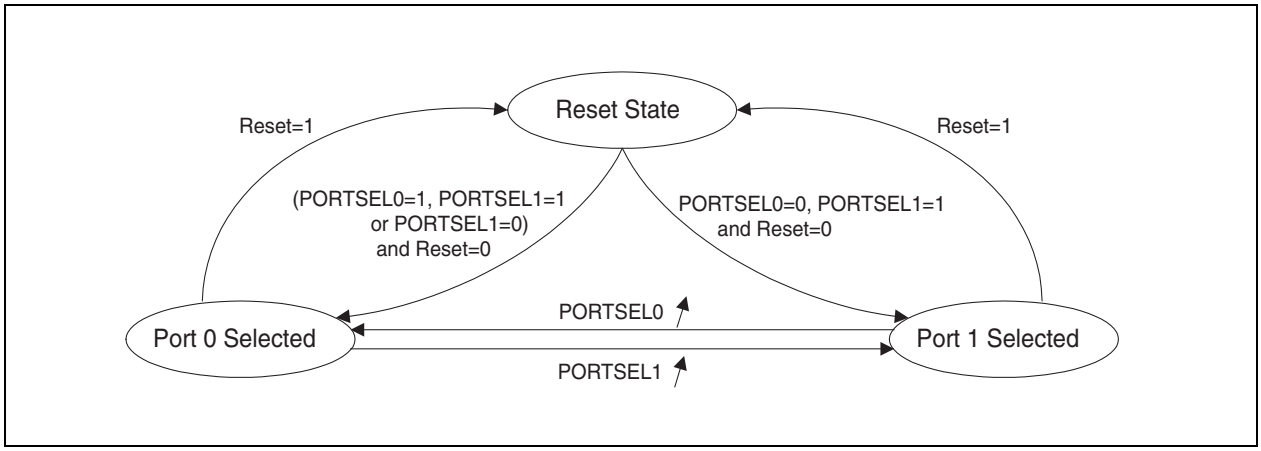


Figure 3. Reset State Machine (Edge-Sensitive Mode)

High-Speed Outputs

Each port has a high-speed output buffer that transmits the differential serial ATA data at rates up to 3.0 Gbps. The output pins for the ports are P0OUTP/N, P1OUTP/N, and P2OUTP/N. Each output buffer has an input to indicate when OOB signals are being transmitted and a single input to control the output voltage amplitude and to enable pre-emphasis.

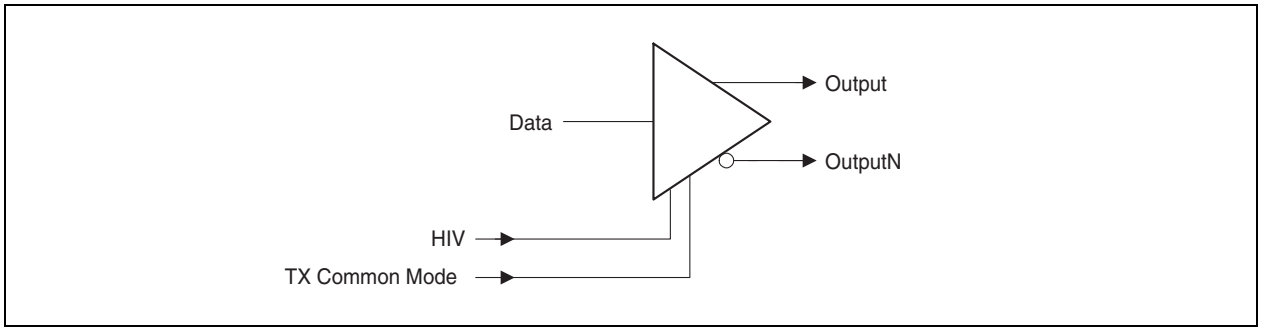


Figure 4. High-Speed Output Buffer

Transmitting OOB Signals

Both differential output signals are at the DC-bias voltage when the output buffer is disabled. The output buffer is disabled when OOB signals are transmitted and when an output port is turned "off." For more information, see "Functional Descriptions," page 4.

Output Amplitude and Pre-Emphasis

Each of the output buffers has an amplitude control input pin, the state of which sets the differential output voltage (within normal SATA levels). Pin HIV0 corresponds to port 0, pin HIV1 corresponds to port 1, and pin HIV2 corresponds to port 2. See Table 4. Recommended output AC-coupling capacitor values are 0.01 µF. When the amplitude control pin is HIGH, the output is configured for high voltage swing mode, which is useful for driving extended length media such as backplanes or external cables. Setting the output to high swing mode should be done only in controlled environments, because the output voltage exceeds the Serial ATA 1.0 differential mode specifications.

The output buffers have a pre-emphasis circuit that is enabled when HIVx is HIGH. Pre-emphasis accentuates higher frequency signals in a transmitted data stream. This feature takes into consideration that a signal loses amplitude and affects the data eye opening as it goes through long trace length runs. Figure 5 shows the effects of the pre-emphasis feature. The amplitude increase is between 20% and 30%, and the duration of the amplitude increase is between 150 ps and 300 ps.

Table 4. Output Amplitude and Pre-Emphasis

HIVx Pin State	Output Swing Level	Pre-Emphasis
0	Normal	None
1	High	Enabled

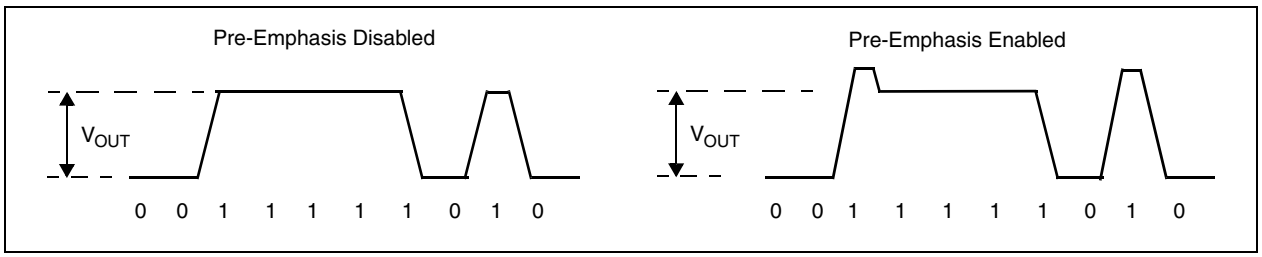


Figure 5. Pre-Emphasis Diagram

High-Speed Inputs

The high-speed input receivers are designed to achieve Serial ATA 1.0 compliance using AC-coupling as described in the Serial ATA 1.0 specification. Recommended input AC-coupling capacitor values are 0.01 µF. The high-speed input receiver contains an OOB signal detector as shown in Figure 6.

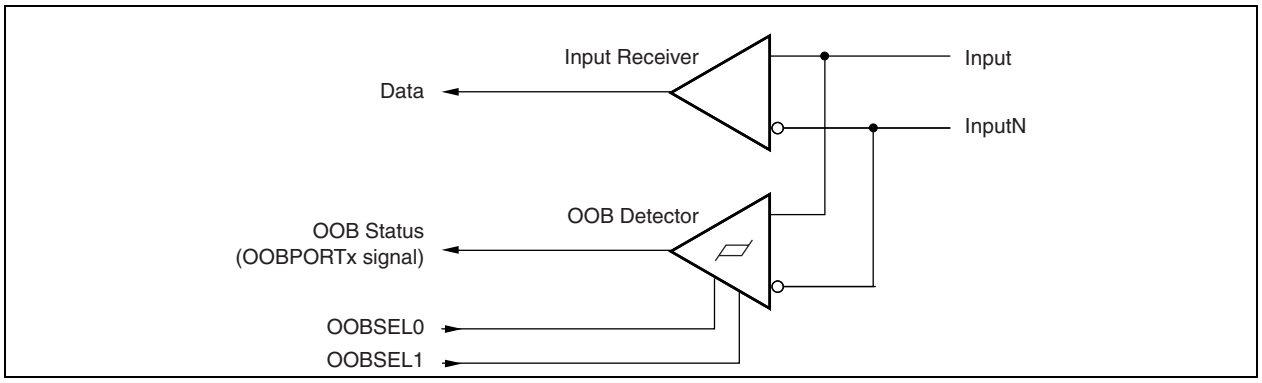


Figure 6. High-Speed Input Receiver

OOB Transfer

The VSC7173 cleanly transfers OOB signals from high-speed inputs to outputs. Two status outputs, OOBPORT0 and OOBPORT1, indicate whether the input signal is data or a common-mode state. OOBPORT1 and OOBPORT1 correspond to port 0 and port 1, respectively. An OOB detector monitors the amplitude of an incoming signal in parallel with each high-speed input. When the amplitude is less than the OOB threshold, the OOB status output is driven HIGH. When the incoming amplitude is greater than the OOB threshold, the OOB status output is driven LOW.

Setting the OOBSEL1 and OOBSEL0 inputs as shown in the following table configures the OOB threshold level for all three ports.

Table 5. Setting the OOB Threshold Level

OOBSEL1	OOBSEL0	OOB THRESHOLD LEVEL
1	0	Nominal setting (150 mV to 250 mV)
0	0	Decrease by ~40 mV
0	1	Decrease by ~80 mV
1	1	Increase by ~40 mV

NOTE: *All values are differential peak-to-peak voltages.*

ELECTRICAL SPECIFICATIONS

DC Characteristics

Specifications are guaranteed over the recommended operating conditions listed in Table 11.

Table 6. LVTTL Inputs and Outputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{OH}	Output HIGH voltage	2.0	2.2	V_{DD}	V	I_{OH} = –4 mA
V_{OL}	Output LOW voltage	0.0	0.2	0.4	V	I_{OL} = 4 mA
V_{IH}	Input HIGH voltage	2.0		V_{DD}	V	
V_{IL}	Input LOW voltage	0.0		0.8	V	
I_I	Input current (includes a weak pull-up resistor)	–200		+50	µA	0V < V_{IL} < 2.4 V

Table 7. High-Speed Inputs and Outputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{TH}	Input threshold voltage for OOB detection		200		mV	See Table 5 on page 7.
V_{OCM}	High-speed output common-mode voltage		2.0		V	Normal Swing mode. 100 Ω termination between true and complement outputs.
			1.7		V	High Swing mode. 100 Ω termination between true and complement outputs.
V_{ICM}	High-speed input common-mode voltage		1.5		V	
Z_{IN}	Differential input impedance	85	100	115	Ω	

Table 8. Power Supply Requirements

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{DD}	Power supply voltage	3.0	3.3	3.6	V	±10% on all supplies
I_{DD}	Power supply current (total on all supply pins)		150	170	mA	Normal Swing mode
			200	235	mA	High Swing mode
P_D	Total power dissipation		540	625	mW	Normal Swing mode
			720	850	mW	High Swing mode

AC Characteristics

Specifications are guaranteed over the recommended operating conditions listed in Table 11 on page 11.

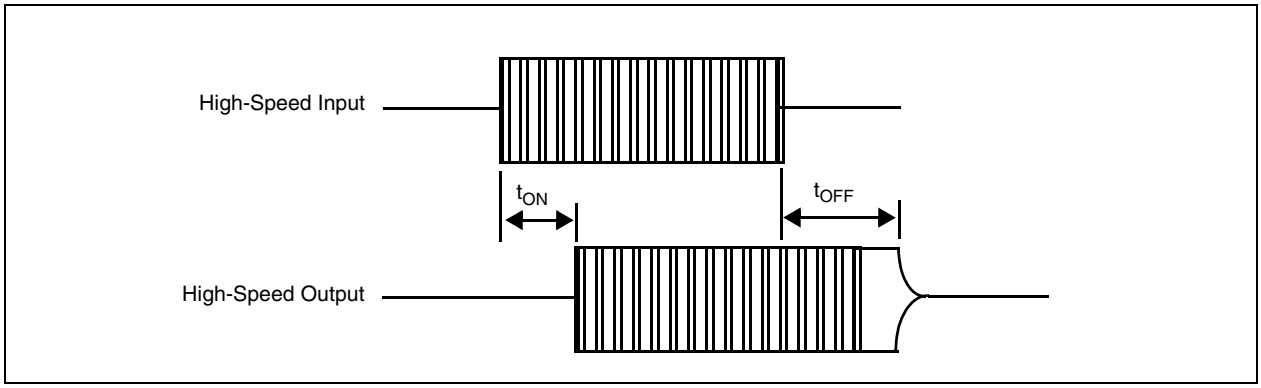
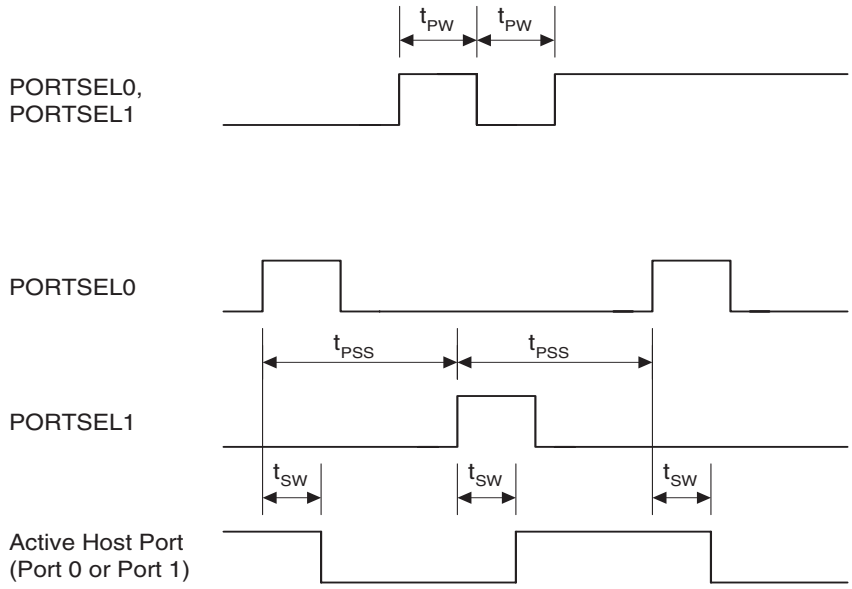


Figure 7. Timing Waveform

Table 9. High-Speed Inputs and Outputs

Symbol	Parameter	Minimum	Maximum	Unit	Condition
t_P	Propagation delay from any high-speed input to high-speed output	0.4	2.0	ns	
t_{ON}	Propagation delay from signal present at input to output buffer turned on	3.0	12.0	ns	
t_{OFF}	Propagation delay from no signal at input to output buffer turned off	3.0	12.0	ns	
t_R, t_F	Rise and fall times	67	260	ps	1.5 Gbps operation, 20% to 80%.
V_{OUT}(1)	OUTx output differential peak-to-peak voltage swing in normal swing mode (HIVx is LOW)	500	700	mVp-p	Measured per Serial ATA 1.0 specification, section 6.6.3. 100 Ω termination between true and complement outputs.
V_{OUT}(1, 2)	OUTx output differential peak-to-peak voltage swing in high swing mode (HIVx is HIGH)	800	1300	mVp-p	Measured per Serial ATA 1.0 specification, section 6.6.3. 100 Ω termination between true and complement outputs.
V_{IN}	INx input differential peak-to-peak swing with OOBSEL1 = 1 and OOBSEL0 = 0 (OOB nominal)	275	1600	mVp-p	Measured per Serial ATA 1.0 specification.
V_{IN}	INx input differential peak-to-peak swing with OOBSEL1 = 0 and OOBSEL0 = 1 (OOB minimal)	225	1600	mVp-p	Measured per Serial ATA 1.0 specification, section 6.6.3.

1. *Refer to Application Note AN-37 for differential measurement techniques.*
2. *Output swings are higher than the Serial ATA 1.0 specification to compensate for anticipated PCB or connector losses.*



Note: Edge-sensitive operation shown.

Figure 8. Timing Waveform for Port Switching

Table 10. Port Switch Timing

Symbol	Parameter	Minimum	Maximum	Unit	Condition
t_{PW}	Pulse width of the port selection pins (PORTSEL0, PORTSEL1).	4.0		ns	
t_{PSS}	Separation between rising edge transitions of the port selection pins.	5.0		ns	Edge-sensitive operation
t_{SW}	Switch time. The time required to make the other host port active following an active edge transition of the port selection pins.		5.0	ns	Applies to both level and edge-sensitive operations

Operating Conditions

Table 11. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Power supply voltage	3.0	3.3	3.6	V
T	Operating temperature(1)	0		+90	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

Maximum Ratings

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Power supply voltage	–0.5	+4.0	V
V_{INT}	LVTTL input voltage	–0.5	V_{DD} + 0.5	V
V_{OUTT}	LVTTL output voltage	–0.5	V_{DD} + 0.5	V
I_{OT}	LVTTL output current	–50	+50	mA
V_{INS}	Serial input voltage	–0.5	V_{DD} + 0.5	V
V_{OUTS}	Serial output voltage	–0.5	V_{DD} + 0.5	V
I_{OS}	Serial output current	–50	+50	mA
T_S	Storage temperature	–65	+140	°C
V_{ESD}	Electrostatic voltage discharge, human body model	–4000	+4000	V

Stresses listed under Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

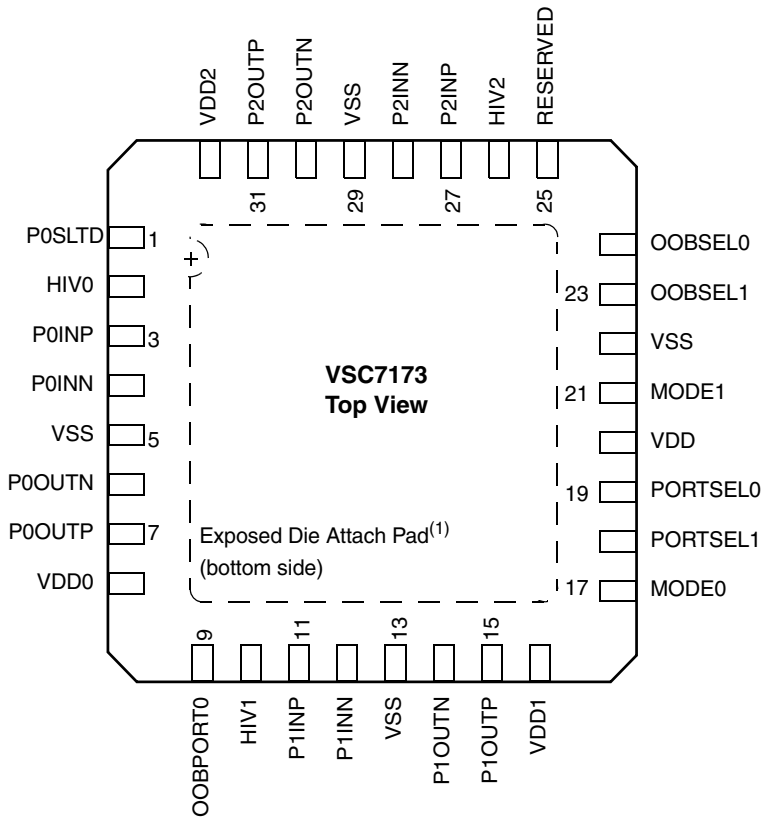
ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Maxim recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PIN DESCRIPTIONS

The VSC7173 is packaged in a 32-pin, leadless quad flat pack (QFP-N) with an exposed pad.

Pin Diagram



1. The exposed Die Attach Pad (DAP) is internally connected to ground and should also be connected to VSS on the board.

Figure 9. Pin Diagram

Pin Identifications

Table 13. Pin Identifications

Pin Number	Signal	Type	Level	Description
7, 6 15, 14 31, 30	P0OUTP, P0OUTN P1OUTP, P1OUTN P2OUTP, P2OUTN	O	High-Speed	These are the high-speed differential outputs for port 0, port 1, and port 2. These outputs must be AC-coupled.
3, 4 11, 12 27, 28	P0INP, P0INN P1INP, P1INN P2INP, P2INN	I	High-Speed	These are the high-speed differential inputs for port 0, port 1, and port 2. These inputs must be AC-coupled.
19 18	PORTSEL0 PORTSEL1	I	LVTTL	These two inputs select the active port (port 0 or port 1). For more information on the modes of operation, see Table 1 on page 4.
2 10 26	HIV0 HIV1 HIV2	I	LVTTL	When HIGH, these inputs select the high voltage swing output mode for the corresponding output buffer and enable pre-emphasis. See Table 4 on page 6.
24 23	OOBSEL0 OOBSEL1	I	LVTTL	These two inputs control the OOB detector threshold voltage for all three input ports. See Table 5 on page 7 for threshold levels.
1	P0SLTD	O	LVTTL	This output reports which port is selected or OOB status of port 1, depending on the value of MODE1. See Table 2 on page 4.
9	OOBPORT0	O	LVTTL	When HIGH, this output indicates that the input signal for port 0 is below the OOB threshold. When LOW, the input signal for port 0 is above the OOB threshold.
17	MODE0	I	LVTTL	This input is used to select the operating mode for the VSC7173 as described in Table 1 on page 4.
21	MODE1	I	LVTTL	This input is used to select the operating mode for the VSC7173 as described in Table 1 on page 4.
20	VDD		Power	3.3 V power supply for all circuits except the high-speed output buffers.
8, 16 32	VDD0, VDD1 VDD2		Power	3.3 V output buffer power supply for P0OUTP/N, P1OUTP/N, and P2OUTP/N, respectively.
25	Reserved			Reserved for future use. Leave unconnected.
5, 13, 22, 29 DAP	VSS		GND	Common ground. DAP is the exposed die attach pad on the bottom of the device.

PACKAGE INFORMATION

The VSC7173 device is available in a lead(Pb)-free package. VSC7173XYI is a 32-pin leadless quad flat pack (QFP-N) with an exposed pad.

Lead(Pb)-free products from Maxim comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 14. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC7173XYI	18.2	30.0	28.7	27.0

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

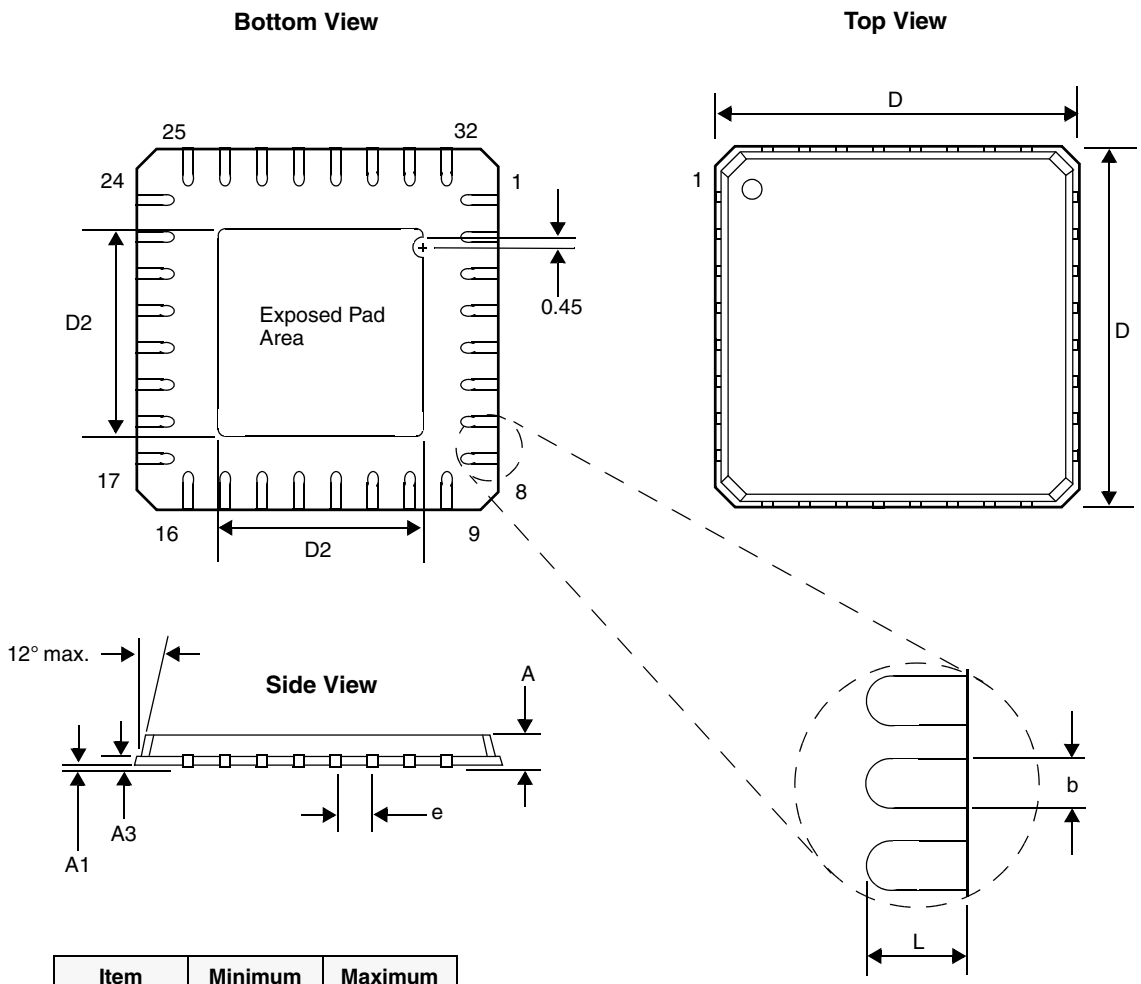
EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurement*

Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Package Drawing

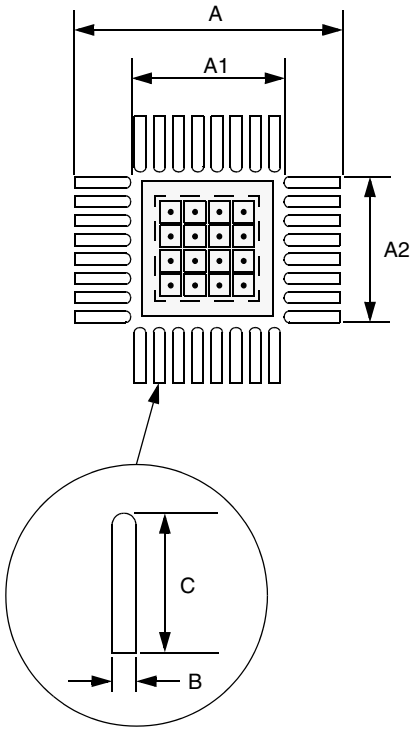


Item	Minimum	Maximum
A	0.85 nom.	0.90
A1	0	0.05
A3	0.20 REF	
b	0.23	0.35
D	7.00 BSC	
D2	4.95	5.25
e	0.65 BSC	
L	0.50	0.75

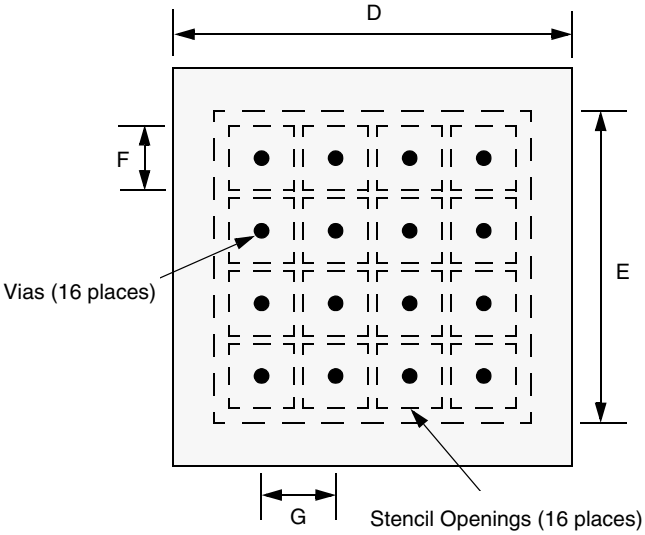
NOTES: *Drawing not to scale.*
All units in mm unless otherwise noted.
"b" is measured 0.20 to 0.25 from the terminal tip.

Figure 10. Package Drawing

Recommended Land Pattern



Land Pad Detail



Item	7 mm x 7 mm x 0.9 mm Exposed Pad QFP-N	Comments
A	7.445 maximum	
A1	5.325 minimum	
A2	4.92 maximum	
B	0.37 maximum	
C	1.06	
D	4.95 minimum 5.075 typical 5.20 maximum	Thermal land dimensions
E	5.10	Solder mask opening dimension
F	1.0	Stencil opening dimensions
G	1.2	Stencil opening and via spacing

NOTES: *All vias 0.30 to 0.33 diameter, plugged.*
Drawing not to scale.
All dimensions are in mm unless otherwise noted.

Figure 11. Recommended Land Pattern

ORDERING INFORMATION

The VSC7173 device is available in a lead(Pb)-free package. VSC7173XYI is 32-pin leadless quad flat pack (QFP-N) with an exposed pad.

Lead(Pb)-free products from Maxim comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Table 15. VSC7173 Ordering Information

Part Number	Description
VSC7173XYI	Lead(Pb)-free 32-pin QFP-N, 7 mm x 7 mm x 0.9 mm body

Maxim Integrated Products
120 San Gabriel Drive
Sunnyvale, CA 94086
United States

408-737-7600
www.maxim-ic.com