

# VSC7321

VITESSE

## VSC7321 Meigs-II™ - 10 x 1G and 10G Ethernet MAC Chip



### FEATURES:

- ▶ Ten Triple-Speed Ethernet MACs w/Support for RGMII/GMII/MII
- ▶ Integrated GbE SERDES for Direct Connection to Optical Modules
- ▶ Intelligent VLAN and MPLS Identification
- ▶ Loss less flow Control in Metro Applications up to 10km
- ▶ 10GbE MAC w/Integrated XAUI SERDES Interface Compliant to IEEE 802.3ae
- ▶ Low Pin Count, low Power OIF SPI-4.2 System Interface
- ▶ Extensive Loopback Capabilities for Both Line and System Side
- ▶ Configurable Parallel or Serial CPU Interface
- ▶ Dual MIIM Interface for Managing PHY Devices
- ▶ Independent Egress and Ingress Shaping/Policing
- ▶ Rate Limiting in 1 Mb/s Increments
- ▶ 802.3ad Compliant Link Aggregation and Trunking
- ▶ Statistical Support for RMON 1 (RFC2819), IEEE 802.3 Annex 30A, and SNMP (RFC 1213, 1573, and 1643)
- ▶ Supports Both Minimum Size 64B Frames as well as 9600B Jumbo Frames
- ▶ Automatic Generation of PAUSE Frames Based on Programmable Per Port FIFO Watermarks

### SPECIFICATIONS:

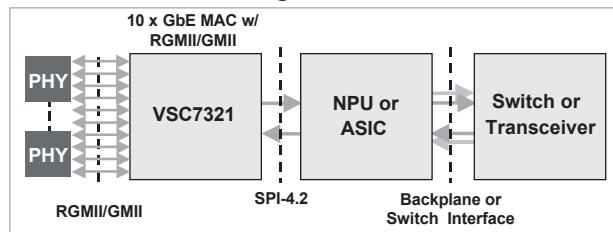
- ▶ Implemented in low Power 0.18 micron CMOS Technology, 2.5V/3.3V IO
- ▶ Industrial Temperature Range (-40°C to +85°C)
- ▶ Standard 5-Pin P1149.1 JTAG Test Port
- ▶ Packaged in a 728 pin TBGA

### APPLICATIONS:

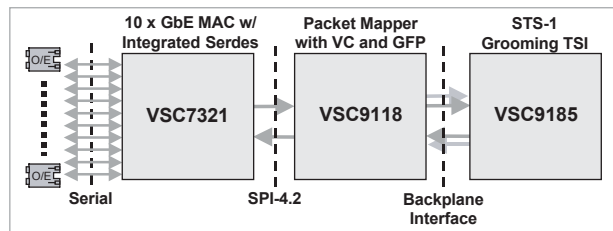
- ▶ Enterprise and Metro Ethernet Switches
- ▶ Multi-Service Provisioning Platforms
- ▶ Metro SONET/SDH Transport (ADMs)
- ▶ Edge and Core Aggregation Routers
- ▶ DWDM Transport Terminals (Wavelength Routers)

### APPLICATION DIAGRAMS:

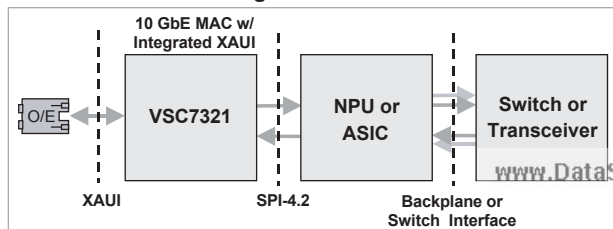
#### 10 x GbE MAC interfacing to NPU or ASIC



#### 10 x GbE over SONET/SDH using the VSC9118



#### 10 GbE MAC interfacing to NPU or ASIC



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## Lansing™ - 10 x 1 Gigabit Ethernet MAC Chip

### GENERAL DESCRIPTION:



Lansing™ is an advanced Ethernet MAC chip, allowing a system with a standard CSIX-64 host interface access to 10 tri-speed (10/100/1000 Mbit/s) Ethernet ports. The 10 separate tri-speed MACs support both half-duplex and full duplex at 10/100 Mbit/s and full duplex at 1 Gbit/s.

On-chip FIFOs capable of handling short-haul flow control are located between the Ethernet ports and the CSIX-64 interface. These FIFOs are also useful for smoothing bursty traffic on both the CSIX-64 and the Ethernet ports, and for compensating for the bursts generated when aggregating links.

Lansing™ can be used together with Meigs-I™ in a flexible port aggregation or port trunking mode. The scheme can be based on MAC addresses or MPLS tags.

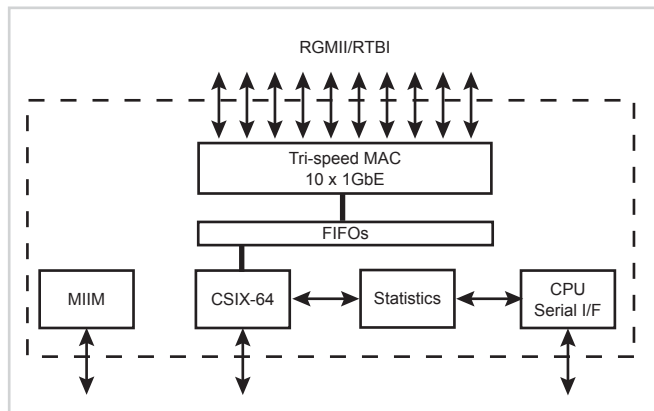
These features allow a 10GbE connection to behave like ten separate tri-speed connections, which make integration of 10GbE into existing designs simpler. Aggregation can be made between the 10GbE port and CSIX-64 or directly between the 10GbE port and the 10 tri-speed ports.

A dual MII Management interface sets up and controls the PHYs. Frames are monitored, and the statistics generated can be analyzed at a later time. All registers can be accessed via the serial or CSIX-64 interfaces.

A comprehensive set of statistics counters supports the RMON 1, IEEE802.3, and SNMP standards.

Test features include cyclic replay of frames at a user definable rate - either built by the external CPU directly inside the FIFOs or captures from incoming traffic.

### VSC7322 BLOCK DIAGRAM:



For more information on Vitesse Products visit the Vitesse web site at [www.vitesse.com](http://www.vitesse.com) or contact Vitesse Sales at (800) VITESSE or [sales@vitesse.com](mailto:sales@vitesse.com)