ETHERNET PRODUCT

VSC7322

VITESSE

Lansing™ - 10 x 1 Gigabit Ethernet MAC Chip

SPECIFICATIONS:

- 25 MHz Reference Clock
- 1.5 V CSIX-64 Power Supply
- 1.8 V Core Power Supply
- 2.5 V RGMII/RTBI Interface Power Supply
- 3.3 V CPU Power Supply
- 680-Pin, 40 x 40 mm TSBGA Package

FEATURES:

- Ten 10/100/1000 Mbit/s RGMII/RTBI interfaces
- CSIX-64 AC Class2 host interface
- Full bandwidth, non-blocking performance on the receive and the transmit
- Internal short-haul flow control memory
- 1024 kbit ingress and egress FIFOs
- Advanced link aggregation/trunking based on SMAC/DMAC and MPLS label in conjunction with Meigs-I™
- Aggregation/Port trunking between 10G and tri-speed ports in conjunction with Meigs-I™
- Intelligent VLAN and MPLS tagging/ untagging feature
- Serial CPU interface for register access
- Full RMON 1, IEEE802.3, and SNMP statistics
- ASIC/FPGA friendly CSIX-64 Interface
- Jumbo frame support
- Advanced test features including internal loop-back, frame collection, and replay

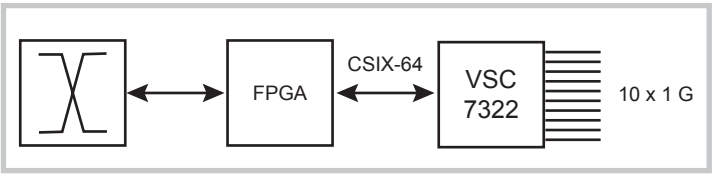
APPLICATIONS:

- 10 port Gigabit Ethernet MAC
- Link aggregation/Port trunking in conjunction with Meigs-I™

FUTURE-PROOF TECHNOLOGY:

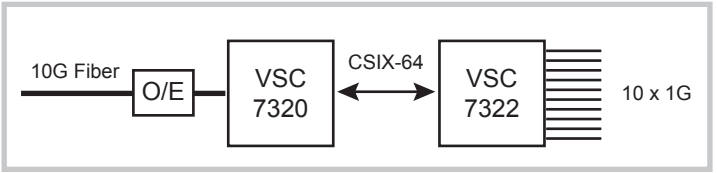
- VSC7322 is part of a product roadmap that includes advanced 10 Gigabit Ethernet technology. As such, the architecture of VSC7322 is designed to take advantage of emerging and future technologies – effectively allowing manufacturers to future-proof switch applications.

GIGABIT LINE CARD APPLICATION:



Application using the VSC7322 and a customer specific FPGA to create a gigabit switching line card

10GbE TO GIGABIT ETHERNET AGGREGATION:



Chipset application using the VSC7320 and VSC7322 back-to-back to aggregate 10 x 1G into 10G Ethernet

VSC7322

Lansing™ - 10 x 1 Gigabit Ethernet MAC Chip

GENERAL DESCRIPTION:

Lansing™ is an advanced Ethernet MAC chip, allowing a system with a standard CSIX-64 host interface access to 10 tri-speed (10/100/1000 Mbit/s) Ethernet ports. The 10 separate tri-speed MACs support both half-duplex and full duplex at 10/100 Mbit/s and full duplex at 1 Gbit/s.

On-chip FIFOs capable of handling short-haul flow control are located between the Ethernet ports and the CSIX-64 interface. These FIFOs are also useful for smoothing bursty traffic on both the CSIX-64 and the Ethernet ports, and for compensating for the bursts generated when aggregating links.

Lansing™ can be used together with Meigs-I™ in a flexible port aggregation or port trunking mode. The scheme can be based on MAC addresses or MPLS tags.

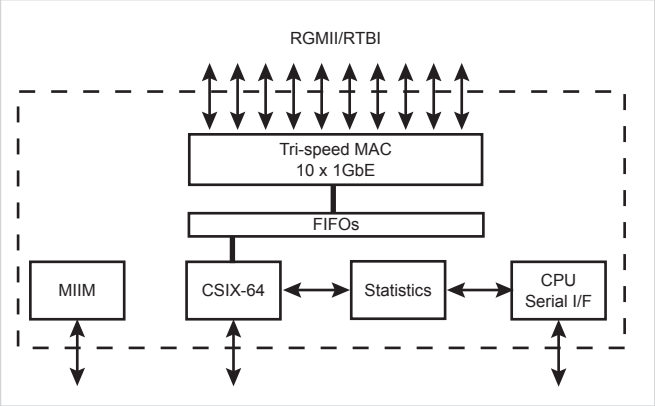
These features allow a 10GbE connection to behave like ten separate tri-speed connections, which make integration of 10GbE into existing designs simpler. Aggregation can be made between the 10GbE port and CSIX-64 or directly between the 10GbE port and the 10 tri-speed ports.

A dual MII Management interface sets up and controls the PHYs. Frames are monitored, and the statistics generated can be analyzed at a later time. All registers can be accessed via the serial or CPU Interface.

A comprehensive set of statistics counters supports the RMON 1, IEEE802.3, and SNMP standards.

Test features include cyclic replay of frames at a user definable rate - either built by the external CPU directly inside the FIFOs or captures from incoming traffic.

VSC7322 BLOCK DIAGRAM:



For more information on Vitesse Products visit the Vitesse web site at www.vitesse.com or contact Vitesse Sales at (800) VITESSE or sales@vitesse.com

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