

Preliminary Data Sheet

VSC7924

SONET/SDH 2.5Gb/s Laser Diode Driver

Features

- Rise Times Less Than 100ps
- High-Speed Operation (Up to 2.5Gb/s NRZ Data)
- Single-Ended Operation
- Single Power Supply
- Direct Access to Modulation and Bias FETs
- Data Density Monitors
- 24-Pin Ceramic Package

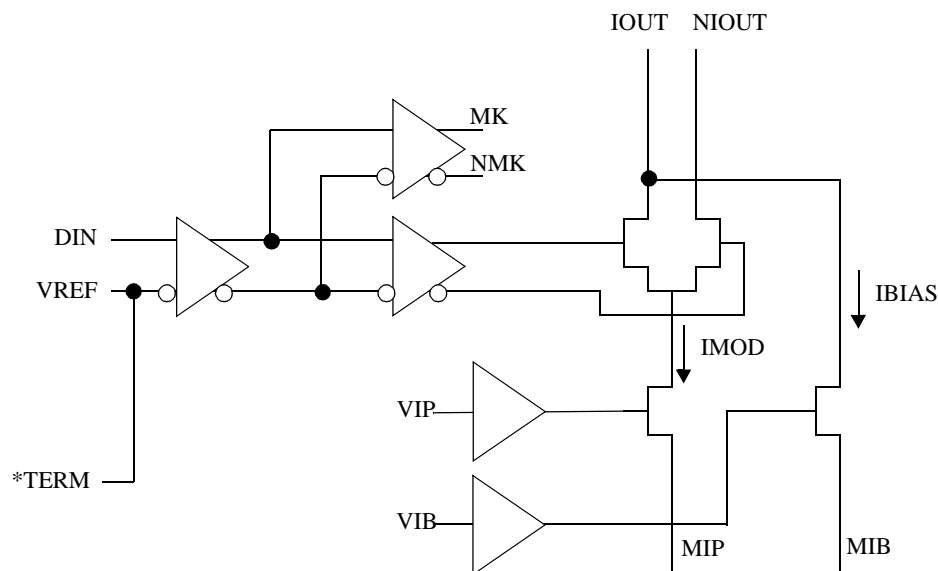
Applications

- SONET/SDH at 622Mb/s, 1.244Gb/s, and 2.488Gb/s
- Full-Speed Fibre Channel (1.062Gb/s)

General Description

The VSC7924 is a single 5V supply, 2.5Gb/s laser diode driver with direct access to the laser modulation and bias FETs. Laser bias and modulation currents are set by external components allowing precision monitoring and setting of the current levels. Data inputs accept ECL levels. Data density outputs are provided to allow the user to adjust the laser bias in high unbalanced data applications.

VSC7924 Block Diagram



*Terminated to Off-chip Capacitor

Table 1: Signal Pin Reference

Signal	Type	Level	# Pins	Description
DIN	In	ECL	1	Data Input
MK, NMK	Out	ECL	2	Data Density Differential Outputs
NIOUT	Out		1	Laser Modulation Current Output (Complementary)
IOUT	Out		1	Laser Modulation Current Output (To Laser Cathode))
VSS	Pwr	Pwr	5	Negative Voltage Rail
GND	Pwr	Pwr	8	Positive Voltage Rail
VIP	In	DC	1	Modulation Gate Node
MIP	In	DC	1	Modulation Source Node
VIB	In	DC	1	Bias Gate Node
MIB	In	DC	1	Bias Source Node
VREF	In	DC	1	Data Input Reference
TERM	In	DC	1	Data Input Reference
Total Pins			24	

Table 2: Absolute Maximum Ratings

Symbol	Rating	Limit
V _{SS}	Negative Power Supply Voltage	V _{CC} to -6.0V
T _J	Maximum Junction Temperature	-55°C to +125°C
T _{STG}	Storage Temperature	-65°C to +150°C

Table 3: ECL Input and Outputs

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V _{IN}	Input Voltage Swing	300		800	mV	Peak-to-peak, V _{REF} = -1.3V
V _{OH}	ECL Output High Voltage	-1200		-700	mV	50Ω to -2.0V
V _{OL}	ECL Output Low Voltage	-2000		-1600	mV	50Ω to -2.0V

Table 4: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
GND	Positive Voltage Rail		0		V	
VSS	Negative Voltage Rail	-5.5	-5.2	-4.9	V	
T _{Cl}	Operational Temperature ⁽¹⁾	-40		85 ⁽²⁾	°C	Power dissipation = 1.25W
T _J	Junction Temperature			125	°C	

NOTES: (1) Lower limit of specification is ambient temperature and upper limit is case temperature.

(2) See "Calculation of the Maximum Case Temperature" section for detailed maximum temperature calculations.

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Table 5: Power Dissipation

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
I_{VSS}	Power Supply Current (V_{SS})			220	mA	$V_{SS} = -5.5V, I_{MOD} = I_{BIAS} = 0mA$
P_D	Total Power Dissipation			1120	mW	$V_{SS} = -5.5V, I_{MOD} = I_{BIAS} = 0mA,$ $R_{LOAD} = 25\Omega$ to GND
P_{DMAX}	Maximum Power Dissipation			1815	mW	$V_{SS} = -5.5V, I_{MOD} = 60mA,$ $I_{BIAS} = 50mA, I_{OUT} = 0V$

Table 6: Laser Driver DC Electrical Specifications

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
I_{BIAS}	Programmable Laser Bias Current	2		50	mA	
I_{MOD}	Programmable Modulation Current	2		60	mA	
V_{IB}	Laser Bias Control Voltage			$V_{SS} + 2.1$	V	$I_{BIAS} = 50mA$
V_{IP}	Laser Modulation Control Voltage			$V_{SS} + 2.1$	V	$I_{MOD} = 60mA$
V_{OCM}	Output Voltage Compliance	GND -2.2V			V	$V_{SS} = -5.2V$

Table 7: Laser Driver AC Electrical Specifications

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
t_R, t_F	Output Rise and Fall Times			100	ps	25 Ω load, 20%-80%, 15mA < I_{MOD} < 60mA, $I_{BIAS} = 20mA$

Table 8: Package Thermal Specifications

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
θ_{JCC}	Thermal Resistance from junction-to-case		25		$^{\circ}C/W$	Ceramic Package

Calculation of the Maximum Case Temperature

The VSC7924 is designed to operate with a maximum junction temperature of 125°C. The rise from the case to junction is determined by the power dissipation of the device. The power dissipation is determined by the V_{SS} current plus the operating I_{MOD} and I_{BIAS} currents.

The power of the chip is determined by the following formula:

$$P_D = (-V_{SS} * I_{SS}) + ((V_{IOUT} - V_{SS}) * I_{MOD}) + ((V_{BIAS} - V_{SS}) * I_{BIAS})$$

For example with:

$$\begin{aligned} V_{SS} &= -5.2V \\ I_{MOD} &= 40mA \\ I_{BIAS} &= 20mA \\ V_{BIAS} &= -2.0V \\ V_{IOUT} &= -2.0V \end{aligned}$$

$$P_D = (-5.2 * 220mA) + ((5.2 - 2.0) * 40mA) + ((5.2 - 2.0) * 20mA)$$

$$P_D = 1144mW + 128mW + 64mW = 1.336W$$

The thermal rise from junction to case is $\theta_{JC} * P_D$. For the ceramic package, $\theta_{JC} = 25^\circ\text{C}/\text{W}$. Thus the thermal rise is:

$$25^\circ\text{C}/\text{W} * 1.336W = 33.4^\circ\text{C}$$

The maximum case temperature is:

$$125^\circ\text{C} - 33.4^\circ\text{C} = 91.6^\circ\text{C}$$

The absolute maximum power dissipation of the device is at:

$$\begin{aligned} V_{SS} &= -5.5V \\ I_{MOD} &= 60mA \\ I_{BIAS} &= 50mA \\ V_{BIAS} &= 0V \\ V_{IOUT} &= 0V \end{aligned}$$

$$P_D = (5.5 * 220mA) + (5.5 * 60mA) + (5.5mA * 50mA) \quad P_D = 1.815W$$

This will net a maximum junction to case thermal rise of: $1.815W * 25^\circ\text{C}/\text{W} = 45.4^\circ\text{C}$

This situation will allow maximum case temperature of: $125^\circ\text{C} - 45.4^\circ\text{C} = 79.6^\circ\text{C}$

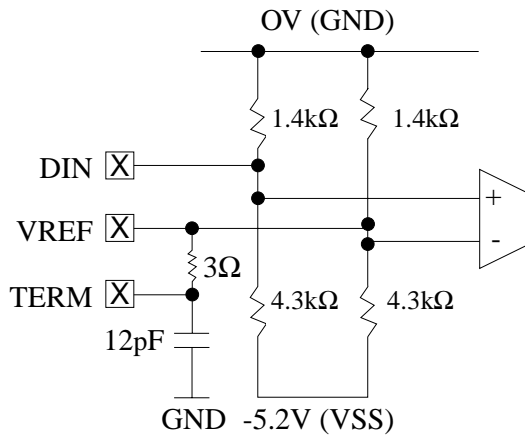
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Input Termination Schemes

Figure 1: Input Structure



Nominal $V_{REF} = 1.3V$
 1.4kΩ, 4.3kΩ resistor on die, nominal values

Figure 2: Single-Ended AC Coupled

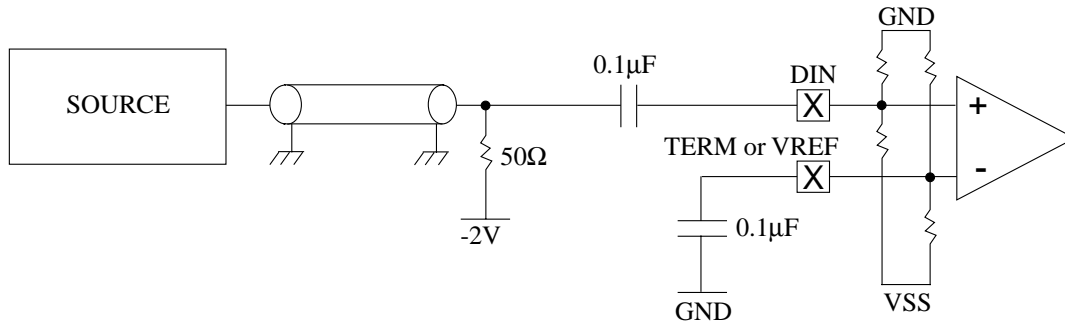


Figure 3: Single Ended AC Coupled with Offset Adjust

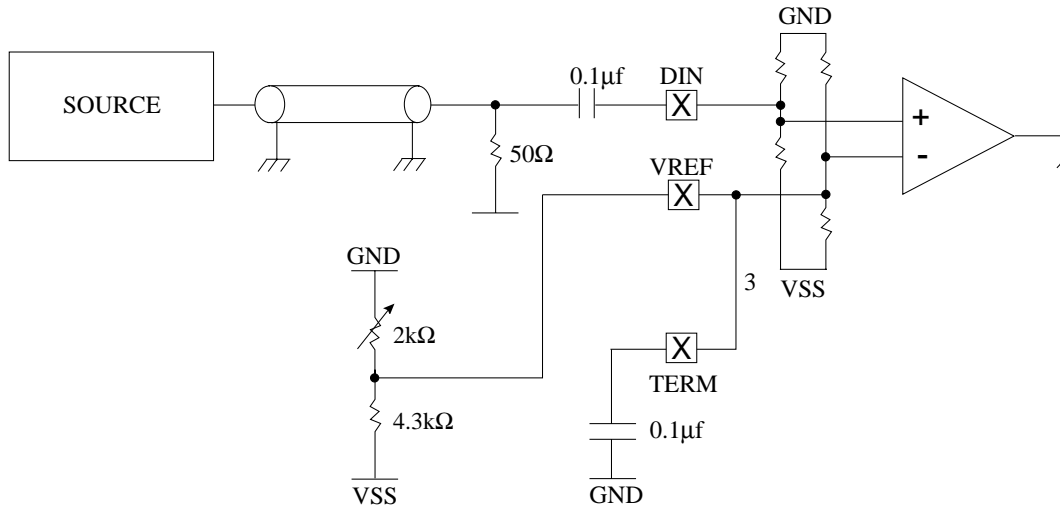
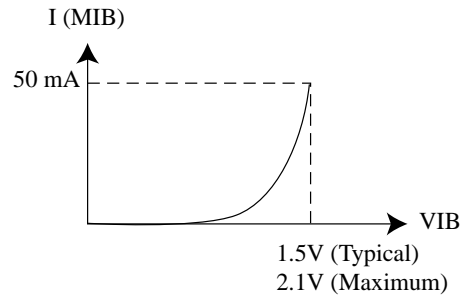
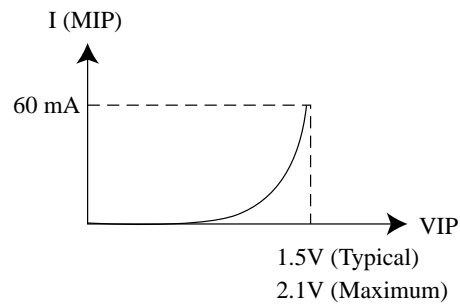


Figure 4: Control Signals VIP and VIB

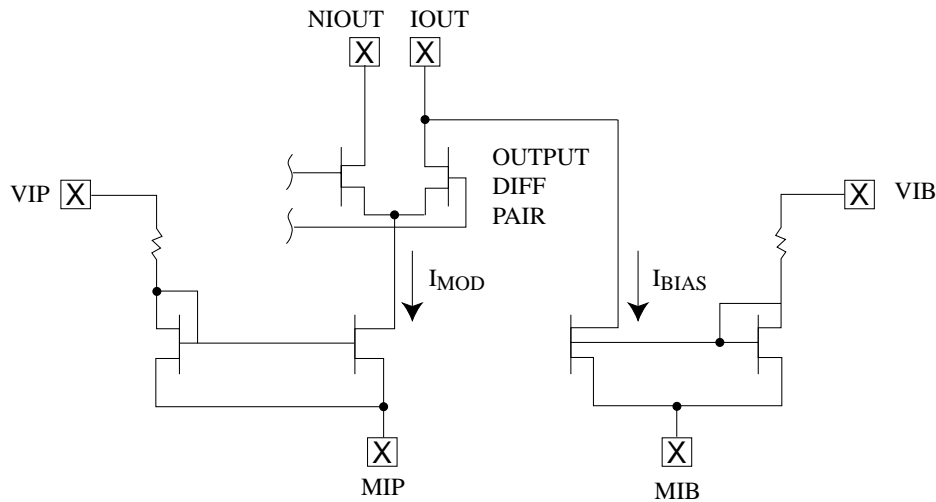


Typical Bias Current v.s. Bias Voltage



Typical Modulation Current v.s. Modulation Voltage

Figure 5: Simplified Output Structure

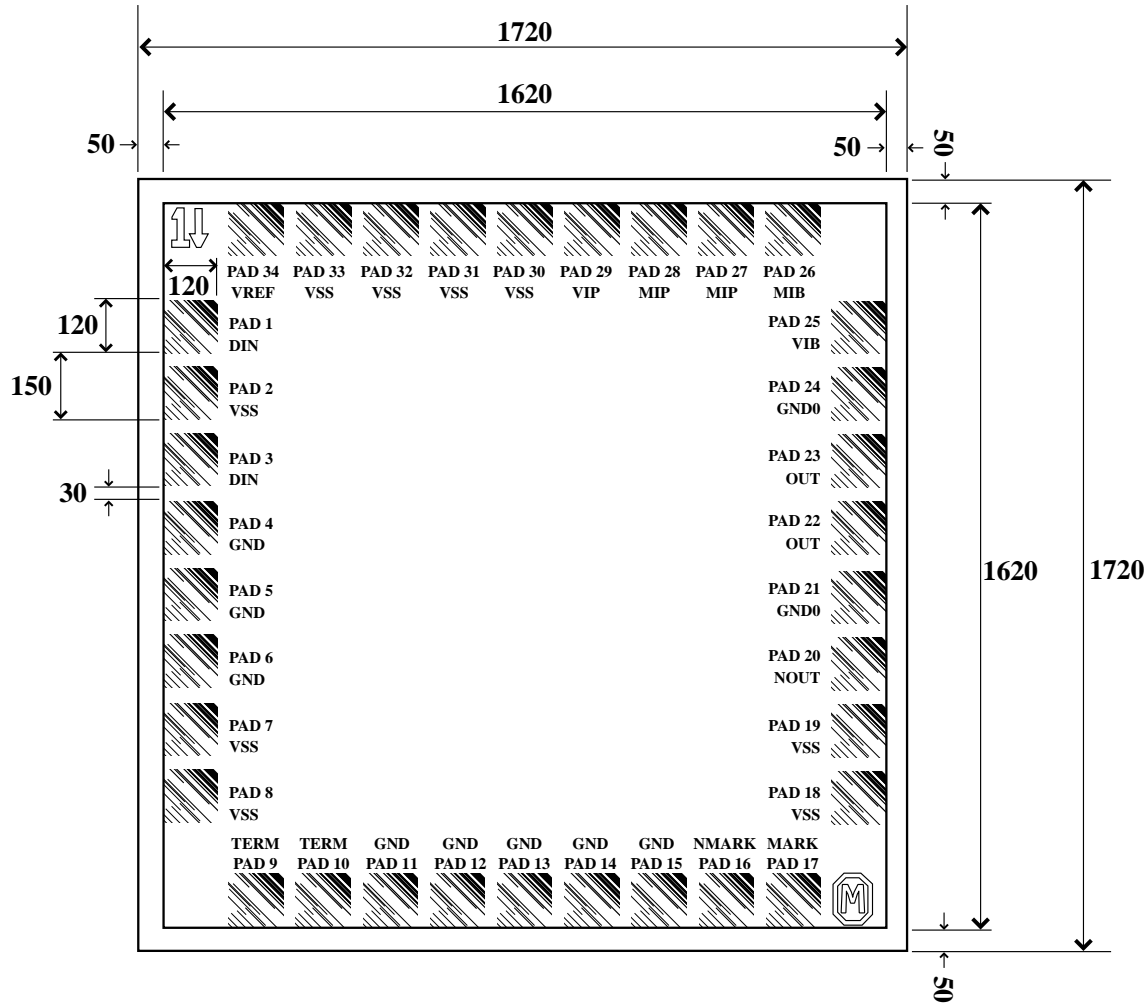


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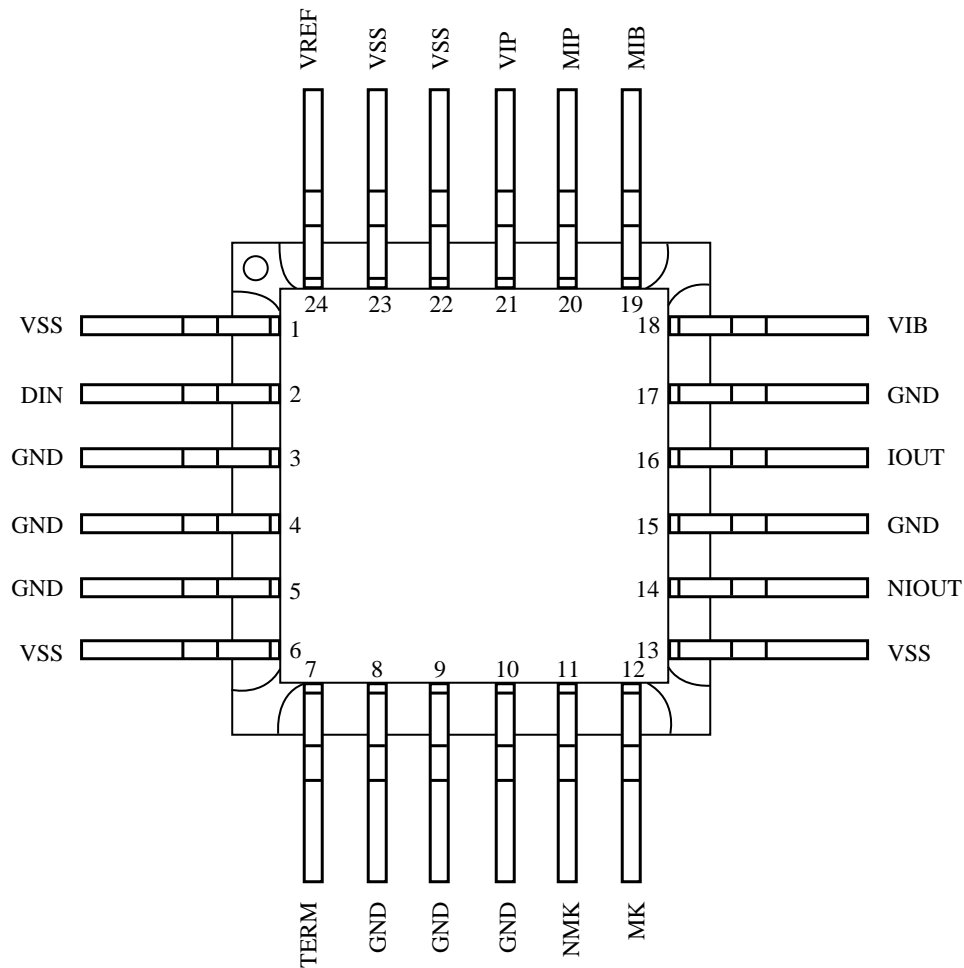
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Figure 6: Pad Assignments for VSC7924 Die



- 1) Die size = $1620\mu\text{m} \times 1620\mu\text{m}$
- 2) Actual die size = $1720\mu\text{m} \times 1720\mu\text{m}$ (after the die are cut up)
- 3) Pad size = $120\mu\text{m} \times 120\mu\text{m}$
- 4) Pad pitch = $150\mu\text{m}$
- 5) Space between pads = $30\mu\text{m}$

Pin Diagram for 24-Pin Ceramic Package



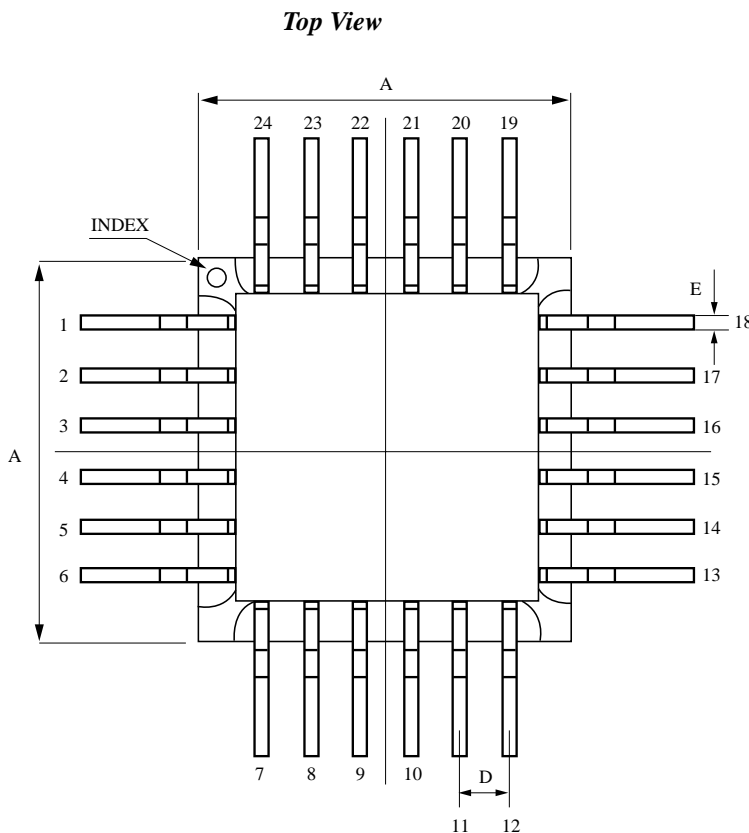
Note: Package bottom plate is connected to GND within the package.
Package lid is electrically unconnected.

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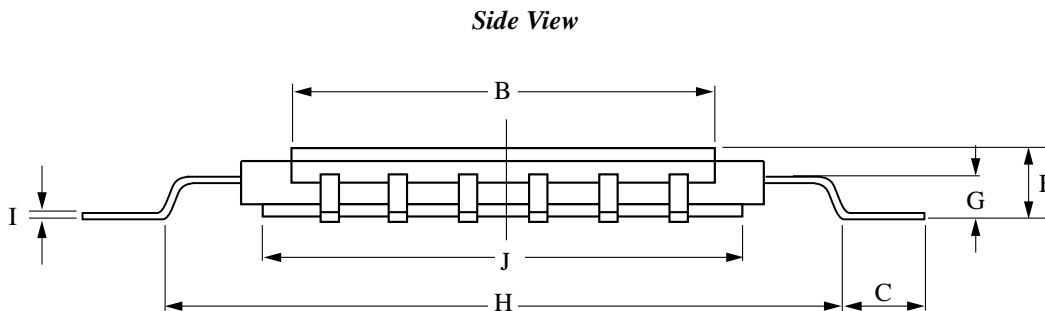
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Package Information - 24 Pin Ceramic Package (Formed Leads)

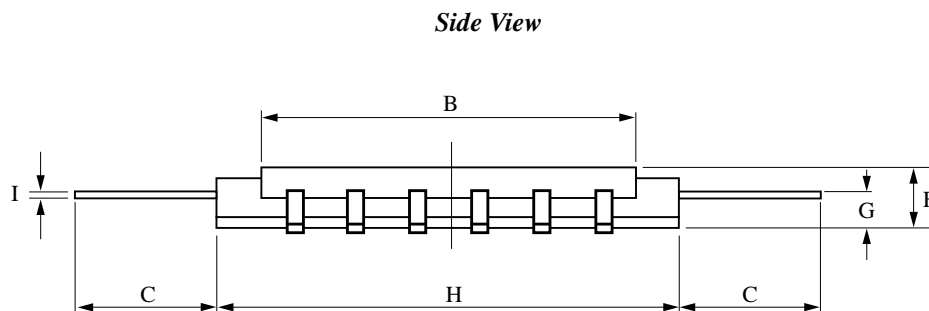
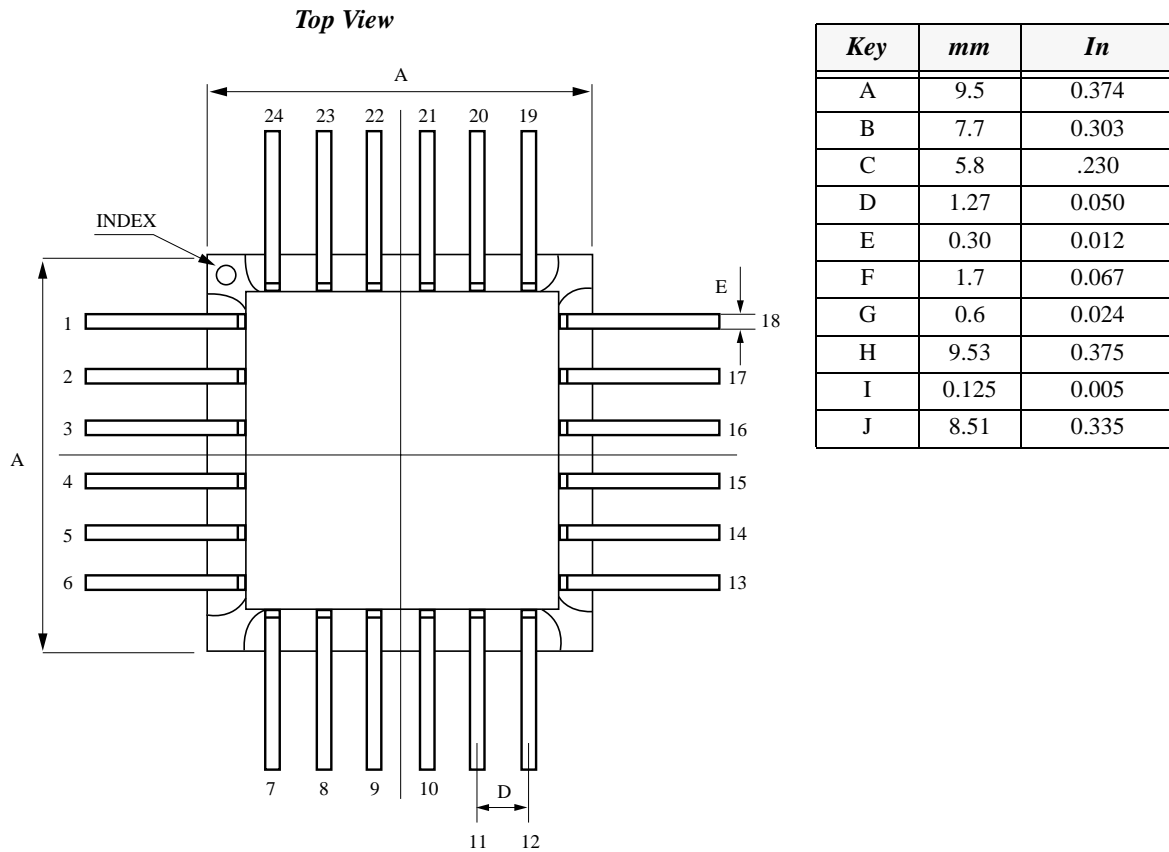


Key	mm	In
A	9.5	0.374
B	7.7	0.303
C	2.0	0.079
D	1.27	0.050
E	0.30	0.012
F	1.7	0.067
G	0.6	0.024
H	11.5	0.453
I	0.125	0.005
J	8.51	0.335



NOTES: Drawing not to scale.
 Package #: 101-312-0 Issue #:1
 L id #: 101-303-1 Issue #:1

Package Information - 24 Pin Ceramic Package (Straight Leads)



NOTES: Drawing not to scale.
Package #: 101-000-0 Issue #:1

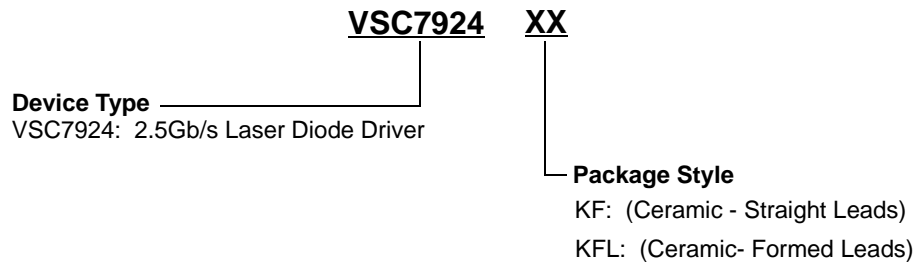
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Ordering Information

The order number for this product is formed by a combination of the device number, and package style.



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