VITESSE

VSC8115
Datasheet

STS-12/STS-3 Multirate Clock and Data Recovery Unit

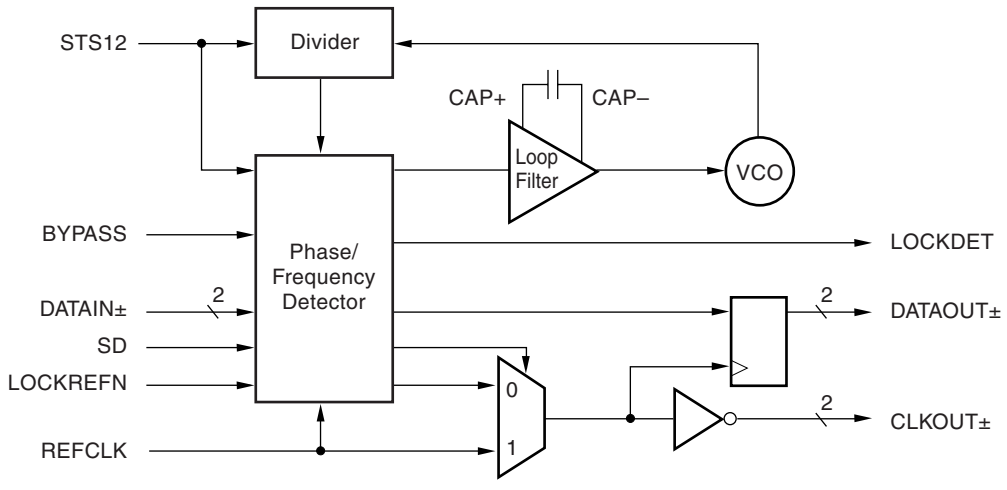
FEATURES

- Performs clock and data recovery for 622.08 Mbps (STS-12/OC-12/STM-4) or 155.52 Mbps (STS-3/OC-3/STM-1) NRZ data
- 19.44 MHz reference frequency LVTTL input
- Lock Detect output pin monitors data run length and frequency drift from reference clock
- Data is retimed at the output
- Active HIGH Signal Detect LVPECL input
- Low jitter, high-speed outputs support LVPECL and low-power LVDS
- Low power: 188 mW typical
- 3.3 V power supply
- 20-pin TSSOP package
- Requires one external capacitor
- PLL bypass operation facilitates board debug process

GENERAL DESCRIPTION

The VSC8115 functions as a clock and data recovery (CDR) unit for SONET/SDH-based equipment to derive high-speed timing signals. The VSC8115 recovers the clock from the scrambled non-return to zero (NRZ) data operating at 622.08 Mbps (STS-12/OC-12/STM-4) or 155.52 Mbps (STS-3/OC-3/STM-1). After the clock is recovered, the data is retimed using an output flip-flop. Both recovered clock and retimed data outputs support LVDS and LVPECL signals to facilitate a low-jitter and low-power interface.

VSC8115 Block Diagram



FUNCTIONAL DESCRIPTION

The VSC8115 contains an on-chip phase locked-loop (PLL) consisting of a phase/frequency detector (PFD), a loop filter using one external capacitor, an LC-based voltage-controlled oscillator (VCO), and a programmable frequency divider. The PFD compares the phase relationship between the VCO output and an external 19.44 MHz LVTTL reference clock to make coarse adjustments to the VCO block so that its output is held within ±500 ppm of the reference clock. The PFD also compares the phase relationship between the VCO output and the serial data input to make fine adjustments to the VCO block. The loop filter converts the phase detector output into a smooth DC voltage. This DC voltage is used as the input to the VCO block whose output frequency is a function of the input voltage. The VCO output signal is fed into a programmable frequency divider that generates either a 622.08 Mbps signal if STS12 is HIGH, or a 155.52 Mbps signal if STS12 is LOW, back to the PFD.

Lock Detection

The VSC8115 features a lock detection for the PLL. The lock detect (LOCKDET) output goes HIGH to indicate that the PLL is locked to the serial data inputs and that valid data and clock are present at the high-speed differential outputs. If LOCKDET output is LOW, then either the PLL is forced to lock to the REFCLK input or the VCO has drifted away from the local reference clock by more than 500 ppm.

LOCKDET requires that the reference clock be present to operate properly.

Signal Detection

The VSC8115 has a signal detect (SD) input and a lock-to-reference (LOCKREFN) input. The SD pin is a LVPECL input and the LOCKREFN pin is a LVTTL input. These two control pins are used to indicate an LOS condition and are connected inside the part as shown in Figure 1 on page 3. If either one of these two inputs goes LOW and BYPASS is LOW, the VSC8115 will enter a Loss of Signal (LOS) state, and will hold the DATAOUT± output at logic LOW state. During the LOS state, the VSC8115 will also hold the output clock CLKOUT± to within ±500 ppm of the REFCLK. See Table 1 on page 3.

Most optical modules have an SD output. This SD output indicates that there is sufficient optical power and is typically active HIGH. If the SD output on the optical module is LVPECL, it should be connected directly to the SD input on the VSC8115, and the LOCKREFN input be tied HIGH. If the SD output is LVTTL, it should be connected directly to the LOCKREFN input, and the SD input should be tied HIGH.

The SD and LOCKREFN inputs also can be used for other applications when it is required to hold the CLKOUT± output to within ±500 ppm of the reference clock and to force the DATAOUT± output to the logic LOW state.

Reference Clock

Upon powering up the VSC8115, it is recommended that the reference clock be present at least 40 bit times before the data signal is introduced.

PLL Bypass Operation

The BYPASS pin is intended for use in production test and should be set at logic LOW in normal operation. If both BYPASS and STS12 pins are set at logic HIGH, the VSC8115 will bypass the PLL and present an inverted version of the REFCLK to the clock output CLKOUT±. The REFCLK's rising edge is used to capture data at DATAIN± and transmit data at DATAOUT±. This bypass operation can be used to facilitate the board debugging process.

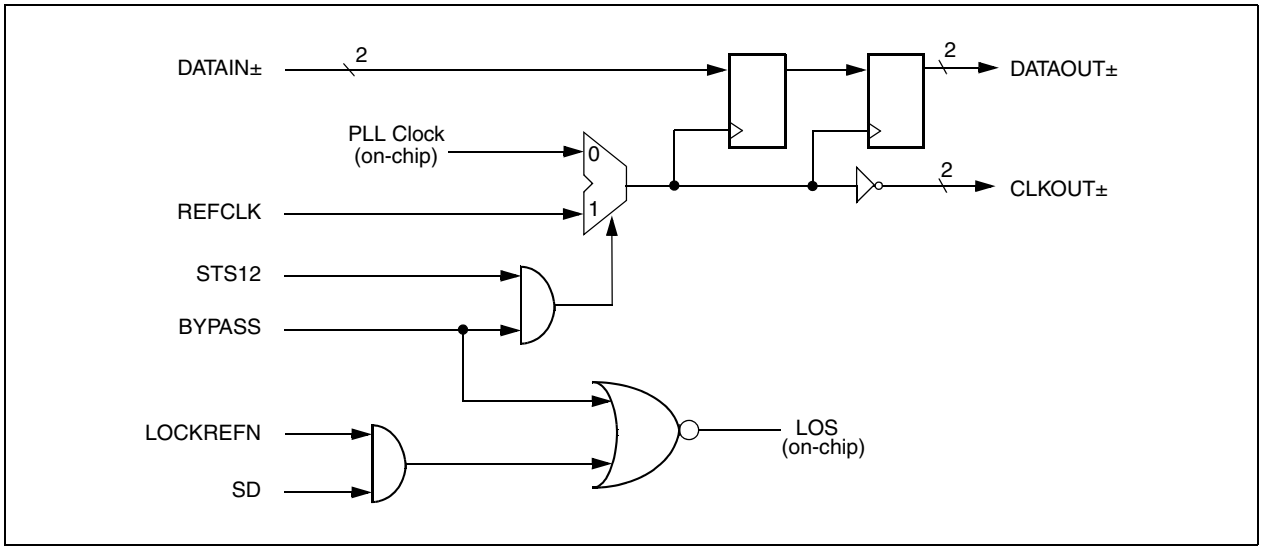


Figure 1. Control Diagram for Signal Detection and PLL Bypass Operation

Table 1. Signal Detect and PLL Bypass Operation Control

STS12	BYPASS	LOCKREFN	SD	DATAOUT	CLKOUT
1	0	1	1	DATAIN	PLL clock
1	0	1	0	LOW	PLL clock
1	0	0	1	LOW	PLL clock
1	0	0	0	LOW	PLL clock
1	1	X	X	DATAIN	REFCLK
0	0	1	1	DATAIN	PLL clock
0	0	1	0	LOW	PLL clock
0	0	0	1	LOW	PLL clock
0	0	0	0	LOW	PLL clock
0	1	X	X	Not allowed	Not allowed

ELECTRICAL SPECIFICATIONS

DC Characteristics

Guaranteed over recommended operating conditions listed in Table 8 on page 5.

Table 2. LVPECL Single-Ended Inputs and Outputs

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IH}	Input HIGH voltage	V_{DD} – 1.125	V_{DD} – 0.5	V	Guaranteed input HIGH voltage
V_{IL}	Input LOW voltage	V_{DD} – 2.0	V_{DD} – 1.5	V	Guaranteed input LOW voltage
I_{IH}	Input HIGH current	–0.5	10	µA	$V_{IN} = V_{DD} – 0.5$ V
I_{IL}	Input LOW current	–0.5	10	µA	$V_{IN} = V_{DD} – 2.0$ V
V_{OL}	Output LOW voltage	V_{DD} – 2.0	V_{DD} – 1.8	V	50Ω to (V_{DD} – 2.0 V)
V_{OH}	Output HIGH voltage	V_{DD} – 1.25	V_{DD} – 0.67	V	50Ω to (V_{DD} – 2.0 V)

Table 3. LVPECL Differential Inputs

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IH}	Input HIGH voltage	V_{DD} – 1.75	V_{DD} – 0.4	V	Guaranteed input HIGH voltage
V_{IL}	Input LOW voltage	V_{DD} – 2.0	V_{DD} – 0.7	V	Guaranteed input LOW voltage
ΔV_{IN}	Differential input voltage	250		mV	
I_{IH}	Input HIGH current	–0.5	10	µA	$\Delta V_{IN} = 0.5$ V
I_{IL}	Input LOW current	–0.5	10	µA	$\Delta V_{IN} = 0.5$ V

Table 4. LVDS Differential Outputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{OCM}	Output common-mode voltage	1.0	1.35	1.7	V	
ΔV_{OUT}	Differential output swing	700		1700	mV	

Table 5. LVPECL Differential Outputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{OCM}	Output Common-Mode Voltage	0.8	1.35	1.7	V	50 Ω to (V_{DD} – 2.0 V)
ΔV_{OUT}	Differential Output Swing	800		1700	mV	50 Ω to (V_{DD} – 2.0 V)

Table 6. LVTTL Inputs

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IH}	Input HIGH voltage	2.0	V_{DD}	V	
V_{IL}	Input LOW voltage	0	0.8	V	
I_{IH}	Input HIGH current	–50	50	µA	V_{IN} = 2.75 V, V_{DD} = maximum
I_{IL}	Input LOW current	–50	50	µA	V_{IN} = 0.5 V, V_{DD} = maximum

Table 7. Power Supply Requirements

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
I_{DD}	Power supply current from V_{DD}		57	80	mA	Outputs unterminated
P_D	Power dissipation		188.1	277	mW	Outputs unterminated

Operating Conditions

Table 8. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Power supply voltage	3.135	3.3	3.465	V
T	Operating temperature under bias[1]				
	VSC8115, VSC8115-T	0		70	°C
	VSC8115-02	–40		85	°C
	VSC8115-03	–20		85	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

Maximum Ratings

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Power supply voltage, referenced to GND	–0.5	4.0	V
	DC input voltage (LVPECL, LVTTL)	–0.5	V_{DD} + 0.5	V
	Output current (LVDS or LVPECL)	+50	–50	
T_S	Storage temperature	–65	150	°C
V_{ESD}	Electrostatic discharge voltage, human body model	–750	750	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

AC Characteristics

Guaranteed over recommended operating conditions listed in Table 8 on page 5.

Table 10. Performance Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
f	VCO center frequency		622.08		MHz	
f_{TOL}	CRU's reference clock frequency tolerance	–250		250	ppm	
fT_{REF_CLK}	OC-12/STS-12 capture range		±500		ppm	With respect to the fixed reference frequency.
$CLKOUT_{DC}$	Clock output duty cycle	45		55	% of UI	20% minimum transition density.
t_{LOCK}	OC-12/STS-12 acquistion lock time			16	µs	Valid REFCLK and device already powered up.
$t_{LOCKDET\_R}$, $t_{LOCKDET\_F}$	LVDS and LVPECL output rise time and fall time			500	ps	10% to 90%, with 100 Ω and 5 pF capacitive equivalent load.
J_{GEN_CLK}	CLKOUT± jitter generation		0.005	0.01	UI_{rms}	
J_{TOL}	OC-12/STS-12 jitter tolerance	0.45			UI	Sinusoidal input jitter of DATAIN± from 250 kHz to 5 MHz.

Jitter Tolerance

Jitter tolerance is the ability of the CDR to track timing variations in the received data stream. The Telecordia and ITU specifications allow the received optical data to contain jitter; however, the amount that must be tolerated is a function of the frequency of the jitter. At high frequencies, the specifications do not require the VSC8115 to tolerate large amounts of jitter, whereas, at low frequencies, many unit intervals (bit times) of jitter have to be tolerated. The VSC8115 tolerates this jitter with margin over the specification limits. See Figure 2. The VSC8115 obtains and maintains lock based on the data transition information. When there is no transition on the data stream, the recovered clock frequency is held to within ±500 ppm of the reference clock. The VSC8115 maintains lock status with a data stream carrying over 1,000 consecutive identical digits (CID).

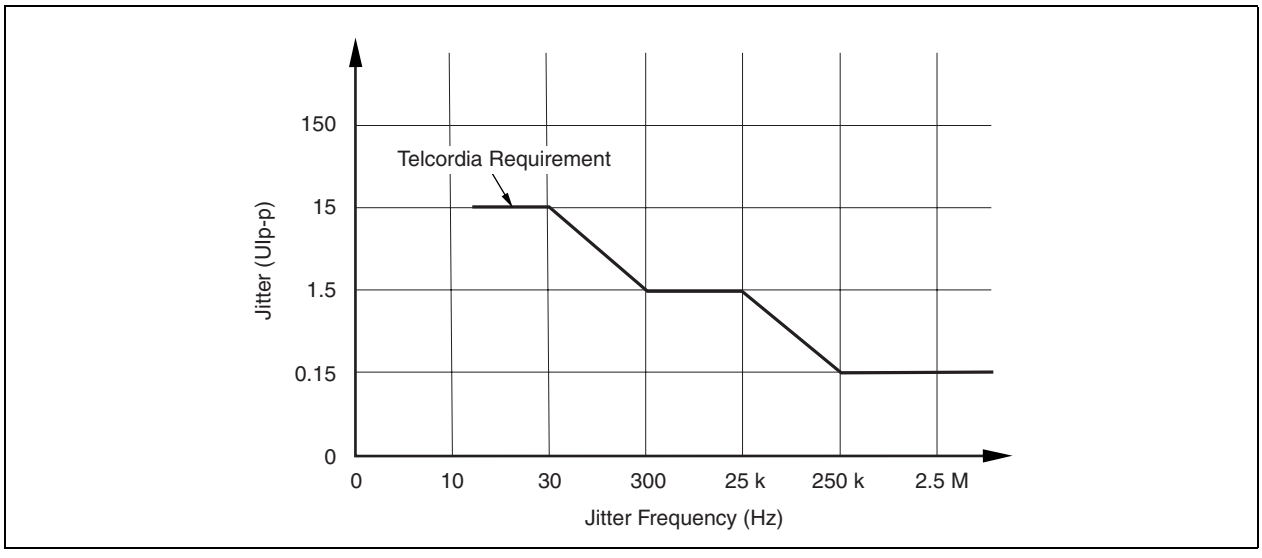


Figure 2. Input Jitter Tolerance Specification

Jitter Generation

Maximum jitter generation is 0.01 UI within the SONET/SDH band when rms jitter of less than 14 ps (OC-12) or 56 ps (OC-3) is presented to the serial data inputs.

Retimed Data and Clock Outputs

It is recommended that the retimed data output be captured with the rising edge of the clock output as shown in Figure 3. Data valid time is longer for OC-3/STS-3 mode of operation than that of OC-12/STS-12. Data valid time before the output clock's rising edge is the available setup time (t_{SU}), while the data valid time after the clock's rising edge is the available hold time (t_H).

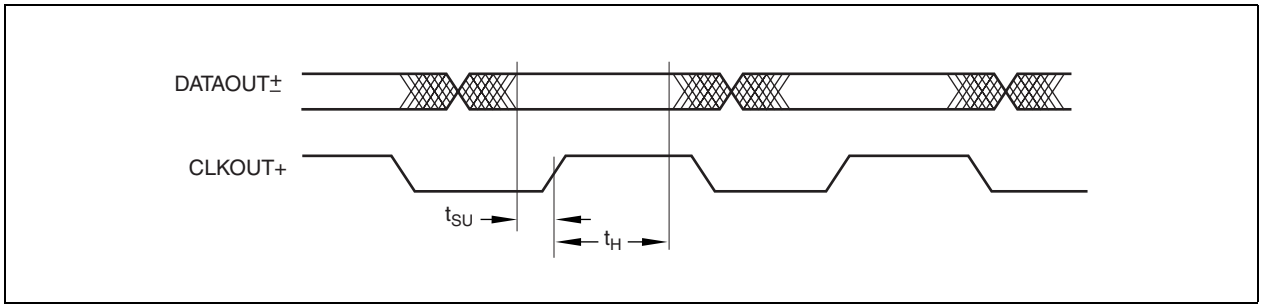


Figure 3. Retimed Data and Clock Outputs Timing Diagram

Table 11. Retimed Data and Clock Outputs Timing

Symbol	Parameter	Minimum	Maximum	Unit	Condition
t_{SU}	Available setup time	450 2.0		ps ns	STS-12 operation (622.08 MHz) STS-3 operation (155.52 MHz)
t_H	Available hold time	650 3.0		ps ns	STS-12 operation (622.08 MHz) STS-3 operation (155.52 MHz)

High-Speed Outputs

The high-speed output buffers, DATAOUT± and CLKOUT±, can be terminated as either LVDS or LVPECL outputs. If used as LVDS outputs, the transmission lines should be routed with 100 Ω differential impedance and terminated at the receive end with a 100Ω resistor across the differential pair. If used as LVPECL outputs, the transmission line should be 50 Ω terminated, with 50 Ω pull-down resistors near the receiving end. See Figure 4 and Figure 5.

Figure 4. High-Speed Outputs, LVDS Termination

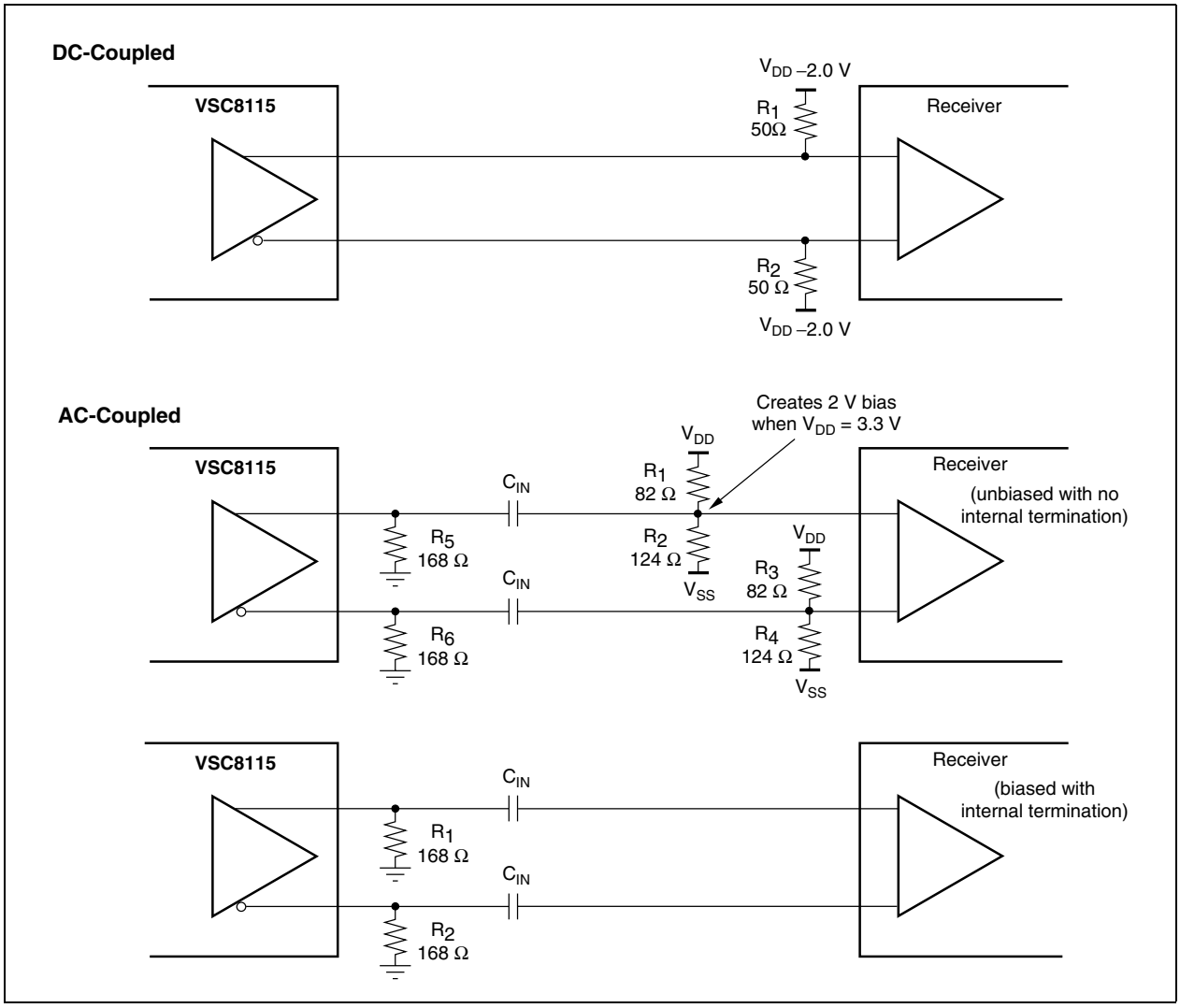


Figure 5. High-Speed Outputs, LVPECL Terminations

PACKAGE INFORMATION

Pin Diagram

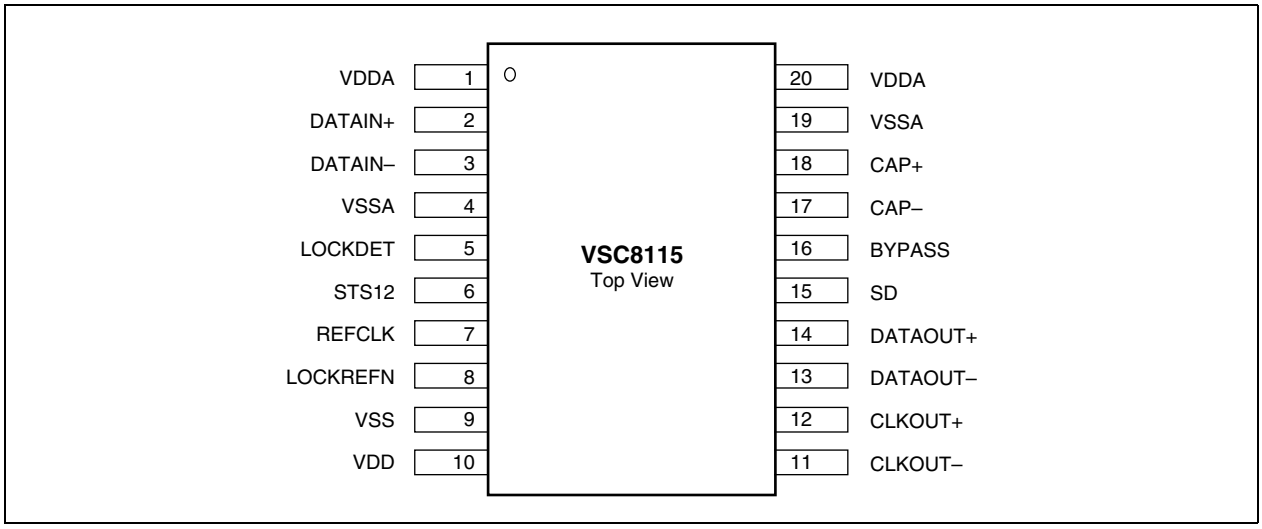


Figure 6. Pin Diagram

Pin Identifications

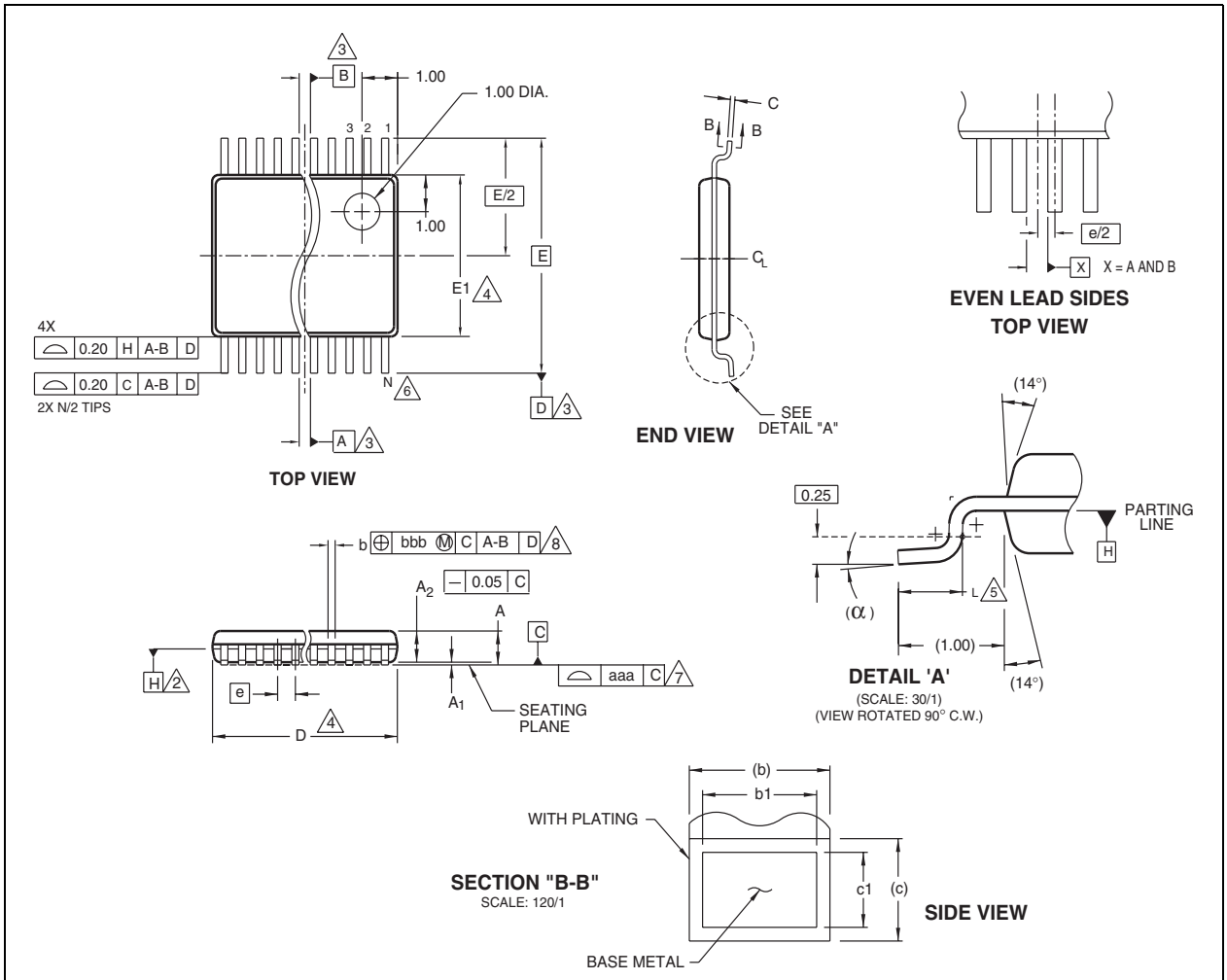
Table 12. Pin Identifications

Pin	Signal	I/O	Type	Description
1	VDDA		Pwr	3.3 V power supply for high-speed I/Os and on-chip PLL blocks.
2	DATAIN+	I	LVDS/PECL	Receive data input, true. The high-speed output clock (CLKOUT±) is recovered from this high-speed differential input data.
3	DATAIN–	I	LVDS/PECL	Receive data input, complement. The high-speed output clock (CLKOUT±) is recovered from this high-speed differential input data.
4	VSSA		Power	Ground pin for low-speed I/Os and on-chip digital PLL blocks.
5	LOCKDET	O	LVPECL	Active HIGH to indicate that the PLL is locked to serial data input and valid clock and data are present at the serial outputs (DATAOUT± and CLKOUT±). The LOCKDET will go inactive under the following conditions: • If SD is set LOW • If LOCKREFN is set LOW • If the VCO has drifted away from the local reference clock, REFCLK, by more than 500 ppm.
6	STS12	I	LVTTL	STS-12 or STS-3 mode selection. Set HIGH to select the STS-12 operation. Set LOW to select the STS-3 operation.
7	REFCLK	I	LVTTL	Local reference clock input for the CRU, 19.44 MHz. REFCLK is used for the PLL phase adjustment during power up. It also serves as a stable clock source in the absence of serial input data.
8	LOCKREFN	I	LVTTL	Lock to REFCLK input. When set LOW, this pin holds the CLKOUT± output to within ±500 ppm of the REFCLK input and forces the DATAOUT± output to the LOW state.
9	VSS		Power	Ground pin for low-speed I/Os and on-chip digital CMOS blocks.
10	VDD		Power	3.3 V power supply for low-speed I/Os and on-chip digital CMOS blocks.

Table 12. Pin Identifications *(continued)*

Pin	Signal	I/O	Type	Description
11	CLKOUT–	O	LVDS/LVPECL	High-speed clock output, complement. This clock is recovered from the receive data input (DATAIN±) and supports either LVDS or LVPECL.
12	CLKOUT+	O	LVDS/LVPECL	High-speed clock output, true. This clock is recovered from the receive data input (DATAIN±) and supports either LVDS or LVPECL.
13	DATAOUT–	O	LVDS/LVPECL	High-speed data output, complement. This is the retimed version of the receive data input (DATAIN±) and supports either LVDS or LVPECL.
14	DATAOUT+	O	LVDS/LVPECL	High-speed data output, true. This is the retimed version of the receive data input (DATAIN±) and and supports either LVDS or LVPECL.
15	SD	I	LVPECL	Signal detect. SD should be connected to the SD output on the optical module. SD is active HIGH. When SD is set HIGH, it means there is sufficient optical power. When SD is set LOW to indicate an LOS condition, the CLKOUT± output signal will be held to within +500 ppm of the RECLK input. Additionally, the DATAOUT± will be held in the LOW state.
16	BYPASS	I	LVTTL	Used for production testing. Set to V_{SS} for normal operation.
17	CAP–	I	Analog	External loop filter input, complement. The loop filter capacitor should be connected to these pins. The capacitor value should be 1.0 µF ±10%.
18	CAP+	I	Analog	External loop filter input, true. The loop filter capacitor should be connected to these pins. The capacitor value should be 1.0 µF ±10%.
19	VSSA		Power	Ground pin for low-speed I/Os and on-chip digital PLL blocks.
20	VDDA		Power	3.3 V power supply for high-speed I/Os and on-chip PLL blocks.

Package Drawing



NOTES:

1. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
2. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUM A-B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
4. 'D' & 'E1' ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D AND 0.25mm ON E PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD SHOULD BE 0.07mm FOR 0.65MM PITCH, 0.08MM FOR 0.50MM PITCH AND 0.07MM FOR 0.40MM PITCH PACKAGES. SEE SECTION "B-B".
9. SECTION 'B-B' TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.

Dimensional References (mm)			
Ref.	**Min**	**Typ**	**Max**
A			1.10
A_1	0.05		0.15
A_2	0.85	0.90	0.95
aaa		0.076	
b	0.19		0.30
b1	0.19	0.22	0.25
bbb		0.10	
c	0.09		0.20
c1	0.09	0.127	0.16
D		6.50 BSC	
E1	4.30	4.40	4.50
e		0.65 BSC	
E		6.40 BSC	
L	0.50	0.60	0.70
N		20	
α	0°		8°

Figure 7. Package Drawing

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

ORDERING INFORMATION

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8115 device.

VSC8115 STS-12/STS-3 Multirate Clock and Data Recovery Unit

Part Number	Description
VSC8115YA	20-pin TSSOP, 4.40 mm × 6.50 mm body Operating temperature: 0 °C ambient to 70 °C case
VSC8115XYA	Lead-free, 20-pin TSSOP, 4.40 mm × 6.50 mm body Operating temperature: 0 °C ambient to 70 °C case
VSC8115YA-T	20-pin TSSOP, 4.40 mm × 6.50 mm body, tape and reel Operating temperature: 0 °C ambient to 70 °C case
VSC8115XYA-T	Lead-free, 20-pin TSSOP, 4.40 mm × 6.50 mm body, tape and reel Operating temperature: 0 °C ambient to 70 °C case
VSC8115YA-02	20-pin TSSOP, 4.40 mm × 6.50 mm body Operating temperature under bias: –40 °C ambient to 85 °C case
VSC8115XYA-02	Lead-free, 20-pin TSSOP, 4.40 mm × 6.50 mm body Operating temperature under bias: –40 °C ambient to 85 °C case
VSC8115YA-02-T	20-pin TSSOP, 4.40 mm × 6.50 mm body, tape and reel Operating temperature under bias: –40 °C ambient to 85 °C case
VSC8115XYA-02-T	Lead-free, 20-pin TSSOP, 4.40 mm × 6.50 mm body, tape and reel Operating temperature under bias: –40 °C ambient to 85 °C case
VSC8115YA-03	20-pin TSSOP, 4.40 mm × 6.50 mm body Operating temperature under bias: –20 °C ambient to 85 °C case
VSC8115XYA-03	Lead-free, 20-pin TSSOP, 4.40 mm × 6.50 mm body Operating temperature under bias: –20 °C ambient to 85 °C case
VSC8115YA-03-T	20-pin TSSOP, 4.40 mm × 6.50 mm body, tape and reel Operating temperature under bias: –20 °C ambient to 85 °C case
VSC8115XYA-03-T	Lead-free, 20-pin TSSOP, 4.40 mm × 6.50 mm body, tape and reel Operating temperature under bias: –20 °C ambient to 85 °C case

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