**Advance Product Information**

# VSC8162

*2.488 Gbit/sec SONET/SDH*
*1:16 Demux with Clock Recovery*

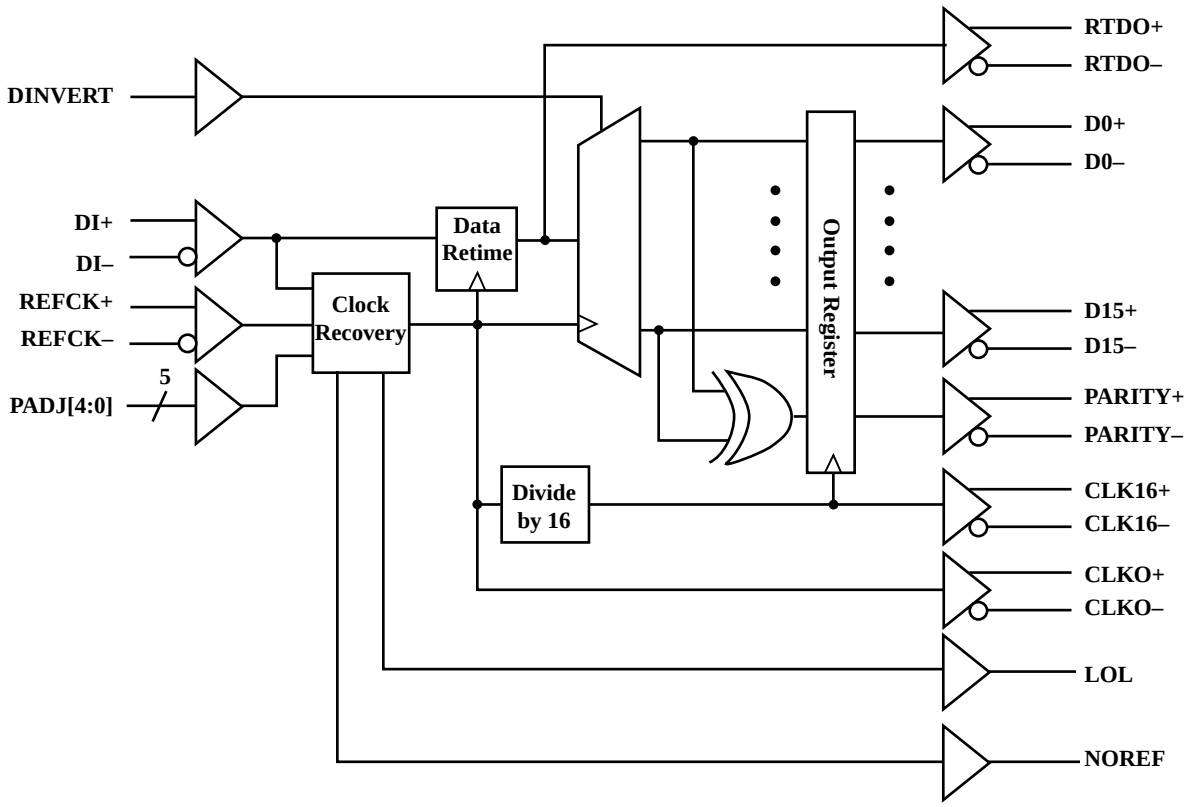
## Features

- 2.488Gb/s 1:16 Demux with Integrated Clock and Data Recovery
- Recovered Clock and Data Available
- Monolithic Phase Locked Loop
- Digitally Adjustable Serial Data Sampling Point
- Differential Low Speed Outputs
- Differential/Single-ended Reference Clock
- Loss of Lock Detection
- Meets SONET OC-48 and SDH STM-16 Jitter Tolerance Requirements

## General Description

The VSC8162 combines a clock recovery unit (CRU) with a 1:16 demultiplexer on a single chip to directly generate 16-bit wide data from an incoming 2.488Gb/s NRZ data stream. An on-chip Phase Locked Loop (PLL) generates a 2.488GHz clock which remains phase locked to the incoming data. The incoming data is retimed and demultiplexed to a 16-bit word. A Loss of Lock (LOL) signal indicates gross conditions where incoming data no longer has sufficient transitions to keep the CRU in lock.

## VSC8162 Functional Block Diagram



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## Functional Description

**Clock Recovery:**

The clock recovery unit (CRU) consists of a phase detector, voltage controlled oscillator (VCO), loop filter and frequency control unit (FCU). The components of the CRU are fully integrated on the VSC8162. A 19.44MHz reference clock (REFCLK) is required for proper operation of the Clock Recovery Unit (CRU). Jitter tolerance of the CRU is well above the SONET and SDH jitter tolerance masks. In addition, the recovered high speed clock is output on the CLKO pins.

Incoming data is presented to both the clock recovery circuit and the data retiming circuit. When the CRU is in lock mode, a phase detector circuit is effective. When there is a phase error between the incoming data and the on-chip VCO, the phase detector output raises or lowers the voltage on the loop filter to null the phase difference.

The frequency control unit (FCU) monitors the frequency difference between the reference clock, REFCK, and the recovered clock. At the time that the VCO frequency, $f_{VCO}$, and the 128x REFCK frequency, 128 x $f_{REF}$, differ by less than 1 MHz, the FCU only passively monitors the frequency difference continuously without sending any corrections to the loop filter. In the event of the loss of an input signal, or if the input is switching randomly, the VCO will drift in one direction. At the time that $f_{VCO}$ and 128 x $f_{REF}$ differ by more than 1 MHz, the FCU will maintain the VCO frequency to be at approximately 1MHz off the frequency of 128 x $f_{REF}$, and the lock detector will assert the LOL output. LOL is designed to be asserted from between 2.3us and 100us after the interruption of data.

When NRZ data is again presented at the data input, the phase detector will permit the VCO to lock to the incoming data. Hysteresis is provided which delays the deassertion of LOL until approximately 160us following the restoration of valid data.

The NOREF output will go high to indicate that there is no signal on the REFCK input, or that the REFCK is more than approximately 25% above or below the expected value.

**Retiming:**

The retiming decision circuit functions as a D Flip Flop. The recovered clock nominally clocks the decision circuit in the center of the data eye. Internally, the recovered clock is duplicated to create 32 copies, with a phase difference between each of 1/32 of a unit interval. The PADJ[4:0] inputs select which of the 32 phases are to be used to retime the data. Certain lightwave systems employing optical amplifiers suffer from noise in the leading edge of the data eye. Therefore these systems may achieve their lowest Bit Error Rate (BER) by delaying the retiming point until later in the eye. The PADJ inputs can be strapped to generate a fixed delay or the customer can develop a dynamic circuit which can select the optimum retiming point during a training sequence. The retimed high speed data can be monitored using the RTDO pins.

Figure 1 and Table 1 indicate how the PADJ pins adjust the sampling point in the data eye. The step size of each unit interval is approximately 12.5ps. The values in Table 1 are not exact and should be used only as an approximation of the expected delay. Due to environmental variations, the actual measured value at any point could vary by as much as +/- 1 step size. It should be noted that PADJ[4:0] = ‘00000’ always corresponds to the sampling center point and that the delay between unit intervals increases monotonically.



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PADJ are ECL compatible inputs (see Table 6). If the pins are left floating, the inputs will default to the logic low state. In order to set to a logic high level, the inputs can be tied directly to $V_{CC}$ without the need for a resistor.

**Table 1: Retiming Phase Adjust Settings**

| *PADJ4* | *PADJ3* | *PADJ2* | *PADJ1* | *PADJ0* | *Degrees From Center* | *PS From Center* |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0.00 | 0.0 |
| 0 | 0 | 0 | 0 | 1 | 11.25 | 12.6 |
| 0 | 0 | 0 | 1 | 0 | 22.50 | 25.1 |
| 0 | 0 | 0 | 1 | 1 | 33.75 | 37.7 |
| 0 | 0 | 1 | 0 | 0 | 45.00 | 50.2 |
| 0 | 0 | 1 | 0 | 1 | 56.25 | 62.8 |
| 0 | 0 | 1 | 1 | 0 | 67.50 | 75.4 |
| 0 | 0 | 1 | 1 | 1 | 78.75 | 87.9 |
| 0 | 1 | 0 | 0 | 0 | 90.00 | 100.5 |
| 0 | 1 | 0 | 0 | 1 | 101.25 | 113.0 |
| 0 | 1 | 0 | 1 | 0 | 112.50 | 125.6 |
| 0 | 1 | 0 | 1 | 1 | 123.75 | 138.2 |
| 0 | 1 | 1 | 0 | 0 | 135.00 | 150.7 |
| 0 | 1 | 1 | 0 | 1 | 146.25 | 163.3 |
| 0 | 1 | 1 | 1 | 0 | 157.50 | 175.8 |
| 0 | 1 | 1 | 1 | 1 | 168.75 | 188.4 |
| 1 | 0 | 0 | 0 | 0 | 180.00 | 201.0 |
| 1 | 0 | 0 | 0 | 1 | -168.75 | -188.4 |
| 1 | 0 | 0 | 1 | 0 | -157.50 | -175.8 |
| 1 | 0 | 0 | 1 | 1 | -146.25 | -163.3 |
| 1 | 0 | 1 | 0 | 0 | -135.00 | -150.7 |
| 1 | 0 | 1 | 0 | 1 | -123.75 | -138.2 |
| 1 | 0 | 1 | 1 | 0 | -112.50 | -125.6 |
| 1 | 0 | 1 | 1 | 1 | -101.25 | -113.0 |
| 1 | 1 | 0 | 0 | 0 | -90.00 | -100.5 |
| 1 | 1 | 0 | 0 | 1 | -78.75 | -87.9 |
| 1 | 1 | 0 | 1 | 0 | -67.50 | -75.4 |
| 1 | 1 | 0 | 1 | 1 | -56.25 | -62.8 |
| 1 | 1 | 1 | 0 | 0 | -45.00 | -50.2 |
| 1 | 1 | 1 | 0 | 1 | -33.75 | -37.7 |
| 1 | 1 | 1 | 1 | 0 | -22.50 | -25.1 |
| 1 | 1 | 1 | 1 | 1 | -11.25 | -12.6 |




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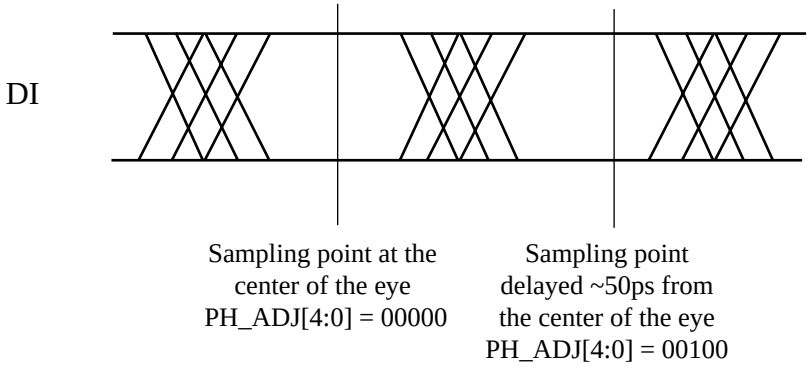
**Figure 1: Retiming Offset**




### 1:16 Demultiplexer

The demultiplexer inside of the VSC8162 consists of a 1:16 demultiplexer and timing circuitry which generates a divide-by-16 clock from the high speed clock input. The demultiplexer accepts a serial data stream input (DI+/DI-) at 2.488 Gb/s and deserializes it into 16 parallel differential outputs (D0..D15). The timing parameters of the parallel data outputs (D0..D15) are specified with respect to the falling edge of CLK16, so that CLK16 can be used to clock the destination of D0..D15.

The parity output of the demultiplexer is the XOR of all 16 parallel outputs. The DINVERT input is an ECL input (see Table 6) which can be used to invert the sense of the data through the demultiplexer. If DINVERT is left floating, it defaults to the low state, which is the state that corresponds to normal operation (no data inversion).

### FILTI, FILTO Pins

The FILTI and FILTO pins are used to provide additional capacitance to the loop filter of the VCO. To optimize the VCO's performance, it is recommended that 0.1µF, size 0805 capacitors are connected between the FILTI+ and FILTI- pins, as well as the FILTO+ and FILTO- pins.

### Supplies

The VSC8161 is designed to operate with $V_{EE}$ = -5.2V, $V_{TT}$ = -2.0V and $V_{CC}$ = GND (0.0V). However, the part can be operated in an all positive supply environment, or a mixed positive and negative supply environment.

To operate in an all positive supply environment, each of the supply voltages must be shifted up by 5.2V such that $V_{EE}$ will now be GND, $V_{TT}$ = +3.2V and $V_{CC}$ = +5.2V. To operate in a mixed positive and negative supply environment, each of the supply voltages must be shifted up by 2.0V such that $V_{TT}$ will now be GND, $V_{EE}$ = -3.2V and $V_{CC}$ = +2.0V.

Bear in mind that termination voltages must be adjusted to reflect any shift in supply voltages.



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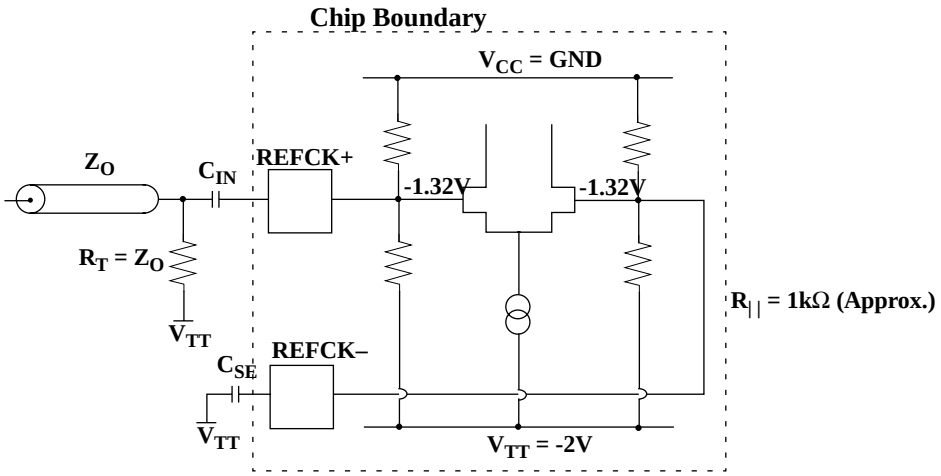
## Interface Recommendations

### REFCK+, REFCK– Inputs

Internal biasing will position the reference voltage of approximately -1.32V on both the true and complement inputs. This input can either be DC coupled or AC coupled; it can also be driven single-ended or differentially. Figure 2 shows the configuration for single-ended, AC-coupling operation. In the case of direct coupling and single-ended input, it is recommended that a stable $V_{REF}$ for ECL levels be used for the complementary input.

**Figure 2: Single-ended AC Coupling for REFCK+, REFCK– Inputs**




**$C_{IN}$ TYP = 0.1µF**
**$C_{SE}$ TYP = 0.1µF for single ended applications.**
**(Capacitor values are selected for REFCLK = 19.44 MHz)**

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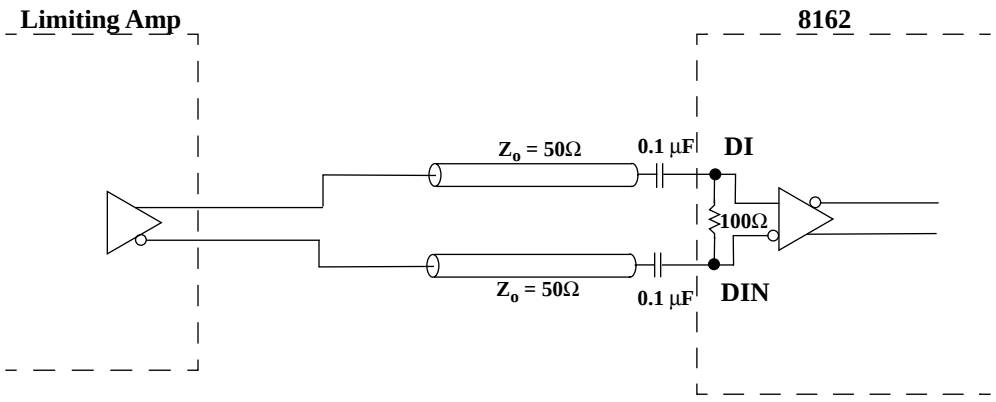
**High Speed Data Input:**

The data input receiver is internally terminated with a 100 ohm resistor between the true and complement inputs. The inputs are internally biased to allow AC coupling. These inputs are recommended to be AC coupled to permit use with a variety of limiting amplifiers. See Figure 3.

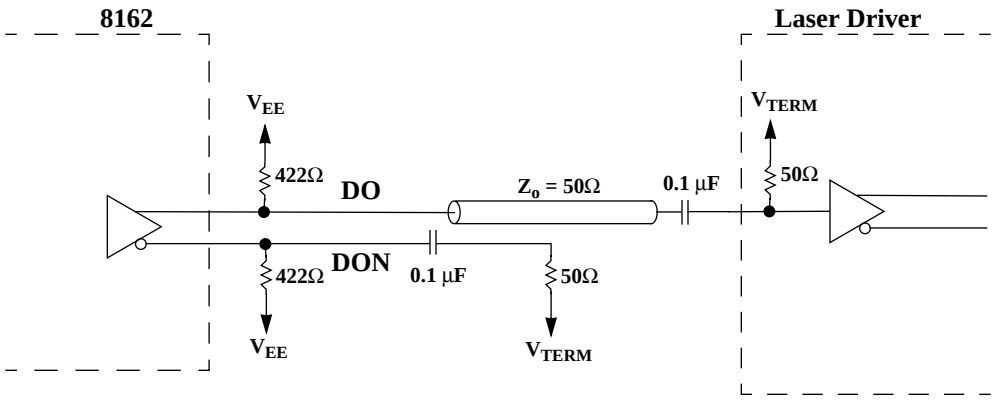
**Figure 3: High-Speed Data Input Termination**




**High Speed Data Output:**

A high speed data output termination scheme is shown in Figure 4. In order to disable the high speed data switching, the 422Ω pulldown resistors can be removed.

**Figure 4: High-Speed Data Output Termination**



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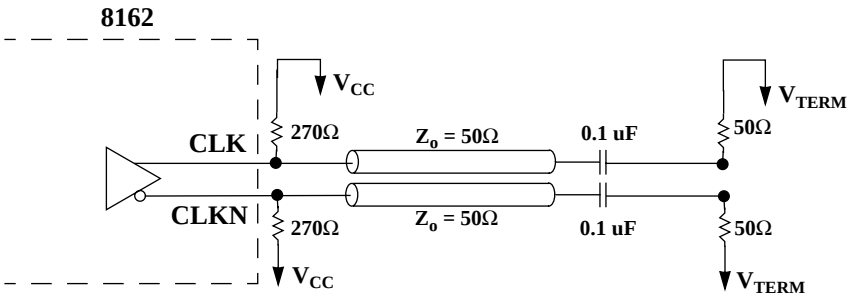
### High Speed Clock Output

The high speed clock output is provided for test and measurement purposes. A termination method for the high speed clock output is shown in Figure 5. In addition to the AC coupling method shown, the device may also be DC coupled with a 50Ω resistor connected to $V_{CC}$. By using these termination methods, a nominal voltage swing of 200mV - 300mV, single-ended peak-to-peak, can be expected.

In order to reduce noise on the board, the clock output can be disabled by using the CKOE pin. CKOE is a normal ECL input, which, when left floating, will default to a low level (output disabled). In order to set the CKOE pin to a logic high, it can be tied directly to $V_{CC}$ without the need for a resistor.

**Figure 5: High-Speed Clock Output Termination**







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**D[0-15]+/-, PARITY+/-, CLK16+/- Outputs:**

The D[0:15]+/-, PARITY+/-, and CLK16+/- output drivers are special-purpose output drivers designed for low power dissipation. Four possible termination schemes are shown in Figures 6, 7, 8, and 9.

Figures 6 and 7 are the preferred termination methods. Figure 6 indicates a DC-differential termination method, and Figure 7 is true differential termination. For interfacing the VSC8162 device directly to a VSC8161, Figure 6 is preferred since the DC differential method does not force a DC common mode level at the receiver. The VSC8161 input receivers have internal DC bias resistor that allow them to set their own DC bias level.

**Figure 6: Low-Speed Output Termination #1**

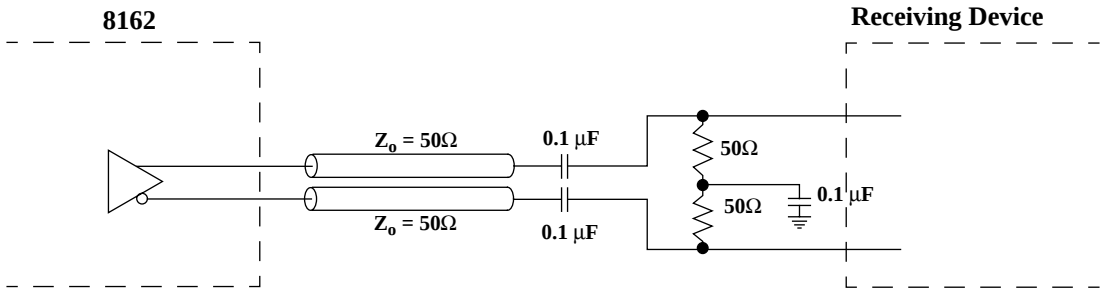


**Figure 7: Low-Speed Output Termination #2**

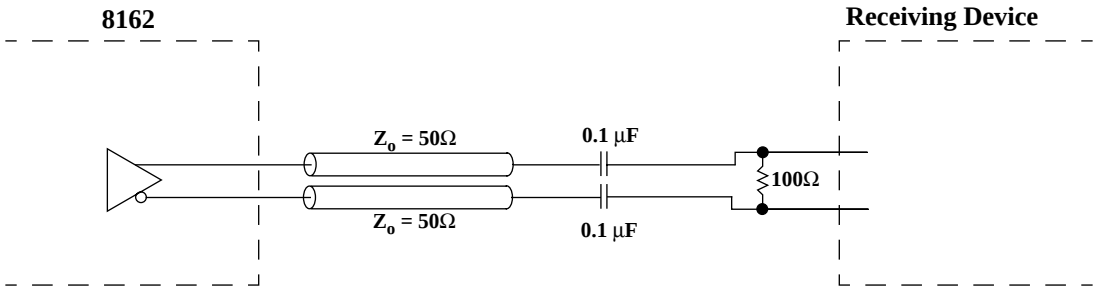




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Figure 8 is a DC coupled termination method and provides the best low frequency response. For applications with low data transition density, a DC coupling termination such as that shown in Figure 6 may be required.

**Figure 8: Low-Speed Output Termination #3**

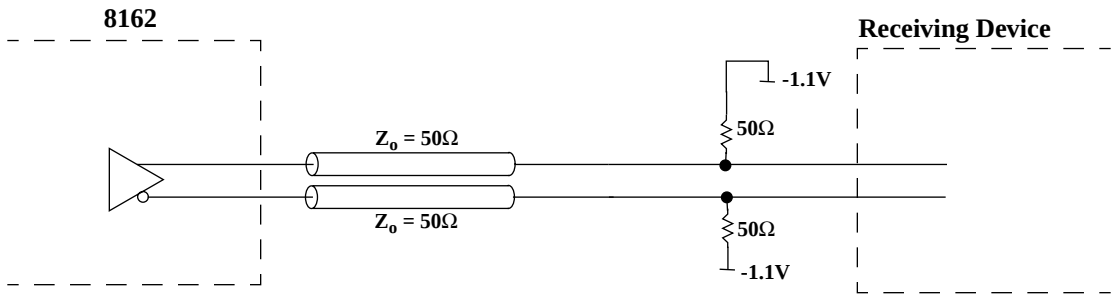
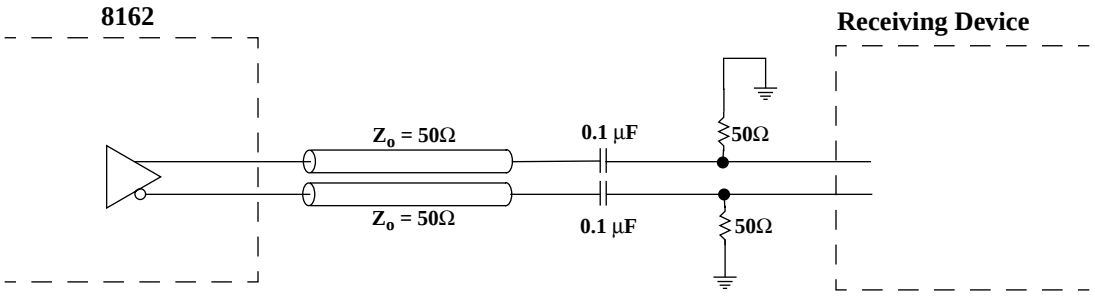



Figure 9 is provided to show that after the AC coupling capacitors, the 50Ω termination resistors can be terminated to any DC voltage, shown in Figure 9 by the ground symbol. Please note that Figure 9 will not work when interfacing the VSC8162 directly to the VSC8161.

**Figure 9: Low-Speed Output Termination #4**







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## *AC Characteristics (Over recommended operating conditions)*

**Table 2: High Speed Clock and Data Outputs Timing Characteristics**

| *Parameters* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Center of output data eye from falling edge of CLKO+ | -75 | — | +75 | ps | — |
| $t_{DH}$ | CLKO period | — | 401.9 | — | ps | — |
| $t_r$,$t_f$ | RTDO± rise and fall times | — | — | 150 | ps. | 20% to 80% into 50Ω load. |
| $t_r$,$t_f$ | CLKO± rise and fall times | — | — | 135 | ps | 20% to 80% into 50Ω load. |

**Figure 10: VSC8162 High Speed Output Interface**

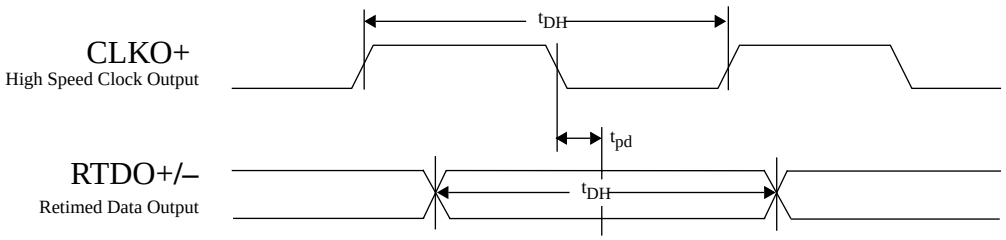


**Table 3: D[0-15]+/-, PARITY+/-, CLK16+/- Output Specifications**

| *Parameters* | *Description* | *MIN* | *Typ* | *MAX* | *Unit* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{DIFF}$ | Output level | 600 | — | 1100 | mV | — |
| $t_r$,$t_f$ | Output Rise/Fall Times | — | — | 1200 | ps | 20% to 80% into 50Ω load |
| $t_{CQ}$ | Clock-to-Data | -0.2 | — | 1.8 | ns | — |
| $t_{DC}$ | CLK16 duty cycle | 45 | — | 55 | % | — |
| $t_D$ | CLK16 period | — | 6.4 | — | ns | — |

**Figure 11: VSC8162 Parallel Interface**

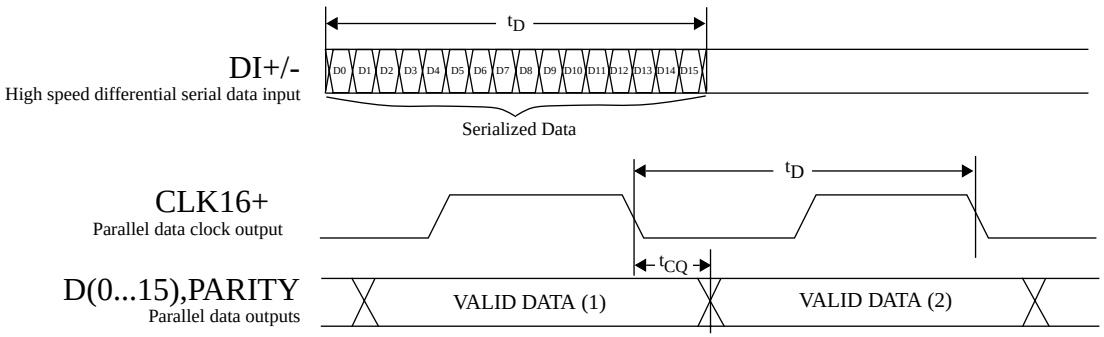




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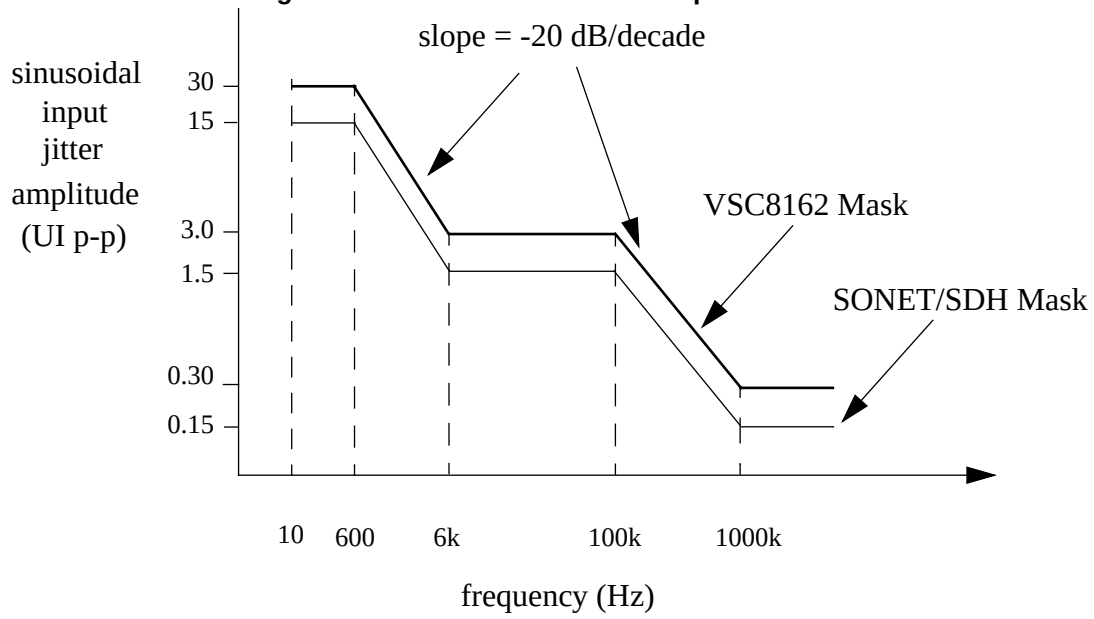
**Table 4: PLL Parameters**

| *Parameters* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $RC_d$ | REFCK Duty Cycle | 45 | — | 55 | % | — |
| $RC_f$ | REFCK Frequency | — | 19.44 | — | MHz | — |
| $\Delta f_{RC}$ | REFCK Frequency Tolerance | -100 | — | +100 | ppm | — |
| $t_{ACQ}$ | Acquisition time | — | — | 20 | µs | With valid reference clock |
| $t_{set}$ | Loss of Lock set time | 2.3 | — | 100 | µs | From data interruption |
| $t_{clr}$ | Loss of Lock clear time | 125 | — | 250 | µs | From data restoration |
| $t_{density}$ | Maximum zero-timing-content period | — | 1200 | — | UI | For 0 BER |
| $t_{jitter}$ | Jitter generation[a] | — | 3.6 | 4.0 | ps rms | — |
| $t_{tolerance}$ | Jitter tolerance[b] | Exceeds mask in Figure 9 | | | | — |

*a. Measured at the HS clock output for jitter in the 12 kHz to 20 MHz band. Assume 1.2 ps rms input data jitter*
*b. Error-free operation guaranteed when electrical input signal is subject to jitter specified by mask in Figure 9.*

**Figure 12: VSC8162 Jitter Mask Specification**







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## *DC Characteristics (Over Recommended Operating Conditions)*

### Table 5: High Speed Data and Clock Inputs and Outputs

| *Parameters* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{DIFF}$ | Serial input absolute voltage differential peak-to-peak swing (DI±) | 200 | — | 1200 | mV | — |
| $V_{CM}$ | Input common mode range | -1.6 | — | -1 | V | — |
| $R_{IN}$ | Input Resistance between DI+ and DI- | 80 | 100 | 120 | Ohm | — |
| $\Delta V_{OD}$ | Data Output voltage swing | 600 | — | 1200 | mV | — |
| $V_{ODCM}$ | Data Output common mode | -1.6 | — | -1 | V | — |
| $\Delta V_{OC}$ | Clock Output voltage swing | 100 | — | 300 | mV | — |
| $V_{OCCM}$ | Clock Output common mode | -0.2 | — | 0 | V | — |

### Table 6: Low Speed ECL Inputs and Outputs

| *Parameters* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | -1100 | — | -700 | mV | 50 ohms to $V_{TT}$ |
| $V_{OL}$ | Output LOW voltage | $V_{TT}$ | — | -1620 | mV | 50 ohms to $V_{TT}$ |
| $V_{IH}$ | Input HIGH voltage | -1040 | — | -600 | mV | — |
| $V_{IL}$ | Input LOW voltage | $V_{TT}$ | — | -1600 | mV | — |
| $I_{IH}$ | Input HIGH current | — | — | 200 | µA | — |
| $I_{IL}$ | Input LOW current | -50 | — | — | µA | — |

### Table 7: Power Supply

| *Parameters* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | -5.46 | — | -4.94 | V | — |
| $V_{TT}$ | Supply voltage | -2.1 | — | -1.9 | V | — |
| $P_D$ | Power dissipation | — | — | 4.2 | W | Outputs open |
| $I_{EE}$ | Supply Current | — | — | 620 | mA | Outputs open |
| $I_{TT}$ | Supply Current | — | — | 380 | mA | Outputs open |



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## Absolute Maximum Ratings[1]

Power Supply Voltage, ($V_{EE}$) ..... -7V to $V_{CC}$+0.5V
Power Supply Voltage, ($V_{TT}$) ..... -3V to 0.5V
DC Input Voltage (Differential inputs) ..... -2.5V to +0.5V
Output Current (Differential Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55$^{o}$ to +125$^{o}$C
Storage Temperature ..... -65$^{o}$C to +150$^{o}$C

## Recommended Operating Conditions

Power Supply Voltage, ($V_{EE}$) ..... -5.2V±5%
Power Supply Voltage, ($V_{TT}$) ..... -2.0V±5%
Operating Temperature Range ..... 0$^{o}$C Ambient to +85$^{o}$C Case Temperature

*Notes:*

*(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*




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## *Package Pin Descriptions*

**Figure 13: Package Pin Diagram**

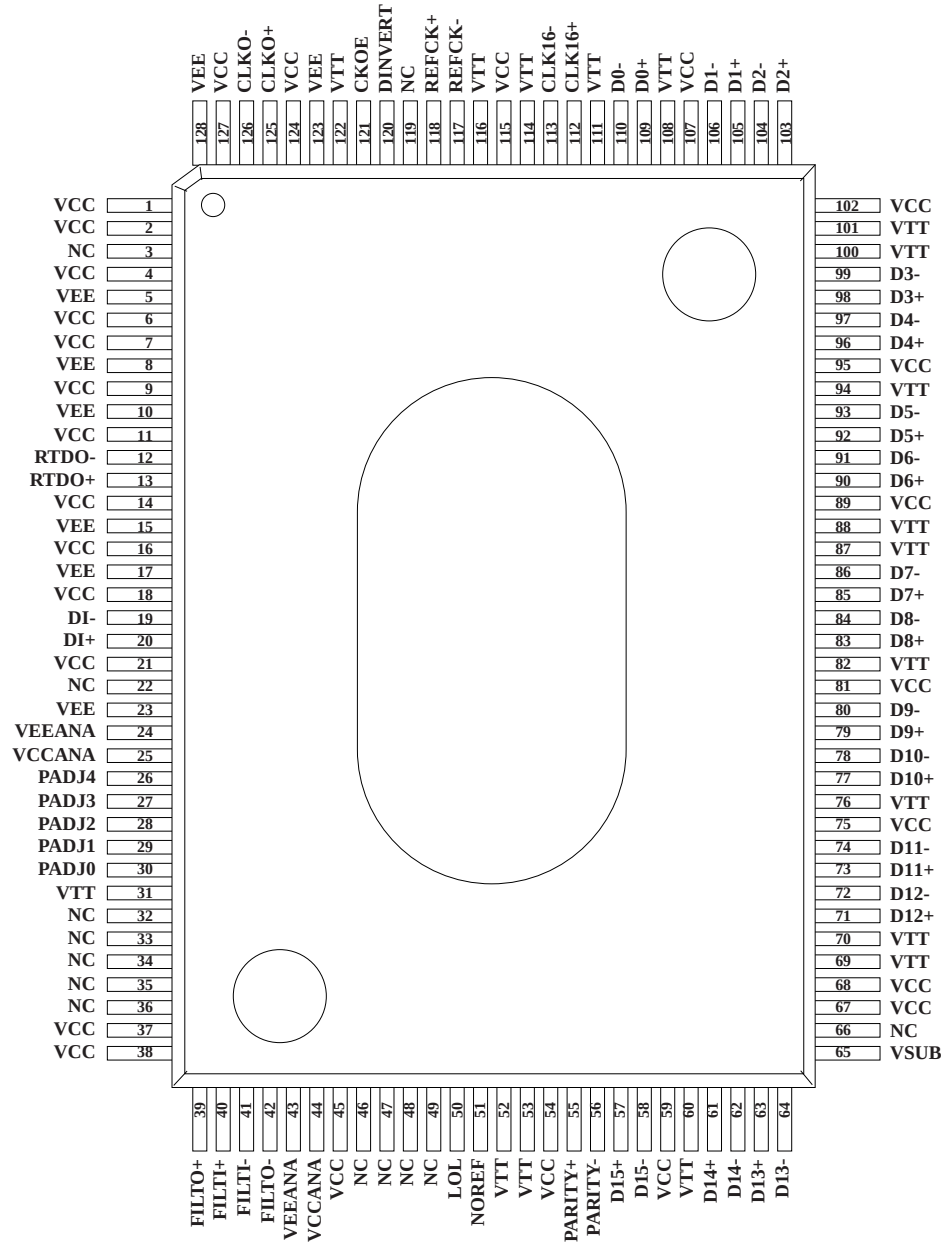






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**Table 8: Package Pin Identification**

| *Signal Name* | *Pin #* | *I/O* | *Description* |
|---|---|---|---|
| VCC | 1 | - | Power supply (GND typ.) |
| VCC | 2 | - | Power supply (GND typ.). |
| NC | 3 | - | Do not connect, leave open |
| VCC | 4 | - | Power supply (GND typ.) |
| VEE | 5 | - | Power supply (-5.2V typ.) |
| VCC | 6 | - | Power supply (GND typ.) |
| VCC | 7 | - | Power supply (GND typ.) |
| VEE | 8 | - | Power supply (-5.2V typ.) |
| VCC | 9 | - | Power supply (GND typ.) |
| VEE | 10 | - | Power supply (-5.2V typ.) |
| VCC | 11 | - | Power supply (GND typ.) |
| RTDO- | 12 | O | High speed data output (complement) |
| RTDO+ | 13 | O | High speed data output (true) |
| VCC | 14 | - | Power supply (GND typ.) |
| VEE | 15 | - | Power supply (-5.2V typ.) |
| VCC | 16 | - | Power supply (GND typ.) |
| VEE | 17 | - | Power supply (-5.2V typ.) |
| VCC | 18 | - | Power supply (GND typ.) |
| DI- | 19 | I | High speed data input (complement) |
| DI+ | 20 | I | High speed data input (true) |
| VCC | 21 | - | Power supply (GND typ.) |
| NC | 22 | - | Do not connect, leave open |
| VEE | 23 | - | Power supply (-5.2V typ.) |
| VEEANA | 24 | - | Power supply for analog circuits (-5.2V typ.) |
| VCCANA | 25 | - | Power supply for analog circuits (GND typ.) |
| PADJ4 | 26 | I | Decision circuit phase adjust |
| PADJ3 | 27 | I | Decision circuit phase adjust |
| PADJ2 | 28 | I | Decision circuit phase adjust |
| PADJ1 | 29 | I | Decision circuit phase adjust |
| PADJ0 | 30 | I | Decision circuit phase adjust |
| VTT | 31 | - | Power supply (-2.0V typ.) |
| NC | 32 | - | Do not connect, leave open |
| NC | 33 | - | Do not connect, leave open |
| NC | 34 | - | Do not connect, leave open |
| NC | 35 | - | Do not connect, leave open |
| NC | 36 | - | Do not connect, leave open |




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| *Signal Name* | *Pin #* | *I/O* | *Description* |
|---|---|---|---|
| VCC | 37 | - | Power supply (GND typ.) |
| VCC | 38 | - | Power supply (GND typ.) |
| FILTO+ | 39 | I/O | Connect to FILTI+ with 0.1 µF, 0805 capacitor |
| FILTI+ | 40 | I/O | Connect to FILTO+ with 0.1 µF, 0805 capacitor |
| FILTI- | 41 | I/O | Connect to FILTO- with 0.1 µF, 0805 capacitor |
| FILTO- | 42 | I/O | Connect to FILTI- with 0.1 µF, 0805 capacitor |
| VEEANA | 43 | - | Power supply for analog circuits (-5.2V typ.) |
| VCCANA | 44 | - | Power supply for analog circuits (GND typ.) |
| VCC | 45 | - | Power supply (GND typ.) |
| NC | 46 | - | Do not connect, leave open |
| NC | 47 | - | Do not connect, leave open |
| NC | 48 | - | Do not connect, leave open |
| NC | 49 | - | Do not connect, leave open |
| LOL | 50 | O | Loss of lock |
| NOREF | 51 | O | Loss of reference |
| VTT | 52 | - | Power supply (-2.0V typ.) |
| VTT | 53 | - | Power supply (-2.0V typ.) |
| VCC | 54 | - | Power supply (GND typ.) |
| PARITY+ | 55 | O | Parity bit (true) |
| PARITY- | 56 | O | Parity bit (complement) |
| D15+ | 57 | O | Low-speed Differential Parallel Data (true) |
| D15- | 58 | O | Low-speed Differential Parallel Data (complement) |
| VCC | 59 | - | Power supply (GND typ.) |
| VTT | 60 | - | Power supply (-2.0V typ.) |
| D14+ | 61 | O | Low-speed Differential Parallel Data (true) |
| D14- | 62 | O | Low-speed Differential Parallel Data (complement) |
| D13+ | 63 | O | Low-speed Differential Parallel Data (true) |
| D13- | 64 | O | Low-speed Differential Parallel Data (complement) |
| VSUB | 65 | - | Substrate Voltage (connect to lowest supply voltage, i.e., VEE) |
| NC | 66 | - | Do not connect, leave open |
| VCC | 67 | - | Power supply (GND typ.) |
| VCC | 68 | - | Power supply (GND typ.) |
| VTT | 69 | - | Power supply (-2.0V typ.) |
| VTT | 70 | - | Power supply (-2.0V typ.) |
| D12+ | 71 | O | Low-speed Differential Parallel Data (true) |
| D12- | 72 | O | Low-speed Differential Parallel Data (complement) |
| D11+ | 73 | O | Low-speed Differential Parallel Data (true) |
| D11- | 74 | O | Low-speed Differential Parallel Data (complement) |
| VCC | 75 | - | Power supply (GND typ.) |



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| Signal Name | Pin # | I/O | Description |
|---|---|---|---|
| VTT | 76 | - | Power supply (-2.0V typ.) |
| D10+ | 77 | O | Low-speed Differential Parallel Data (true) |
| D10- | 78 | O | Low-speed Differential Parallel Data (complement) |
| D9+ | 79 | O | Low-speed Differential Parallel Data (true) |
| D9- | 80 | O | Low-speed Differential Parallel Data (complement) |
| VCC | 81 | - | Power supply (GND typ.) |
| VTT | 82 | - | Power supply (-2.0V typ.) |
| D8+ | 83 | O | Low-speed Differential Parallel Data (true) |
| D8- | 84 | O | Low-speed Differential Parallel Data (complement) |
| D7+ | 85 | O | Low-speed Differential Parallel Data (true) |
| D7- | 86 | O | Low-speed Differential Parallel Data (complement) |
| VTT | 87 | - | Power supply (-2.0V typ.) |
| VTT | 88 | - | Power supply (-2.0V typ.) |
| VCC | 89 | - | Power supply (GND typ.) |
| D6+ | 90 | O | Low-speed Differential Parallel Data (true) |
| D6- | 91 | O | Low-speed Differential Parallel Data (complement) |
| D5+ | 92 | O | Low-speed Differential Parallel Data (true) |
| D5- | 93 | O | Low-speed Differential Parallel Data (complement) |
| VTT | 94 | - | Power supply (-2.0V typ.) |
| VCC | 95 | - | Power supply (GND typ.) |
| D4+ | 96 | O | Low-speed Differential Parallel Data (true) |
| D4- | 97 | O | Low-speed Differential Parallel Data (complement) |
| D3+ | 98 | O | Low-speed Differential Parallel Data (true) |
| D3- | 99 | O | Low-speed Differential Parallel Data (complement) |
| VTT | 100 | - | Power supply (-2.0V typ.) |
| VTT | 101 | - | Power supply (-2.0V typ.) |
| VCC | 102 | - | Power supply (GND typ.) |
| D2+ | 103 | O | Low-speed Differential Parallel Data (true) |
| D2- | 104 | O | Low-speed Differential Parallel Data (complement) |
| D1+ | 105 | O | Low-speed Differential Parallel Data (true) |
| D1- | 106 | O | Low-speed Differential Parallel Data (complement) |
| VCC | 107 | - | Power supply (GND typ.) |
| VTT | 108 | - | Power supply (-2.0V typ.) |
| D0+ | 109 | O | Low-speed Differential Parallel Data (true) |
| D0- | 110 | O | Low-speed Differential Parallel Data (complement) |
| VTT | 111 | - | Power supply (-2.0V typ.) |
| CLK16+ | 112 | O | Low-speed clock f = 155.52 MHz (true) |
| CLK16- | 113 | O | Low-speed clock f = 155.52 MHz (complement) |
| VTT | 114 | - | Power supply (-2.0V typ.) |




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| *Signal Name* | *Pin #* | *I/O* | *Description* |
|---|---|---|---|
| VCC | 115 | - | Power supply (GND typ.) |
| VTT | 116 | - | Power supply (-2.0V typ.) |
| REFCK- | 117 | I | 19.44 MHz Reference Clock (complement) |
| REFCK+ | 118 | I | 19.44 MHz Reference Clock (true) |
| NC | 119 | - | Do not connect, leave open |
| DINVERT | 120 | I | Invert Parallel Data Outputs (Logic High = Invert) |
| CKOE | 121 | I | Test input (logic high enables 2.488 GHz clock output) |
| VTT | 122 | - | Power supply (-2.0V typ.) |
| VEE | 123 | - | Power supply (-5.2V typ.) |
| VCC | 124 | - | Power supply (GND typ.) |
| CLKO+ | 125 | O | Test signal - low-swing high speed clock output (true) |
| CLKO- | 126 | O | Test signal - low-swing high speed clock output (complement) |
| VCC | 127 | - | Power supply (GND typ.) |
| VEE | 128 | - | Power supply (-5.2V typ.) |

**Table 9: Power Supply Summary**

| *Signal Name* | *Pin #* | *Description* |
|---|---|---|
| VEE | 5,8,10,15,17,23,123,128 | Power supply (-5.2V typ.) |
| VEEANA | 24,43 | Power supply for analog circuits (-5.2 typ.) |
| VTT | 31,52,53,60,69,70,76, 82,87,88,94,100,101, 108,111,114,116,122 | Power supply (-2.0V typ.) |
| VCC | 1,2,4,6,7,9,11,14,16,18, 21,37,38,45,54,59,67, 68,75,81,89,95,102,107, 115,124,127 | Power supply (GND typ.) |
| VCCANA | 25,44 | Power supply for analog circuits (GND typ.) |
| VSUB | 65 | Substrate Voltage (connect to lowest supply voltage, i.e., VEE) |

All supplies which reference the same voltage may be connected to the same power supply plane. The VCCANA, and VEEANA are noise sensitive supplies. Appropriate power supply noise suppression should be applied to optimize the performance of the device.



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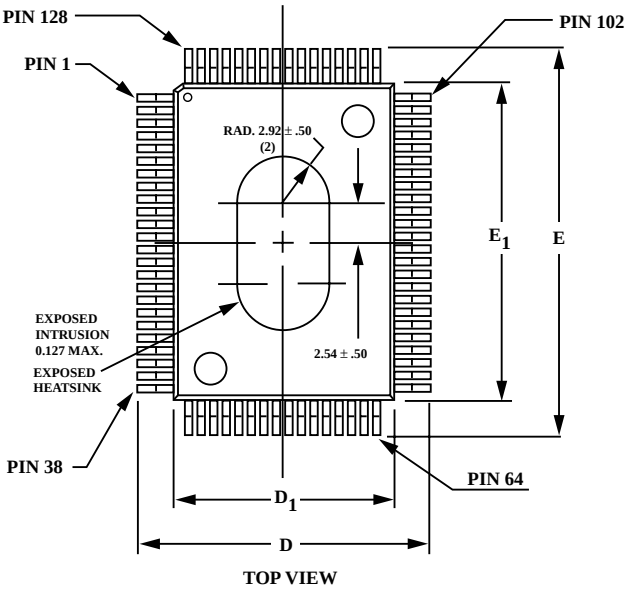
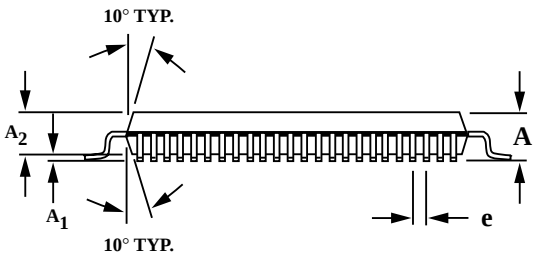
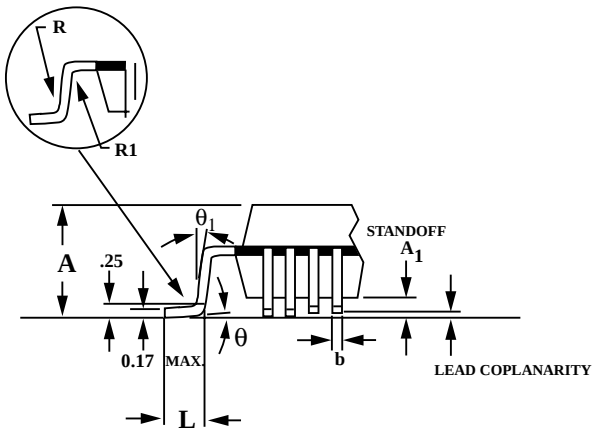
## Package Information

### 128 PQFP Package Drawings




| Key | mm | Tolerance |
|---|---|---|
| A | 2.35 | MAX |
| A1 | 0.25 | MAX |
| A2 | 2.00 | +.10 |
| D | 17.20 | ±.20 |
| D1 | 14.00 | ±.10 |
| E | 23.20 | ±.20 |
| E1 | 20.00 | ±.10 |
| L | .88 | +.15/-.10 |
| e | .50 | BASIC |
| b | .22 | ±.05 |
| θ | 0°-7° | |
| R | .30 | TYP |
| R1 | .20 | TYP |




Notes: 1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

*NOTES:*
*Package #: 101-322-5*
*Issue #: 2*

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## Notice

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## Warning

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