

Features

- 34 Input by 34 Output Crosspoint Switch
- 2.5 Gbits/sec. NRZ Data Bandwidth
- TTL Compatible μ P Interface
- Differential PECL Data Inputs
- On-chip 50 Ω Input Terminations
- 50 Ω Source Terminated PECL Output Drivers
- Single 3.3V Supply
- 14W Maximum Power Dissipation
- High Performance 256 BGA Package

General Description

The VSC835 is a monolithic 34x34 asynchronous crosspoint switch, designed to carry broadband data streams at up to 2.5 Gbit/s. The non-blocking switch core is programmed through a parallel port interface that allows random access programming of each output port. A high degree of signal integrity is maintained through the chip through fully differential signal paths.

The crosspoint function is based on a multiplexer tree architecture. Each data output is driven by a 34:1 multiplexer tree that can be programmed to one and only one of its 34 inputs, and each data input can be routed to multiple outputs. The signal path is unregistered, so no clock is required for the data inputs. The signal path is asynchronous, so there are no restrictions on the phase, frequency, or signal pattern at each input. Each input channel and each output channel has a signal monitor function that can be used to identify loss of activity (LOA). An interrupt pin is provided to signal LOA, after which an external controller can query the chip to determine the channel(s) on which the fault occurred.

Each output driver is a fully differential switched current driver with on-die back-terminations for maximum signal integrity. Data inputs are terminated on die through 50 ohm resistors terminated to V_{TERM} .

The parallel interface uses TTL levels, and provides address, data, and control pins that are compatible with a microprocessor-style interface. The control port provides access to all chip functions, including LOA and programming. Program buffering is provided to allow multiple program assignments to be queued and issued simultaneously via a single configure command.

VSC835 Block Diagram

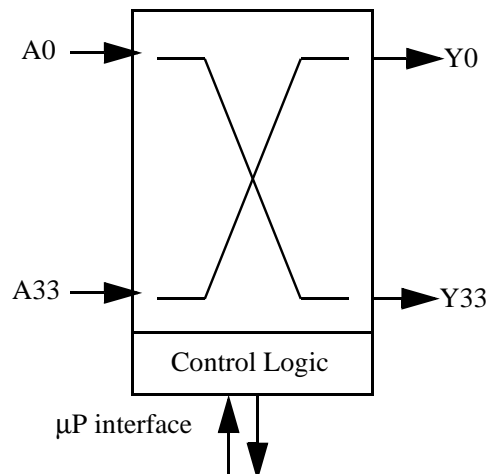
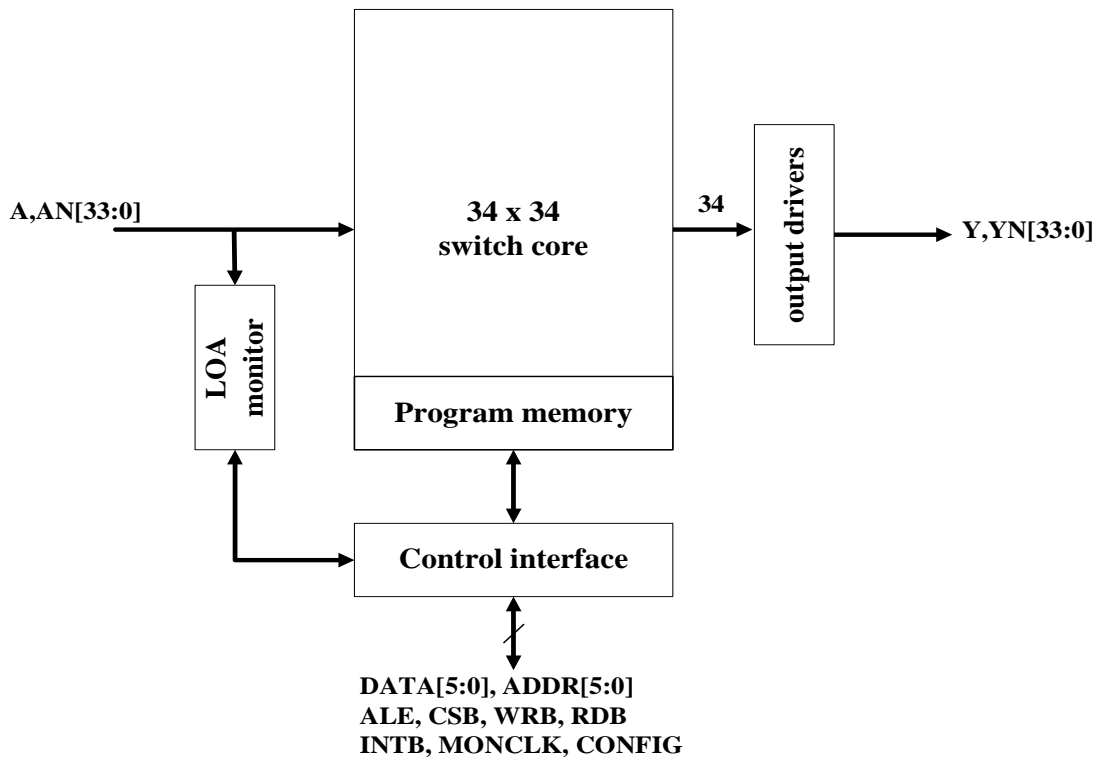


Figure 1: Detailed Block Diagram



Functional Description

Data Paths

All input data must be differential and biased to PECL levels. On-chip terminations are provided, with a nominal impedance of 50 ohms. All input termination resistors are tied to V_{TERM} .

Data outputs are provided through differential current switches with on-chip terminations that produce a PECL level output swing. The drive level of the output circuit is designed to produce standard PECL levels when terminated in 50 ohms to 2.0 volts. Other termination voltages are possible, such as to VCC or 1.3 volts, but the voltage level of the output will be shifted from its nominal value. The common-mode voltage of the output swing can be adjusted using the VCOM pins. The adjustment range is not calibrated, but typically allows for +/- 200mV of adjustment in common-mode voltage. The VCOM pin self-biases to a nominal value when left unconnected.

Output channels can be powered off in pairs if fewer than 34 outputs are required. By connecting the VEE pin associated with a given pair of outputs to VCC, the output pairs will pull to VCC and chip power will be reduced by approximately 300mW per pair.

Programming Interface

The switch core is programmed through a parallel interface circuit that allows random reads or writes to the program memory array. The program memory array is buffered to allow multiple programming instructions to be loaded simultaneously with the CONFIG pin. Parallel programming can be clocked at up to a 50MHz rate and state read-back can be performed at up to 25MHz.

The program data is composed of two parts: output address and input address. The output address, denoted by ADDR[5:0], specifies which output channel is to be programmed. The input address, denoted by DATA[5:0], specifies which input port the switch slice should connect to. The format of the program data is simple binary. For example: ADDR[5:0] (000100) / DATA[5:0] (000110) would direct output channel Y4 to connect to input channel A6. The programming state may be verified (read back) by applying the address of the desired output and asserting RDB. The programming state is unknown at power-on. Additional address space is provided for access to the monitor registers (see sections below). The microprocessor interface consists of the following signals. Levels are TTL (see DC Characteristics)

Table 1: Programming Interface Signal Table

<i>Pin</i>	<i>I/O</i>	<i>Description</i>
D[5:0]	B	Bidirectional data bus to transfer data to/from internal program registers
A[5:0]	I	Address bus to select internal program registers for read-write operations
ALE	I	ALE functionality is not implemented at this time. Tie this pin High.
CSB	I	Chip Select (Active Low): assert this pin whenever the part is being read or programmed.
WRB	I	Write (Active Low): program data will be transferred to the first level internal registers on the rising edge of this signal (when CSB is also low).
RDB	I	Read (Active Low): program data from the internal program or monitor registers will be read out on the data bus when this signal goes low (with CSB also low).
INTB	O	Interrupt (Active Low): this signal is asserted when an LOA condition is found
CONFIG	I	Configure (Active High): assert this signal to transfer queued program information from the first-level internal registers to the second-level registers, making the programming take effect. This signal may be tied high to leave the second-level registers transparent so all programming will take effect immediately. CSB must be active (low) when CONFIG is asserted. CONFIG may be tied to a high-order bit of the address bus
MONCLK	I	Monitor states are transferred to monitor registers on the rising edge of this signal. MONCLK is not expected to exceed 3MHz.

Loss of Activity (LOA) Monitoring

The LOA function consists of an activity monitor on each input channel, connected directly to the pads. The state of a monitor (whether or not it has been toggled by an input transition) can be observed by applying the address¹ of the monitor register corresponding to the signal of interest and asserting RDB. Each monitor register is four bits in length, covering the state of four inputs. There is one extra two-bit monitor for the 33rd and 34th inputs. The state of each monitor is transferred to the register on the rising edge of MONCLK, whereupon the activity monitor is cleared until more activity is detected.

1. See Memory Map Table

2.5 Gbits/sec
34x34 Crosspoint Switch with Signal Detection

If any change in a monitor state occurs after sampling by MONCLK, an interrupt will be signalled by asserting INTB, and the user must identify the offending channel by reading the monitor states. The interrupt will be cleared when the corresponding activity monitor is read, but the monitor state will not be changed. If multiple monitors have triggered the interrupt, it will persist until all the corresponding monitors have been read.

LOA requires a minimum signal level of 30-150mV peak-peak to recognize an input as active. This is required to distinguish noise on an unconnected signal (where both inputs float to the termination voltage) from activity on a live signal. A minimum of two transitions defines activity. The threshold signal level is controlled by the voltage on the VHYS pin. In order to keep the hysteresis in a useful range, it is recommended that VHYS be nominally tied to VCC (useful range is 2.0V to VCC).

Table 2: Memory Map

Address	Access	Description
00h	R/W	Output Y0's programmed input channel (write and then assert CONFIG to program)
01h	R/W	Output Y1's programmed input channel
...
21h	R/W	Output Y33's programmed input channel
22h, 23h	R/O	Rx Signal monitor for inputs [A0-A3], [A4-A7] (Logic '1'=No activity)
24h, 25h	R/O	Rx Signal monitor for inputs [A8-A11], [A12-A15]
26h, 27h	R/O	Rx Signal monitor for inputs [A16-A19], [A20-A23]
28h, 29h	R/O	Rx Signal monitor for inputs [A24-A27], [A28-A31]
2Ah	R/O	Rx Signal monitor for inputs [A32-A33]

AC Characteristics

Table 3: Data Path

Parameter	Description	Min	Typ	Max	Units
F _{RATE}	Data rate	-	-	2.5	Gbits/s
T _{ISKW}	Input channel delay skew (1)	-	300	-	ps
T _{OSKW}	Output channel delay skew (2)	-	300	-	ps
t _R , t _F	High-speed input rise/fall times, 20% to 80% (3)	-	-	150	ps
t _R , t _F	High-speed output rise/fall times, 20% to 80%	-	-	150	ps
t _{jp}	Output data eye jitter, peak-peak, 2 ³¹ PRBS (4)	-	-	100	ps

note: Unless otherwise stated, all specifications are guaranteed but not tested.

note 1: Skew between any two input channels to a given output.

note 2: Skew between any two output channels from the same input channel.

note 3: Required for high-speed output rise/fall spec at F_{RATE}=2.5 Gbits/s. For lower rate signals, use 0.375/F_{RATE}

note 4: Broadband jitter added to a jitter-free signal; jitter is primarily in the form of ISI for random data

Figure 2: Figure 2: Interrupt Timing (Change in Monitor State Registers)

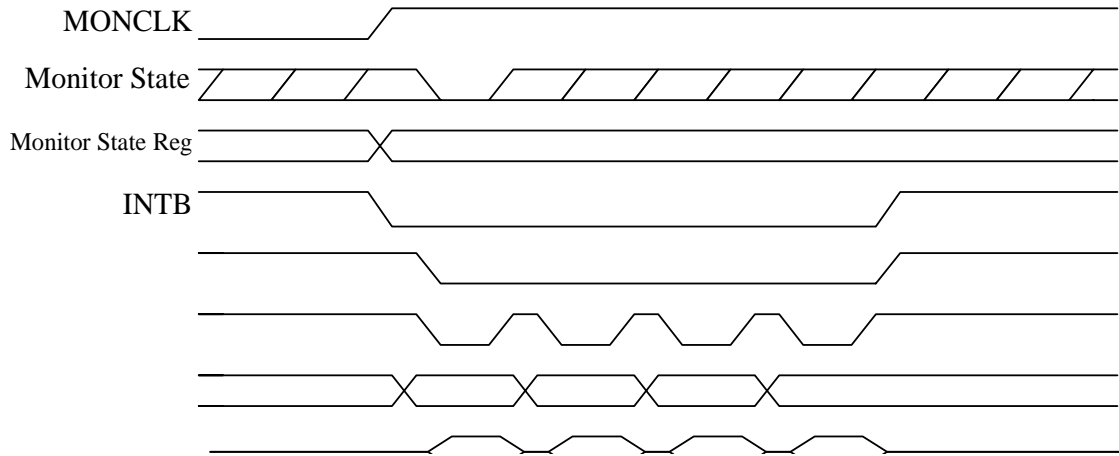


Figure 3: Figure 3: Interrupt Timing (No change in Monitor State Registers)

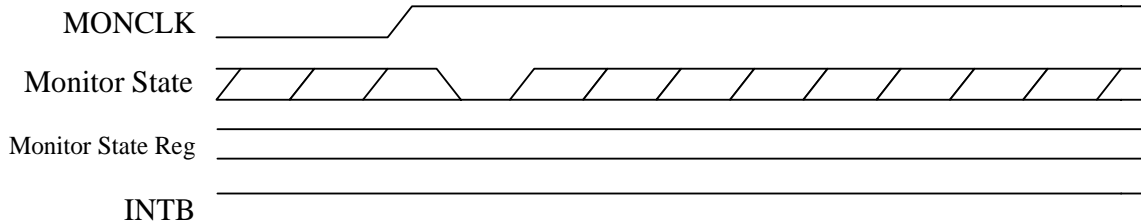


Figure 4: Figure 4: Program Timing

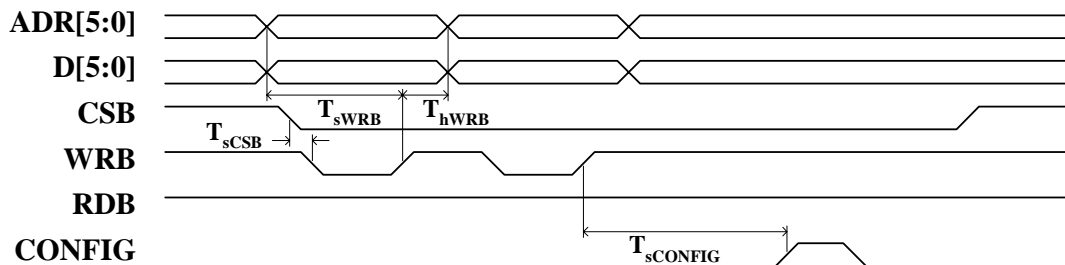


Table 4: Programming Port Interface Timing

<i>Parameter</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Units</i>
T _{config}	Switch configuration delay	-	6	ns
T _{pdADDR}	Data read propagation delay from ADDR	-	30	ns
T _{pdRDB}	Data read propagation delay from RDB (1)	-	7	ns
T _{pdint}	Interrupt propagation delay from MONCLK (2)	-	50	ns
T _{pdstate}	MONCLK to internal state register change delay (2)	-	6	ns
T _{sRDB}	ADDR to RDB setup time	5	-	ns
T _{hRDB}	RDB to ADDR hold time	3	-	ns
T _{sWRB}	WRB setup time (for either ADDR or DATA)	5	-	ns
T _{hWRB}	WRB hold time (for either ADDR or DATA)	3	-	ns
T _{sCONFIG}	WRB to CONFIG setup time	1	-	ns
T _{sCSB}	CSB setup time (to either WRB or RDB)	0	-	ns
T _{pwCONFIG}	CONFIG pulse width (high)	10	-	ns
T _{pwWRB}	WRB pulse width (low and high)	10	-	ns
T _{pwRDB}	RDB pulse width (low and high)	10	-	ns
T _{tsDATA}	DATA tri-state delay (from either RDB or CSB) (2)	-	10	ns

note 1: measured from falling edge.

note 2: measured from rising edge.

DC Characteristics (over the specified operating conditions)

Table 5: Power

<i>Parameter</i>	<i>Description</i>	<i>(Max)</i>	<i>Units</i>
I _{CC}	V _{CC} supply current	4060	mA
P _T	Total chip power	14	W
I _{TERM-V}	V _{TERM} supply current with V _{TERM} =V _{CC} -1.3V	~0	mA
I _{TERM-E}	V _{TERM} supply current with V _{TERM} =V _{CC} -2.0V	-950	mA

Note: I_{cc} Specified with outputs terminated with 50 ohms to +2.0V and Chip V_{term}=+2.0V, V_{cc} = 3.45V

Table 6: Control Port input levels (TTL)

<i>Parameter</i>	<i>Description</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
V _{IH}	Input HIGH voltage (TTL)	2.0	—	3.5	V	—
V _{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I _{IH}	Input HIGH current (TTL)	—	—	500	μA	V _{IN} = 2.4V
I _{IL}	Input LOW current (TTL)	—	—	-500	μA	V _{IN} = 0.5V
V _{OH}	Output HIGH voltage (TTL)	2.4	—	3.0	V	I _{OH} = 2mA
V _{OL}	Output LOW voltage (TTL)	0.1	—	0.4	V	I _{OL} = 1.5mA
I _{OZ}	Tri-state output current (TTL)	-100	—	100	μA	V _{OUT} = 0.4V-2.4V

Table 7: Data input levels (differential PECL)

<i>Parameter</i>	<i>Description</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
V _{ID}	Input differential voltage	400	—	1000	mV	—
V _{ICM}	Input common-mode voltage	1.8	—	2.2	V	V _{CC} =3.3V

Table 8: Data output levels (differential PECL)

<i>Parameter</i>	<i>Description</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
V _{OD}	Output differential voltage	600	—	1000	mV	note 1
V _{OCM}	Output common-mode voltage	1.8	—	2.2	V	note 1

note 1: Nominal PECL mode, VCC=VCCP=3.3V, VEE=0, terminated 50ohms to +2.0V

Absolute Maximum Ratings

Power Supply Voltage (V_{CC}) Potential to GND	-0.5 V to +4.0 V
TTL Input Voltage Applied	-0.5 V to $V_{CC}+0.5$ V
ECL Input Voltage Applied	-0.5 V to $V_{CC}+0.5$ V
Output Current (I_{OUT})	50 mA
Input Current (I_{IN})	± 50 mA
V_{TERM} Current (I_{TERM})	± 800 mA
Case Temperature Under Bias (T_C)	-55° to + 125°C
Storage Temperature (T_{STG})	-65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Operating Conditions

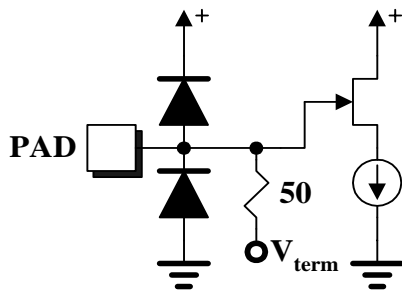
Supply voltage (V_{EE})	0 V
Supply voltage (V_{CC})	+3.3V $\pm 5\%$
Supply voltage (V_{CCP})	+3.3V $\pm 5\%$
Termination voltage (V_{TERM})	$V_{CC}-1.3$ V
Case Temperature Operating Range (T)	0° to 85°C

ESD Ratings

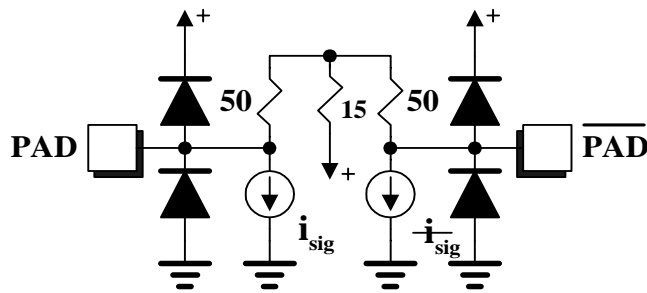
Proper ESD procedures should be used when handling this product. The VSC835 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above TBD.

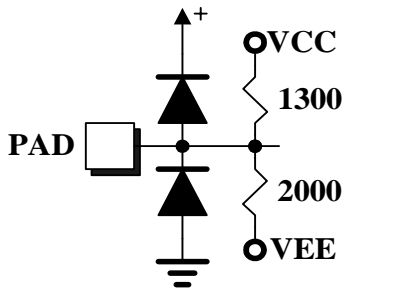
Figure 5: I/O Equivalent Circuits



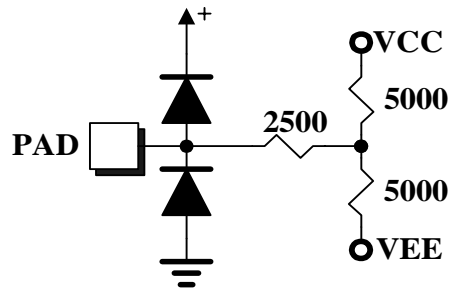
PECL Input Equivalent Circuit



PECL Output Equivalent Circuit



VCOM (L or R) Input Equivalent Circuit



VHYS Input Equivalent Circuit

Package Pin Descriptions

The VSC835 is packaged in a 27x27mm 256 pin ball grid array package. The 256 BGA package is thermally enhanced and carries the high-speed signals over controlled impedance lines from the solder ball to the circuit die. The following sections describe the pinout and mechanical details of the VSC835.

Figure 6: Functional Pinout Floorplan

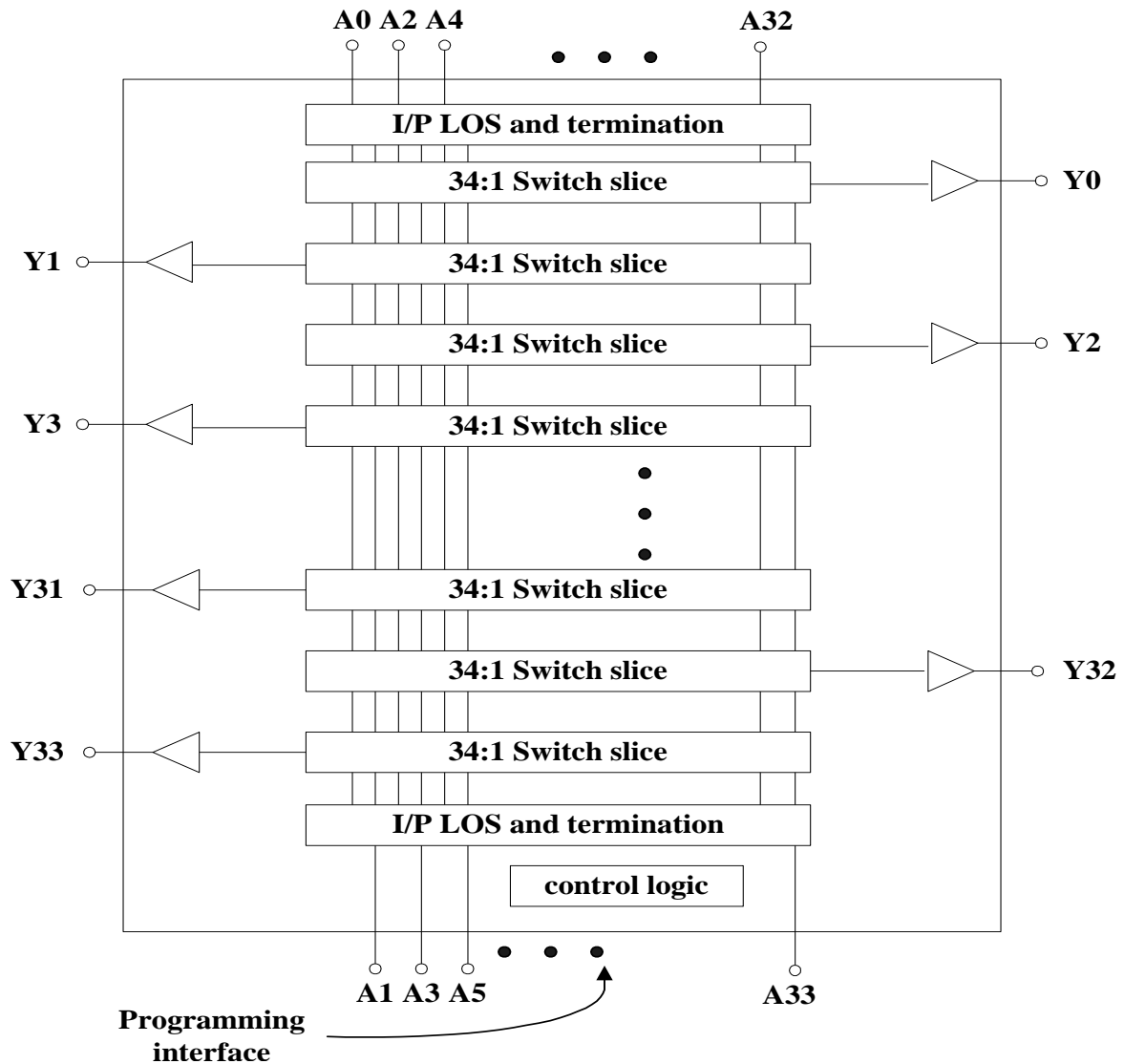


Figure 7: Pinout Diagram

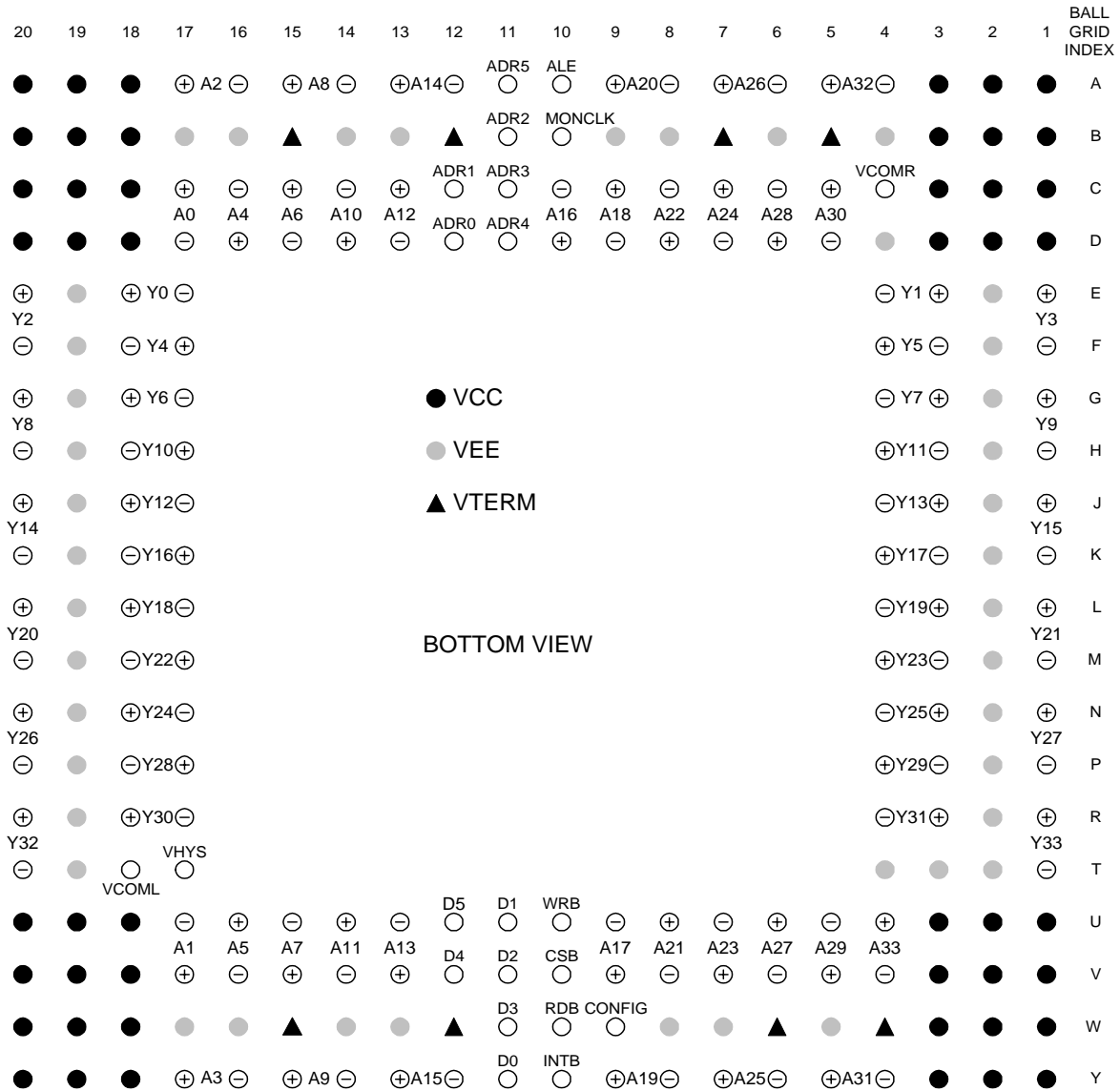


Table 9: Package Pin Identification

<i>Signal Name</i>	<i>Pin</i>	<i>Function</i>	<i>Level</i>
High Speed Data Inputs			
A0, NA0	C17, D17	Data Input	PECL
A1, NA1	V17, U17	Data Input	PECL
A2, NA2	A17, A16	Data Input	PECL
A3, NA3	Y17, Y16	Data Input	PECL
A4, NA4	D16, C16	Data Input	PECL
A5, NA5	U16, V16	Data Input	PECL
A6, NA6	C15, D15	Data Input	PECL
A7, NA7	V15, U15	Data Input	PECL
A8, NA8	A15, A14	Data Input	PECL
A9, NA9	Y15, Y14	Data Input	PECL
A10, NA10	D14, C14	Data Input	PECL
A11, NA11	U14, V14	Data Input	PECL
A12, NA12	C13, D13	Data Input	PECL
A13, NA13	V13, U13	Data Input	PECL
A14, NA14	A13, A12	Data Input	PECL
A15, NA15	Y13, Y12	Data Input	PECL
A16, NA16	D10, C10	Data Input	PECL
A17, NA17	V9, U9	Data Input	PECL
A18, NA18	C9, D9	Data Input	PECL
A19, NA19	Y9, Y8	Data Input	PECL
A20, NA20	A9, A8	Data Input	PECL
A21, NA21	U8, V8	Data Input	PECL
A22, NA22	D8, C8	Data Input	PECL
A23, NA23	V7, U7	Data Input	PECL
A24, NA24	C7, D7	Data Input	PECL
A25, NA25	Y7, Y6	Data Input	PECL
A26, NA26	A7, A6	Data Input	PECL
A27, NA27	U6, V6	Data Input	PECL
A28, NA28	D6, C6	Data Input	PECL
A29, NA29	V5, U5	Data Input	PECL
A30, NA30	C5, D5	Data Input	PECL
A31, NA31	Y5, Y4	Data Input	PECL
A32, NA32	A5, A4	Data Input	PECL
A33, NA33	U4, V4	Data Input	PECL

Table 9: Package Pin Identification

<i>Signal Name</i>	<i>Pin</i>	<i>Function</i>	<i>Level</i>
High Speed Data Outputs			
Y0, YN0	E18, E17	Data Output	PECL
Y1, YN1	E3, E4	Data Output	PECL
Y2, YN2	E20, F20	Data Output	PECL
Y3, YN3	E1, F1	Data Output	PECL
Y4, YN4	F17, F18	Data Output	PECL
Y5, YN5	F4, F3	Data Output	PECL
Y6, YN6	G18, G17	Data Output	PECL
Y7, YN7	G3, G4	Data Output	PECL
Y8, YN8	G20, H20	Data Output	PECL
Y9, YN9	G1, H1	Data Output	PECL
Y10, YN10	H17, H18	Data Output	PECL
Y11, YN11	H4, H3	Data Output	PECL
Y12, YN12	J18, J17	Data Output	PECL
Y13, YN13	J3, J4	Data Output	PECL
Y14, YN14	J20, K20	Data Output	PECL
Y15, YN15	J1, K1	Data Output	PECL
Y16, YN16	K17, K18	Data Output	PECL
Y17, YN17	K4, K3	Data Output	PECL
Y18, YN18	L18, L17	Data Output	PECL
Y19, YN19	L3, L4	Data Output	PECL
Y20, YN20	L20, M20	Data Output	PECL
Y21, YN21	L1, M1	Data Output	PECL
Y22, YN22	M17, M18	Data Output	PECL
Y23, YN23	M4, M3	Data Output	PECL
Y24, YN24	N18, N17	Data Output	PECL
Y25, YN25	N3, N4	Data Output	PECL
Y26, YN26	N20, P20	Data Output	PECL
Y27, YN27	N1, P1	Data Output	PECL
Y28, YN28	P17, P18	Data Output	PECL
Y29, YN29	P4, P3	Data Output	PECL
Y30, YN30	R18, R17	Data Output	PECL
Y31, YN31	R3, R4	Data Output	PECL
Y32, YN32	R20, T20	Data Output	PECL
Y33, YN33	R1, T1	Data Output	PECL

Table 9: Package Pin Identification

<i>Signal Name</i>	<i>Pin</i>	<i>Function</i>	<i>Level</i>
Programming Port			
ADR0	D12	Program data address	TTL
ADR1	C12	Program data address	TTL
ADR2	B11	Program data address	TTL
ADR3	C11	Program data address	TTL
ADR4	D11	Program data address	TTL
ADR5	A11	Program data address	TTL
D0	Y11	Program data	TTL
D1	U11	Program data	TTL
D2	V11	Program data	TTL
D3	W11	Program data	TTL
D4	V12	Program data	TTL
D5	U12	Program data	TTL
ALE	A10	Address latch enable (active high)	TTL
INTB	Y10	Interrupt (active low)	TTL
RDB	W10	Read enable (active low)	TTL
WRB	U10	Write enable (active low)	TTL
CONFIG	W9	Configuration strobe (active high)	TTL
CSB	V10	Chip select (active low)	TTL
MONCLK	B10	Loss of activity monitor clock (active high)	TTL
Power Supplies			
VCC	A1, A2, A3, A18, A19, A20, B1, B2, B3, B18, B19, B20, C1, C2, C3, C18, C19, C20, D1, D2, D3, D18, D19, D20, U1, U2, U3, U18, U19, U20, V1, V2, V3, V18, V19, V20, W1, W2, W3, W18, W19, W20, Y1, Y2, Y3, Y18, Y19, Y20	Power	+3.3V
VEE	B4, B6, B8, B9, B13, B14, B16, B17, D4, E2, E19, H2, H19, M2, M19, T3, T4, W5, W7, W8, W13, W14, W16, W17	Power	GND
VEE	F19	Power for Output Channels 0,2	GND
VEE	G19	Power for Output Channels 4,6	GND
VEE	J19	Power for Output Channels 8,10	GND
VEE	K19	Power for Output Channels 12,14	GND
VEE	L19	Power for Output Channels 16,18	GND

Table 9: Package Pin Identification

<i>Signal Name</i>	<i>Pin</i>	<i>Function</i>	<i>Level</i>
VEE	N19	Power for Output Channels 20,22	GND
VEE	P19	Power for Output Channels 24,26	GND
VEE	R19	Power for Output Channels 28,30	GND
VEE	T19	Power for Output Channel 32	GND
VEE	F2	Power for Output Channels 1,3	GND
VEE	G2	Power for Output Channels 5,7	GND
VEE	J2	Power for Output Channels 9,11	GND
VEE	K2	Power for Output Channels 13,15	GND
VEE	L2	Power for Output Channels 17,19	GND
VEE	N2	Power for Output Channels 21,23	GND
VEE	P2	Power for Output Channels 25,27	GND
VEE	R2	Power for Output Channels 29,31	GND
VEE	T2	Power for Output Channel 33	GND
VTERM	B5, B7, B12, B15, W4, W6, W12, W15	Termination power	+2.0V
Misc.			
VCOML	T18	Slicing level for Y0 - YN16 (even)	ANALOG
VCOMR	C4	Slicing level for Y1 - YN15 (odd)	ANALOG
VHYS	T17	Loss of activity hysteresis threshold	ANALOG

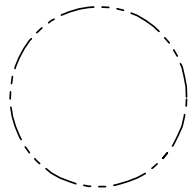
Package Information

27mm 256 BGA Package Drawing

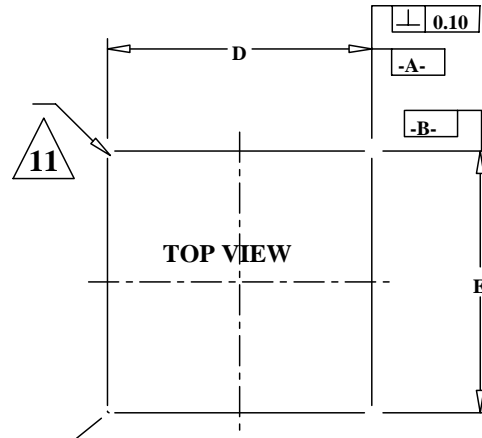
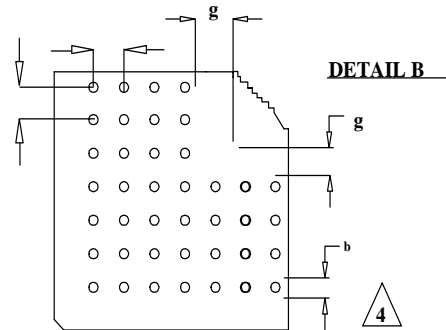
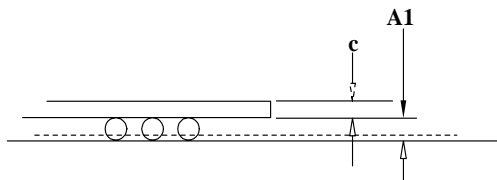
BOTTOM VIEW

19 17 15 13 11 9 7 5 3 1
20 18 16 14 12 10 8 6 4 2

A B
C D
E F
G H
J K
L M
N P
R T
U V
W Y



DETAIL B



(4 PLCS)

DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.65	1.80	1.95
A1	0.60	0.65	0.70
D	26.80	27.00	27.20
D1	24.13 (BSC.)		
E	26.80	27.00	27.20
E1	24.13 (BSC.)		
b	0.65	0.75	0.85
c	1.05	1.15	1.25
M	20		
N	256		
aaa			0.25
ccc			0.25
e	1.27 TYP.		
P	0.15		
g	0.40		
F			0.50

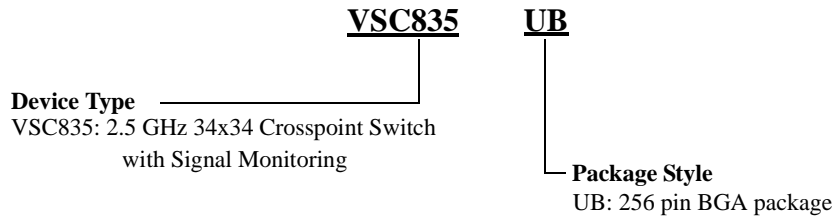
NOTES:

Datasheet VSC835

2.5 Gbits/sec
34x34 Crosspoint Switch with Signal Detection

Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

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2.5 Gbits/sec
34x34 Crosspoint Switch with Signal Detection

Datasheet
VSC835

