

VSC9186

VITESSE

VSC9186 Killington - Quad STS-48/STM-16 and STS-192/STM-64 Line Interface



FEATURES:

- (Bidirectional Quad STS-48/STM-16 or STS-192/ STM-64 Section and Line Termination Device with Pointer Processing and Time Slot Interchange
- (Accommodates a +/- 300ppm Difference Between Incoming and Local System Clock and Performs Pointer Processing on Quad Independent STS-48/ STM-16 or a Single STS-192/STM-64
- (Pointer Processing of all Concatenation Levels Including STS-192c, STS-48c, STS-12c, STS-3c, and STS-1
- (Three ports featuring 16 Serial 622Mb/s Timestream Backplane Interfaces with Integrated CDR to Other Line Interfaces or Switch ICs
- (Section/Line OH Drop/Insertion with External Interfaces on All Channels
- (Supports Section/Line Overhead Transparency
- (Protection Interface Allows Full STS-1/STM-0 Hairpinning and Drop/Continue on Both Tributary and Ring Traffic
- (Two Integrated Bidirectional 768 x 288 STS-1 Level Crossconnects
- (Embedded Hardware UPSR
- (Compliant with SONET and SDH Requirements as Stated in ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707
- (Provides JTAG TAP Controller Conforming to the IEEE 1149.1 Standard
- (Bidirectional Path Monitoring

SPECIFICATIONS:

- (2.5V I/O and 1.8V Core Power Supplies
- (0.18 μ CMOS Technology
- (720-pin CCGA /1.0mm Column Pitch
- (10W Maximum Power Consumption

SPLITTER/COMBINER MODE (DWDM):

- (Four independently-timed 2.5Gb/s SONET/SDH signals are received, terminated, and monitored at the line level. They are pointer processed to the local time domain, passed through an STS-1 level crossconnect, and are multiplexed to a STS-192/STM-64 signal. A STS-192/STM-64 is received in the opposite direction and pointer processed to a local clock. The signal is crossconnected at the STS-1 level and then demultiplexed to four STS-48/STM-16 signals. Full section and line termination are performed at all five SONET Tx and Rx interfaces. Overhead transparency is supported through an external interface for maximum customer flexibility.
- (Two Killington devices may be used in an East/West ring configuration forming a logical 40Gb/s crossconnect. Two bidirectional interfaces allow loopback of all four STS-48/STM-16 and the STS-192/ STM-64 interfaces simultaneously.

ADD/DROP MULTIPLEXING (ADM) MODE:

- (Four independently-timed 2.5Gb/s signals or a single 10Gb/s SONET/SDH signal are received, terminated, and monitored at the line level. The incoming 192 STS-1 signals are sent through a 768 x 288 STS-1 TSI switch that allows ring loopback or hairpinning of tributaries from either the line interface or the backplane interface. B1 parity is supported on both interfaces for backplane integrity monitoring.
- (The backplane receive circuitry has built-in data recovery and realignment of +/- 100 ns on all 16 working and protection LVDS inputs. These signals are then crossconnected again at the STS-1 level through a 768 x 288 TSI and transmitted to either four STS-48/STM-16 or one STS-192/STM-64 interface.

GENERAL DESCRIPTION:

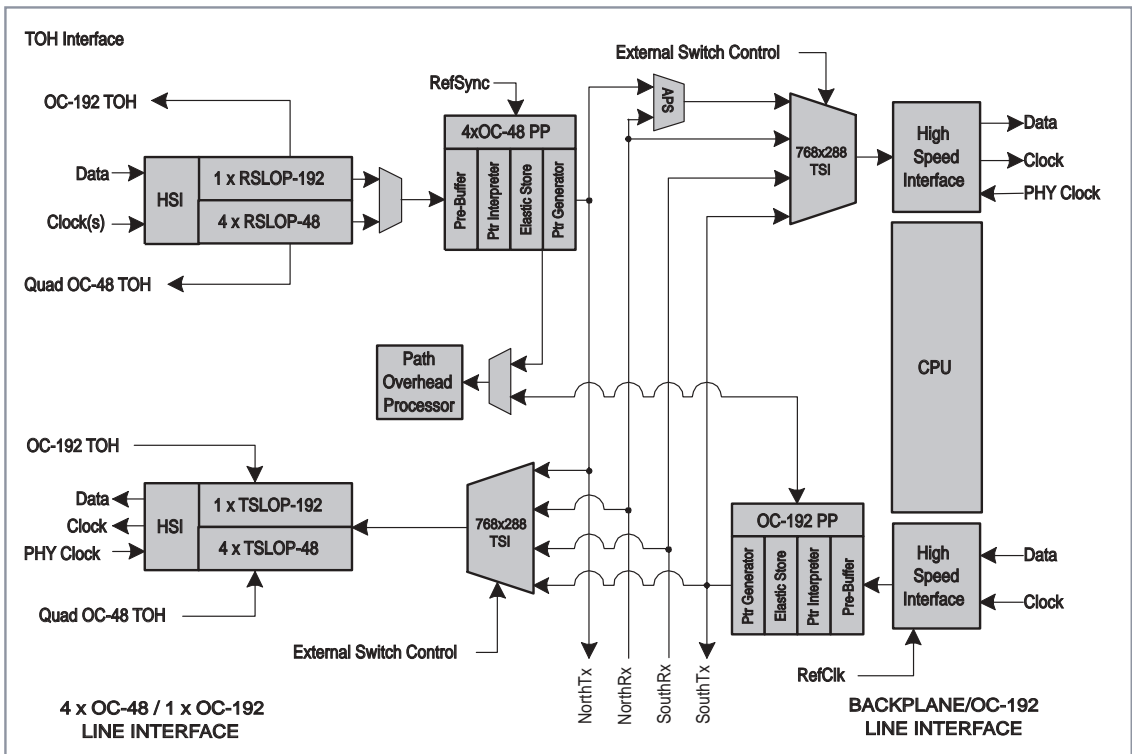


The VSC9186 is a bidirectional quad STS-48/STM-16 or OC-192/STM-64 framer and pointer processor. In addition to full path overhead monitoring, section and line termination are available on line inputs and outputs. A bidirectional protection interface allows both line and tributary traffic to be looped back simultaneously through a companion device. The UPSR is implemented entirely in hardware driven by the STE/LTE logic, pointer interpreter and path overhead monitor.

The VSC9186 can be used in SONET/SDH applications such as Time Slot Interchange (TSI) switches, digital crossconnects, add/drop multiplexers, and DWDM terminal multiplexer applications.

The VSC9186 supports TOH transparency off-chip using the XILINX Virtex II (XC2V1000-4FG256C). A verified reference design is available with purchase.

VSC9186 BLOCK DIAGRAM:



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